



## 1. Description

### 1.1. Project

Project Name	polyphony
Board Name	custom
Generated with:	STM32CubeMX 6.3.0
Date	08/26/2021

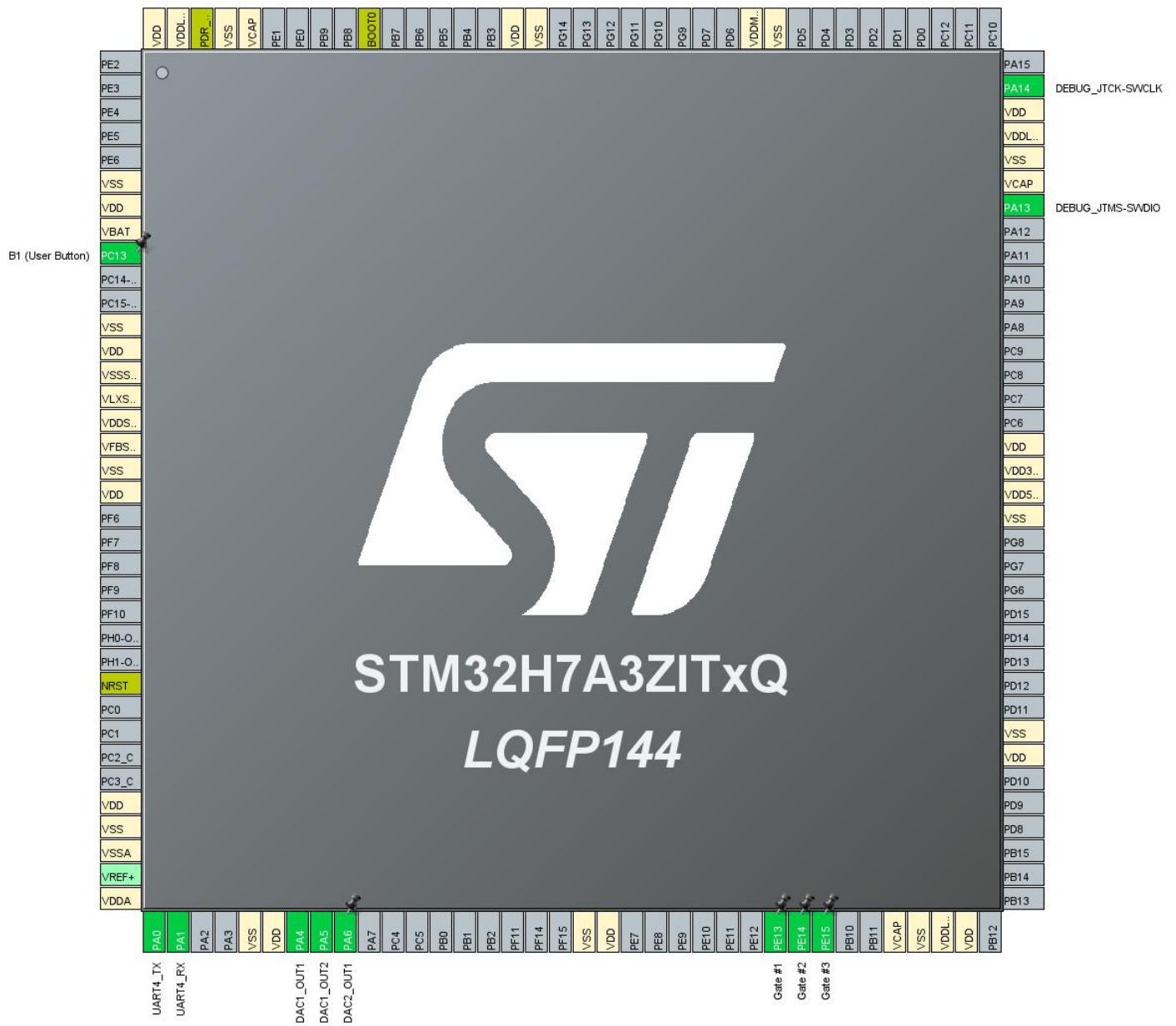
### 1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H7A3/7B3
MCU name	STM32H7A3ZITxQ
MCU Package	LQFP144
MCU Pin number	144

### 1.3. Core(s) information

Core(s)	Arm Cortex-M7
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## 2. Pinout Configuration



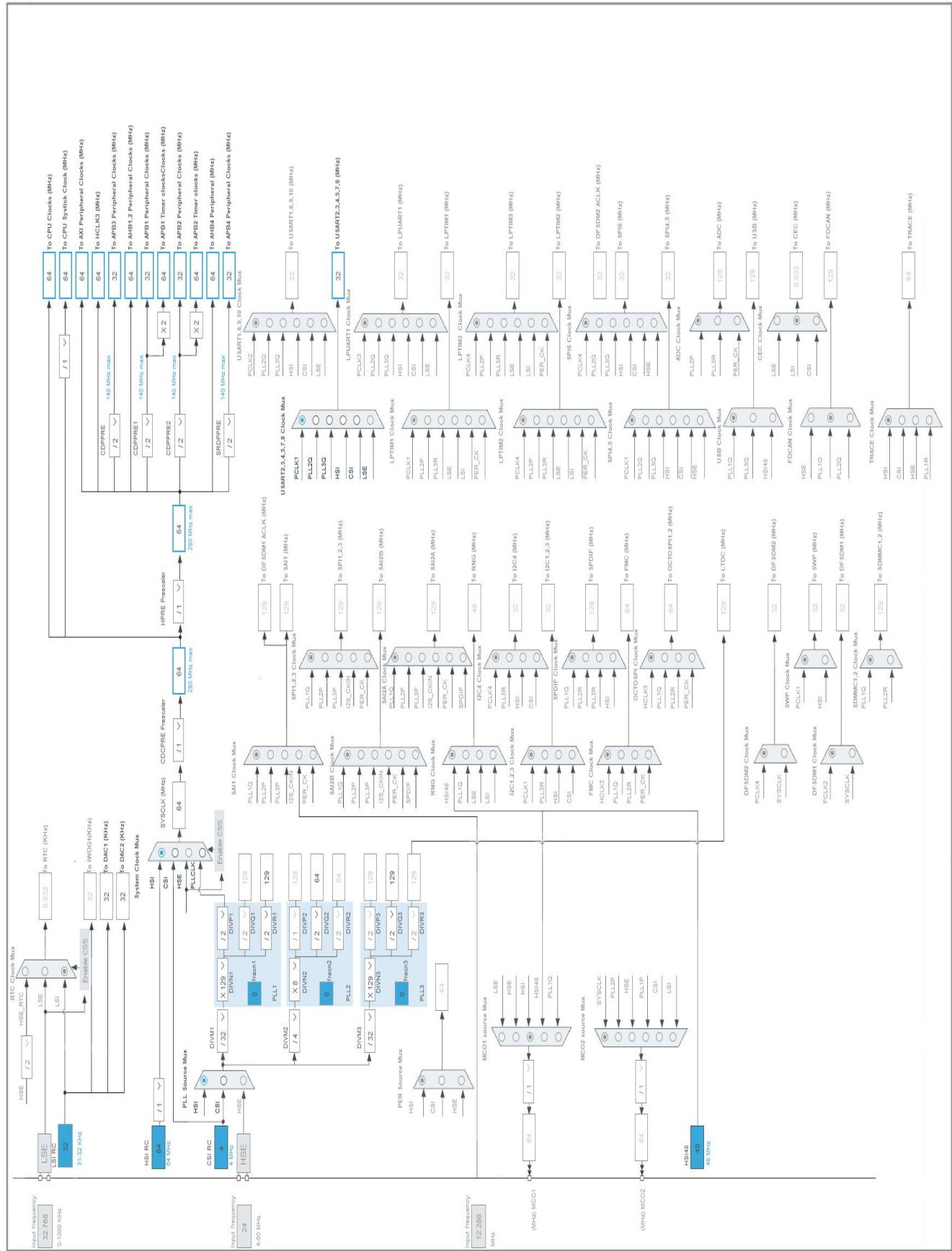
### 3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VSS	Power		
7	VDD	Power		
8	VBAT	Power		
9	PC13 *	I/O	GPIO_Input	B1 (User Button)
12	VSS	Power		
13	VDD	Power		
14	VSSMPS	Power		
15	VLXMPS	Power		
16	VDDSMPS	Power		
17	VFBSMPS	Power		
18	VSS	Power		
19	VDD	Power		
27	NRST	Reset		
32	VDD	Power		
33	VSS	Power		
34	VSSA	Power		
36	VDDA	Power		
37	PA0	I/O	UART4_TX	
38	PA1	I/O	UART4_RX	
41	VSS	Power		
42	VDD	Power		
43	PA4	I/O	DAC1_OUT1	
44	PA5	I/O	DAC1_OUT2	
45	PA6	I/O	DAC2_OUT1	
55	VSS	Power		
56	VDD	Power		
63	PE13 *	I/O	GPIO_Output	Gate #1
64	PE14 *	I/O	GPIO_Output	Gate #2
65	PE15 *	I/O	GPIO_Output	Gate #3
68	VCAP	Power		
69	VSS	Power		
70	VDDLDO	Power		
71	VDD	Power		
79	VDD	Power		
80	VSS	Power		
89	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
90	VDD50_USB	Power		
91	VDD33_USB	Power		
92	VDD	Power		
102	PA13	I/O	DEBUG_JTMS-SWDIO	
103	VCAP	Power		
104	VSS	Power		
105	VDDLDO	Power		
106	VDD	Power		
107	PA14	I/O	DEBUG_JTCK-SWCLK	
118	VSS	Power		
119	VDDMMC	Power		
128	VSS	Power		
129	VDD	Power		
135	BOOT0	Boot		
140	VCAP	Power		
141	VSS	Power		
142	PDR_ON	Reset		
143	VDDLDO	Power		
144	VDD	Power		

\* The pin is affected with an I/O function

## 4. Clock Tree Configuration



## 5. Software Project

### 5.1. Project Settings

Name	Value
Project Name	polyphony
Project Folder	C:\Users\furkle\STM32CubeIDE\workspace_1.6.1\polyphony
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.9.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_UART4_Init	UART4
5	MX_DAC1_Init	DAC1
6	MX_TIM16_Init	TIM16
7	MX_DAC2_Init	DAC2

## 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H7A3/7B3
MCU	STM32H7A3ZITxQ
Datasheet	DS13139_Rev0

### 6.2. Parameter Selection

Temperature	25
Vdd	3.0

### 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1



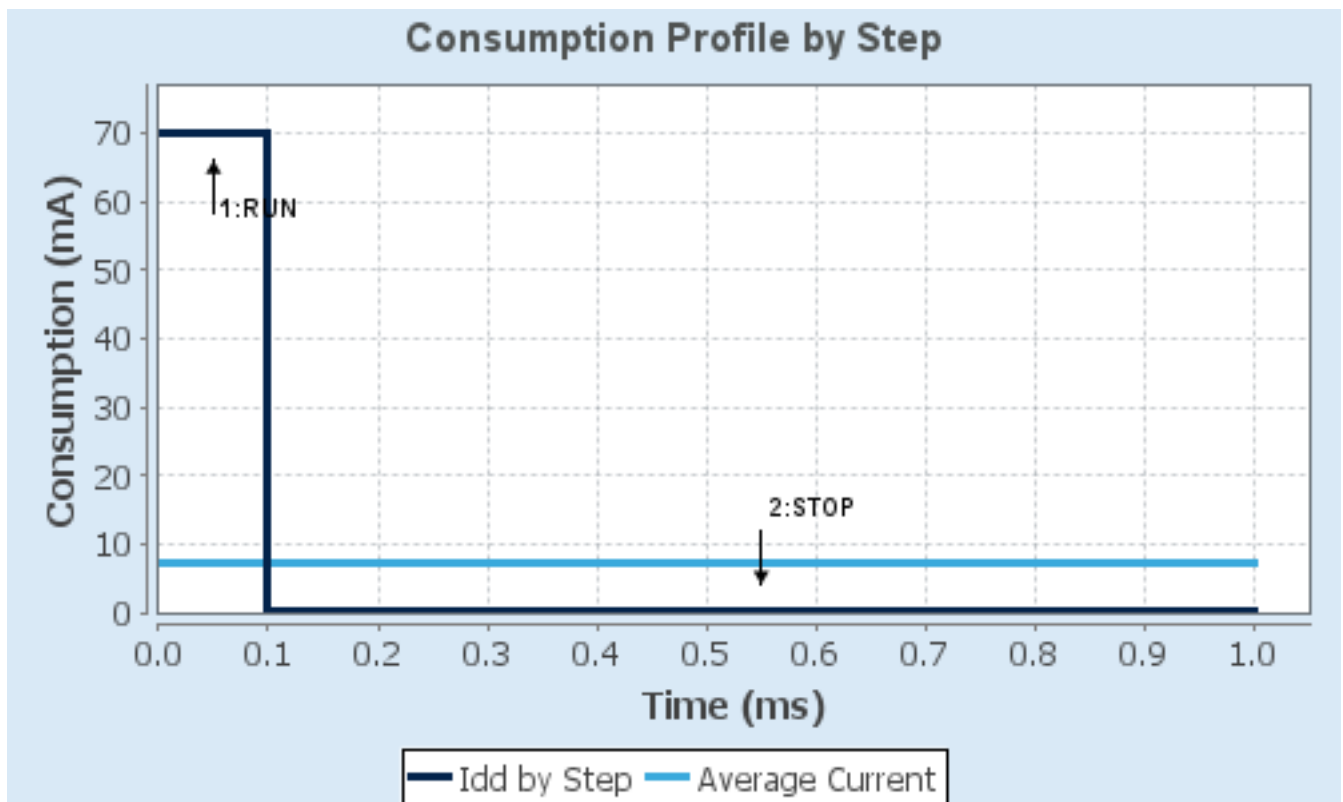
#### 6.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	3.0	3.0
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	VOS0	SVOS5
<b>SRDomain</b>	DRUN	DSTOP
<b>n/a</b>	SRDRUN	SRDSTOP
<b>Fetch Type</b>	ITCM/DTCM/Cache	NA
<b>CPU Frequency</b>	280 MHz	64 MHz
<b>Clock Configuration</b>	HSE PLL	HSI Flash-ON
<b>Clock Source Frequency</b>	16 MHz	64 MHz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	69.92 mA	263.82 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	599.0	0.0
<b>Ta Max</b>	115.77	124.97
<b>Category</b>	In DS Table	In DS Table

#### 6.5. Results

Sequence Time	1 ms	Average Current	7.23 mA
Battery Life	19 days, 14 hours	Average DMIPS	599.2 DMIPS

#### 6.6. Chart



## 7. Peripherals and Middlewares Configuration

### 7.1. DAC1

**OUT1 connected to: both external pin and on chip analog peripherals**

**OUT2 connected to: both external pin and on chip analog peripherals**

#### 7.1.1. Parameter Settings:

##### **DAC Out1 Settings:**

Mode selected	Normal Mode
Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming
On chip peripheral(s)	not yet connected

##### **DAC Out2 Settings:**

Mode selected	Normal Mode
Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming
On chip peripheral(s)	not yet connected

### 7.2. DAC2

**OUT1 connected to: both external pin and on chip analog peripherals**

#### 7.2.1. Parameter Settings:

##### **DAC Out1 Settings:**

Mode selected	Normal Mode
Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming
On chip peripheral(s)	not yet connected

### 7.3. DEBUG

**Debug: Serial Wire**

### 7.4. RCC

#### 7.4.1. Parameter Settings:

#### Power Parameters:

SupplySource	PWR_DIRECT_SMPS_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 3

#### RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	32

#### System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	2 WS (3 CPU cycle)

## 7.5. SYS

**Timebase Source: SysTick**

## 7.6. TIM16

**mode: Activated**

### 7.6.1. Parameter Settings:

#### Counter Settings:

Prescaler (PSC - 16 bits value)	<b>7999 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>100 *</b>
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

## 7.7. UART4

**Mode: Asynchronous**

### 7.7.1. Parameter Settings:

#### Basic Parameters:

Baud Rate	<b>31250 *</b>
Word Length	8 Bits (including Parity)

Parity	None
Stop Bits	1

#### Advanced Parameters:

Data Direction	<b>Receive Only *</b>
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

#### Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

**\* User modified value**

## 8. System Configuration

### 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	
	PA5	DAC1_OUT2	Analog mode	No pull-up and no pull-down	n/a	
DAC2	PA6	DAC2_OUT1	Analog mode	No pull-up and no pull-down	n/a	
DEBUG	PA13	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
UART4	PA0	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	B1 (User Button)
	PE13	GPIO_Output	Output Push Pull	<b>Pull-down *</b>	Low	Gate #1
	PE14	GPIO_Output	Output Push Pull	<b>Pull-down *</b>	Low	Gate #2
	PE15	GPIO_Output	Output Push Pull	<b>Pull-down *</b>	Low	Gate #3

## 8.2. DMA configuration

DMA request	Stream	Direction	Priority
UART4_RX	DMA1_Stream0	Peripheral To Memory	Low

### UART4\_RX: DMA1\_Stream0 DMA request Settings:

Mode: **Circular \***  
Use fifo: Disable  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

## 8.3. BDMA1 configuration

nothing configured in DMA service

## 8.4. BDMA2 configuration

nothing configured in DMA service

## 8.5. MDMA configuration

nothing configured in DMA service

## 8.6. NVIC configuration

### 8.6.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream0 global interrupt	true	0	0
UART4 global interrupt	true	0	0
TIM16 global interrupt	true	0	0
PVD and PVM interrupts through EXTI line	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	unused		
FPU global interrupt	unused		
HSEM1 global interrupt	unused		
DAC2 global interrupt	unused		
ECC diagnostic Global Interrupt	unused		

### 8.6.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream0 global interrupt	false	true	true
UART4 global interrupt	false	true	true
TIM16 global interrupt	false	true	true



**\* User modified value**

## 9. System Views

### 9.1. Category view

#### 9.1.1. Current

Middleware									
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing	Trace and Debug	Power and Thermal	
BDMA1	DAC1 ✓	TIM16 ✓	UART4 ✓				DEBUG ✓		
BDMA2	DAC2 ✓								
CORTEX_M7 ✓									
DMA ✓									
GPIO ✓									
MDMA									
IVIC ✓									
RCC ✓									
SYS ✓									

## 10. Docs & Resources

Type	Link
Datasheet	<a href="http://www.st.com/resource/en/datasheet/DM00674683.pdf">http://www.st.com/resource/en/datasheet/DM00674683.pdf</a>
Reference manual	<a href="http://www.st.com/resource/en/reference_manual/DM00463927.pdf">http://www.st.com/resource/en/reference_manual/DM00463927.pdf</a>
Programming manual	<a href="http://www.st.com/resource/en/programming_manual/DM00237416.pdf">http://www.st.com/resource/en/programming_manual/DM00237416.pdf</a>
Errata sheet	<a href="http://www.st.com/resource/en/errata_sheet/DM00598144.pdf">http://www.st.com/resource/en/errata_sheet/DM00598144.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00167594.pdf">http://www.st.com/resource/en/application_note/CD00167594.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00211314.pdf">http://www.st.com/resource/en/application_note/CD00211314.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00259245.pdf">http://www.st.com/resource/en/application_note/CD00259245.pdf</a>
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