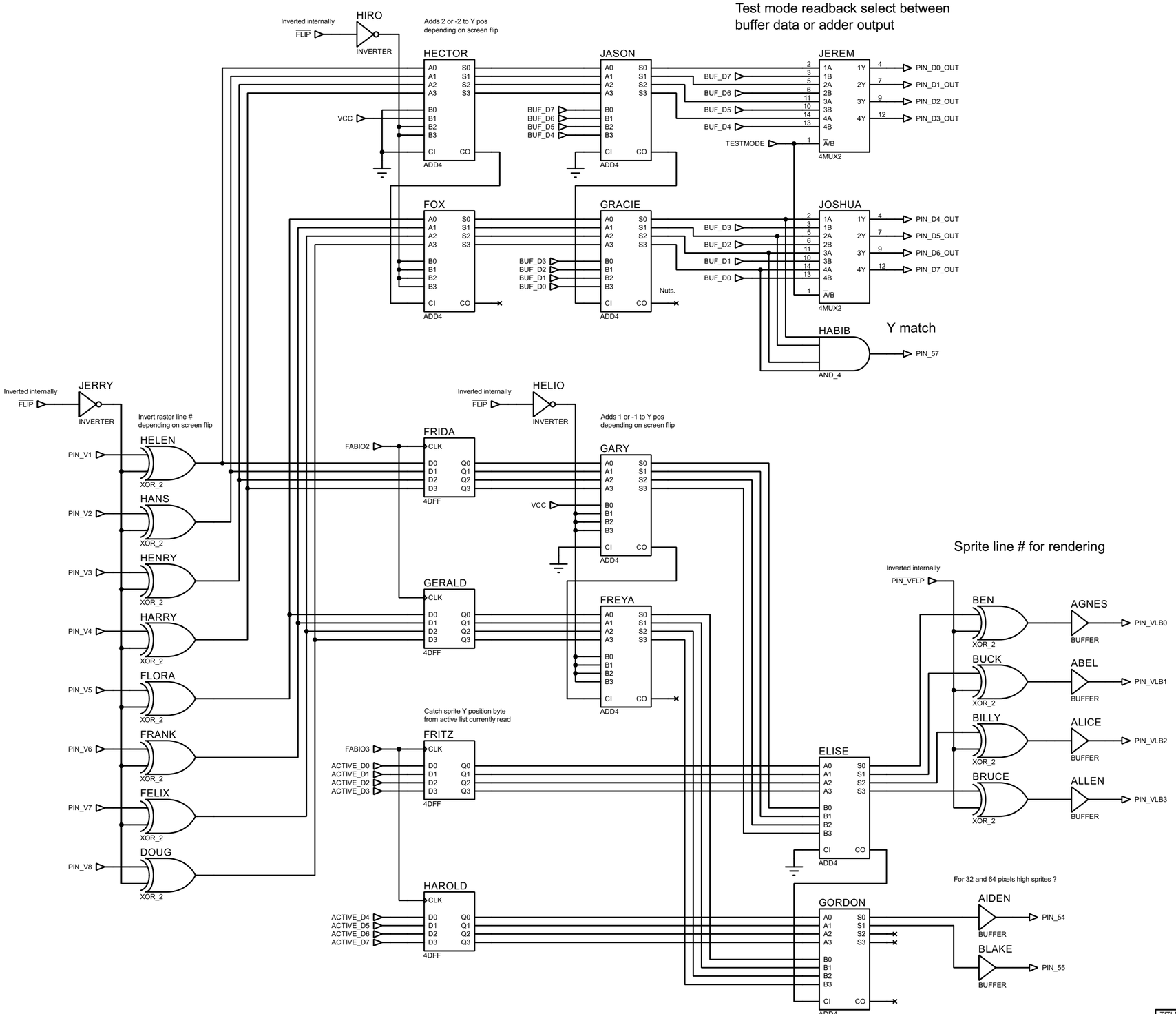
Test mode readback select between buffer data or adder output
Inverted internally
FLIP
INVERTER
HIRO
Adds 2 or -2 to Y pos depending on screen flip
HECTOR
JASON
JEREM
A0 A1 A2 A3
S0 S1 S2 S3
B0 B1 B2 B3
CI CO
ADD4
VCC
BUF_D7 BUF_D6 BUF_D5 BUF_D4
TESTMODE
1A 1B 2A 2B 3A 3B 4A 4B
1Y 2Y 3Y 4Y
Ā/B
4MUX2
PIN_D0_OUT
PIN_D1_OUT
PIN_D2_OUT
PIN_D3_OUT
FOX
GRACIE
JOSHUA
BUF_D3 BUF_D2 BUF_D1 BUF_D0
Nuts.
PIN_D4_OUT
PIN_D5_OUT
PIN_D6_OUT
PIN_D7_OUT
HABIB
Y match
AND_4
PIN_57
JERRY
Invert raster line # depending on screen flip
HELEN
HANS
HENRY
HARRY
FLORA
FRANK
FELIX
DOUG
PIN_V1
PIN_V2
PIN_V3
PIN_V4
PIN_V5
PIN_V6
PIN_V7
PIN_V8
XOR_2
HELIO
Adds 1 or -1 to Y pos depending on screen flip
FRIDA
FABIO2
CLK
D0 D1 D2 D3
Q0 Q1 Q2 Q3
4DFF
GARY
GERALD
FREYA
Catch sprite Y position byte from active list currently read
FRITZ
FABIO3
ACTIVE_D0 ACTIVE_D1 ACTIVE_D2 ACTIVE_D3
ELISE
HAROLD
ACTIVE_D4 ACTIVE_D5 ACTIVE_D6 ACTIVE_D7
GORDON
Sprite line # for rendering
Inverted internally
PIN_VFLP
BEN
BUCK
BILLY
BRUCE
AGNES
ABEL
ALICE
ALLEN
BUFFER
PIN_VLB0
PIN_VLB1
PIN_VLB2
PIN_VLB3
For 32 and 64 pixels high sprites ?
AIDEN
BLAKE
PIN_54
PIN_55
TITLE:
Capcom 86S105
Y POSITION
DATE:
09/01/2025
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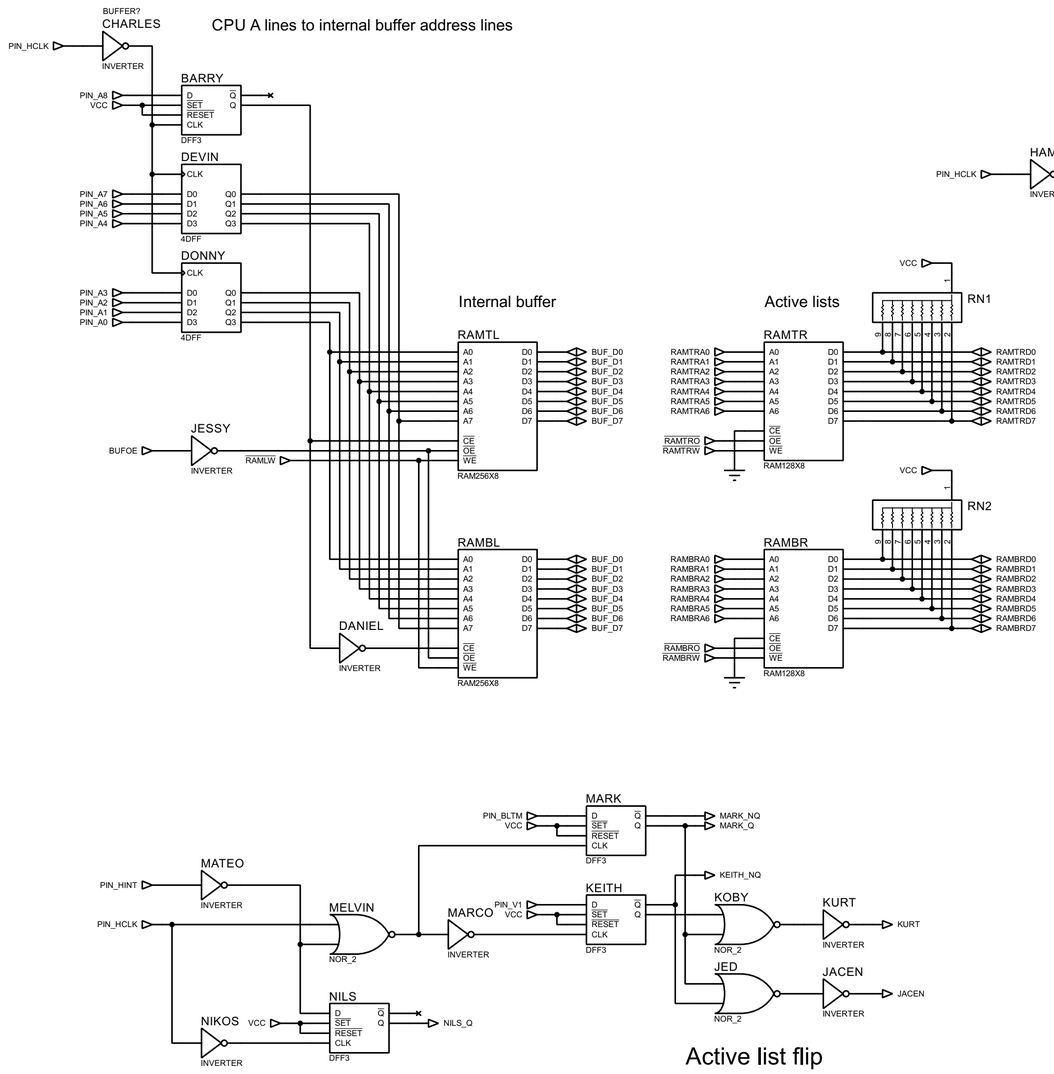
1/4
BY: Sean Gonsalves
REV: B

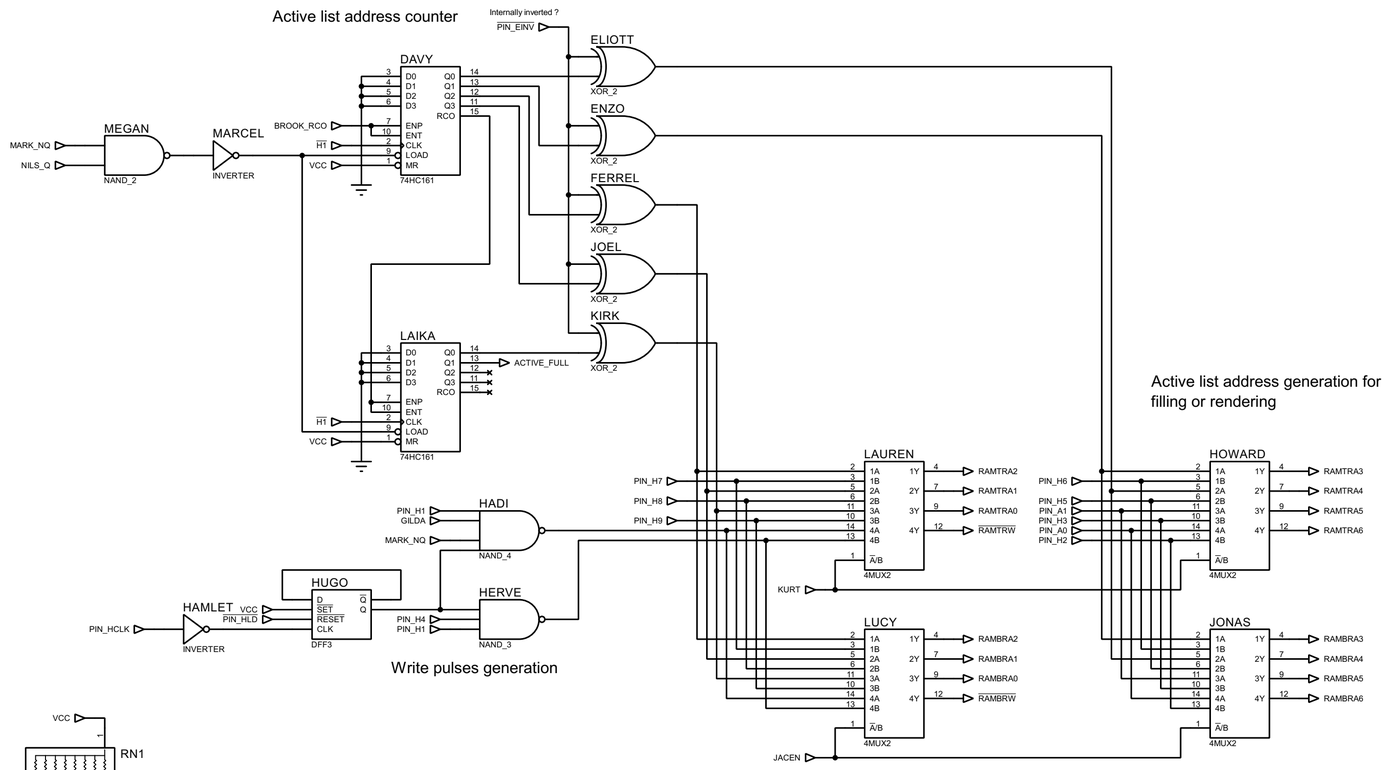
The internal buffer can hold 128 4-byte entries = 512 bytes
[0] is tile #
[1] is attributes (flags, palette...)
[2] is Y pos
[3] is X pos

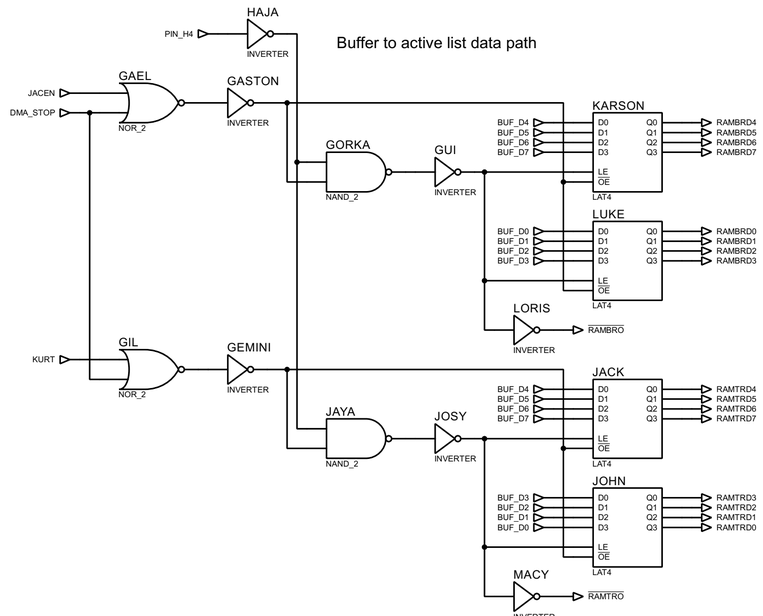
The two smaller RAM blocks are the active sprite lists
When one is used for rendering, the other is filled

This chip DMAs the main work RAM to its internal buffer once per frame, and does Y matching to build active sprite lists each scanline.

During rendering, the tile #, attributes and X pos bytes are output all at the same time (pipelines are used) for the external circuitry to fill the line buffers with the right pixels.







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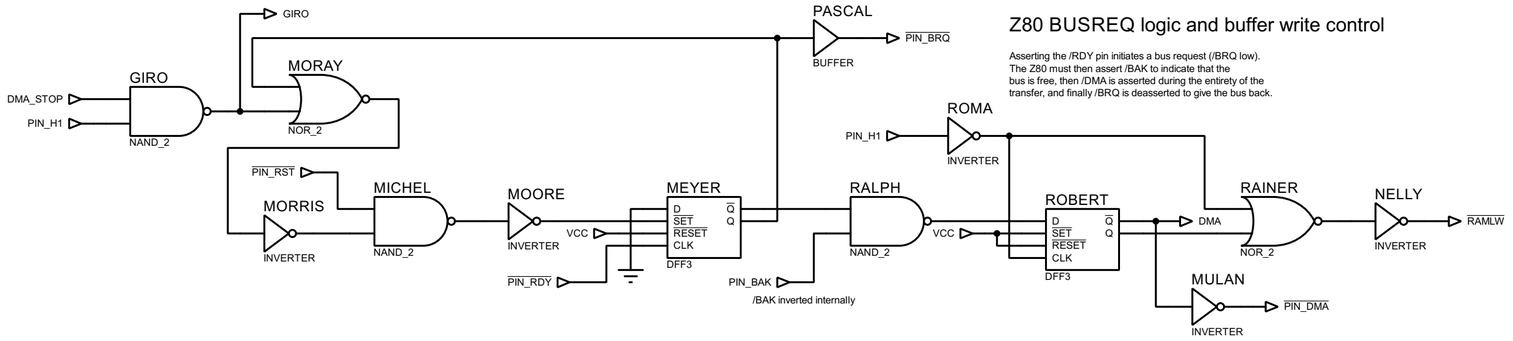
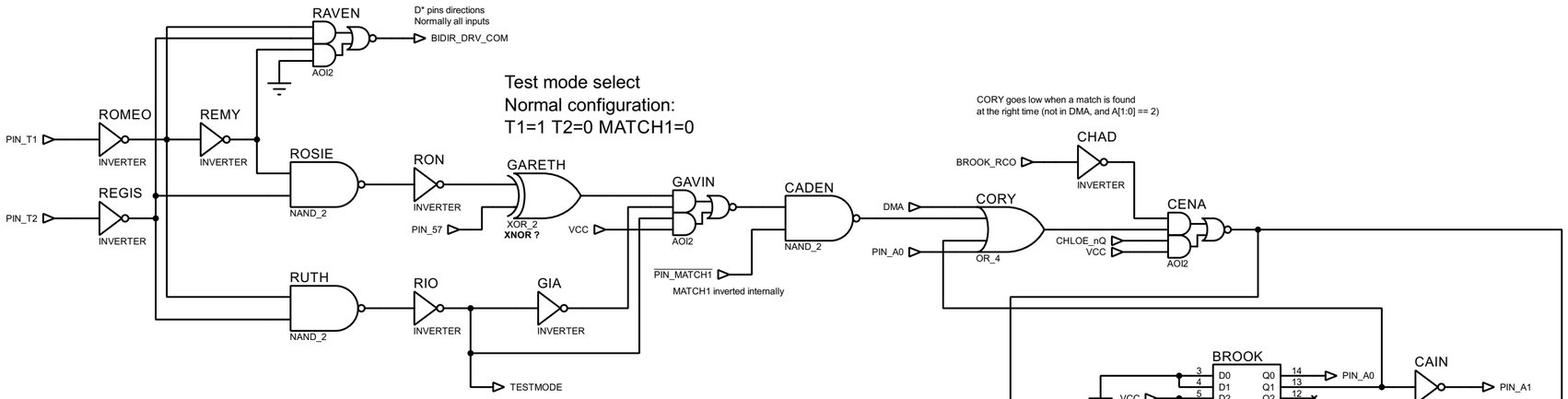
Z80 BUSREQ logic and buffer write control

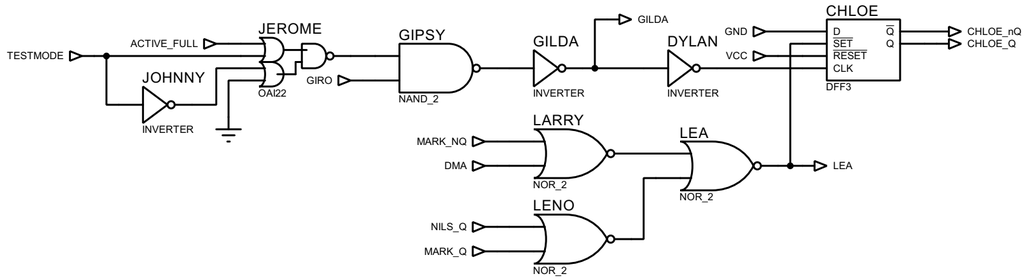
Asserting the /RDY pin initiates a bus request (/BRQ low).
The Z80 must then assert /BAK to indicate that the
bus is free, then /DMA is asserted during the entirety of the
transfer, and finally /BRQ is deasserted to give the bus back.



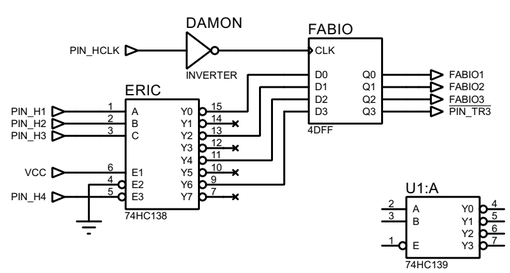
Test mode select
Normal configuration:
T1=1 T2=0 MATCH1=0



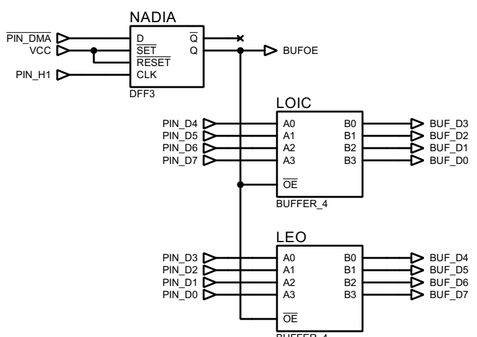
Buffer to active list copy sequencing



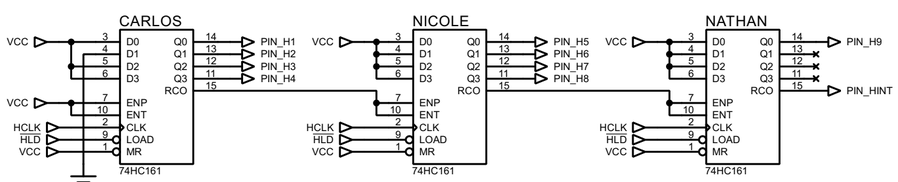
Final output sequencer



DMA Z80 data bus to internal buffer RAM



Internal horizontal counter



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Capcom 86S105 SEQUENCING	09/01/2025
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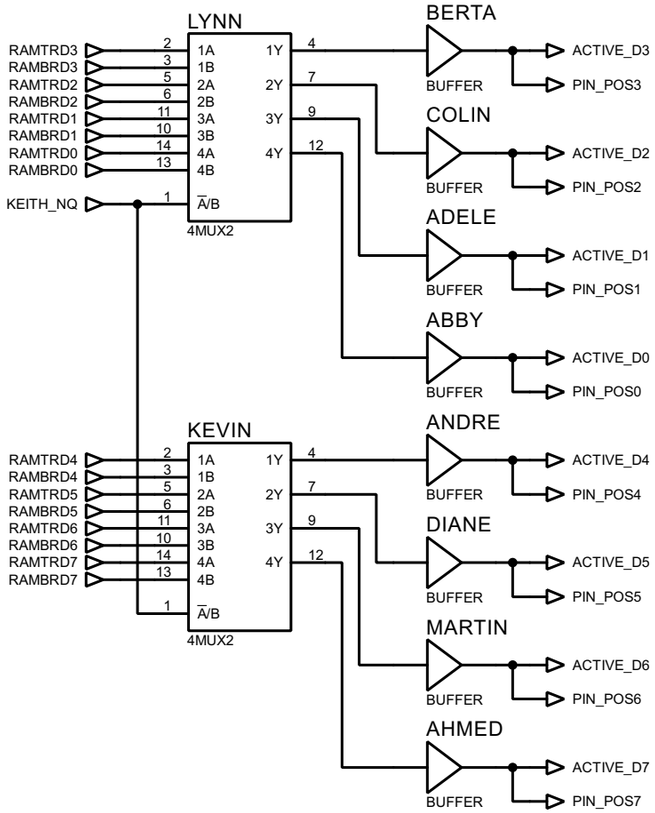
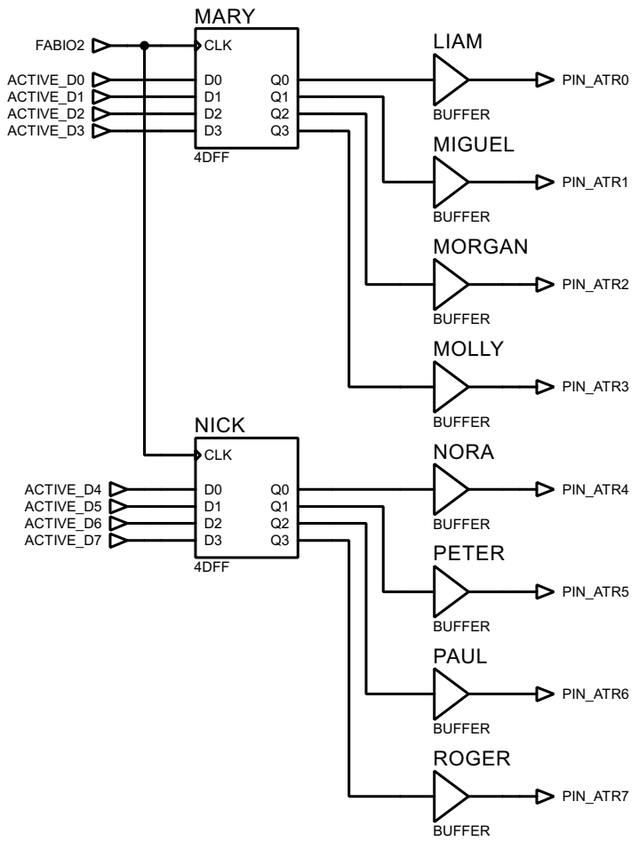
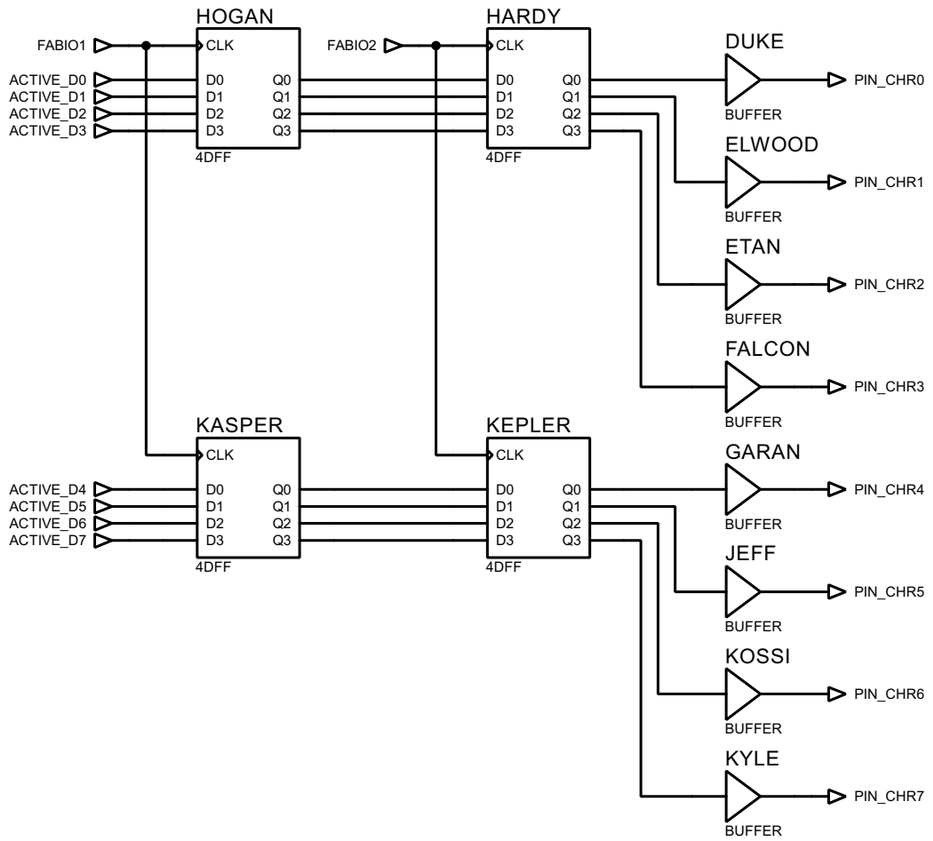
Active list selection for rendering
and x position byte output to POS pins



Active list attribute byte to ATR pins delay x1



Active list tile # byte to CHR pins delay x2



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