S45
CLK_BUF
BUF
CLK_BUF2

L14
INV

K13
CLK_BUF
INV

K12
INV

P31
RES
NAND_8

P30
AND_2

CYCLERES
AB86
INV
CYCLERES

PIN_NRES

R131
CLK
D
Q
Q
DFF

R130
NAND_2

R129
INV
RES

CLK_BUF

P37B
NAND_8

P37A
XNOR_2

P36
NAND_2

P35
CLK
D
Q
DFFN
CLKDIV384

VCC

P38A
NAND_6

P38B
XNOR_2

P39
NAND_2

P40
CLK
D
Q
DFFN
CLKDIV192

P32A
NAND_6

P32B
XNOR_2

P33
NAND_2

P34
CLK
D
Q
DFFN

VCC

M14
NAND_4

M13
XNOR_2

M12
NAND_2

M10
CLK
D
Q
DFFN

R41
NAND_3

R42
XNOR_2

R43
NAND_2

R44
CLK
D
Q
DFFN

R34B
NAND_2

R34A
XNOR_2

R33
NAND_2

R32
CLK
D
Q
DFFN
CLKDIV12

R47
XOR_2

R48
NAND_2

R49
CLK
D
Q
DFFN

R51
RES
XOR_2

R52
NAND_2

R53
CLK
D
Q
DFFN

Divide by 3

R50
NAND_2

S36
INV

R45
AND_3

R46
CLK
D
Q
DFFN

CLKDIV2D_2

CLKDIV32D
CLKDIV16D_2
CLKDIV8D_3
CLKDIV4D_3
D72 NAND_4
D71 CLK D Q Q DFF → TRIGA

CLKDIV32D_3
CLKDIV16D_3
CLKDIV8D_3
CLKDIV4D_5
D68 NAND_4
D67 CLK D Q Q DFF
D8 AND_2 → D8

CLKDIV32D
CLKDIV16D_2
CLKDIV8D_3
CLKDIV4D_5
D74 NAND_4
D73 CLK D Q Q DFF
D9 AND_2 → D9
→ TRIGJ

CLKDIV32D
CLKDIV16D_3
CLKDIV8D_3
CLKDIV4D_5
D75 NAND_4
D76 CLK D Q Q DFF → TRIGB

CLKDIV32D
CLKDIV16D_2
CLKDIV8D_3
CLKDIV4D_3
E63 NAND_4
E64 CLK D Q Q DFF → TRIGC

CLKDIV32D_3
CLKDIV16D_2
CLKDIV8D_3
CLKDIV4D_3
D60 NAND_4
D59 CLK D Q Q DFF → TRIGD

CLKDIV4D_5
CLKDIV8D_3
CLKDIV16D_2
CLKDIV32D_3
E50 NAND_4
E49 CLK D Q Q DFF → TRIGF

CLKDIV32D
CLKDIV16D_2
CLKDIV8D_3
CLKDIV4D_5
E59 NAND_4
E60 CLK D Q Q DFF → TRIGE

CLKDIV32D_3
CLKDIV4D_5
D69 AND_2
D70 CLK D Q Q DFF → TRIGG

CLKDIV4D_5
CLKDIV8D_3
CLKDIV16D_2
CLKDIV32D
E56 NAND_4
E55 AND_2
E54 CLK D Q Q DFF
CLKDIV4_BUF
F63 XOR_2 → TRIGH

CLKDIV8D_3
CLKDIV4D_3
CLKDIV16D_3
CLKDIV32D
E57 NAND_4

CLK_BUF
CLKDIV16D_4
CLKDIV32D_4
H58 A B X0 X1 X2 X3 DEC2
F118 NOR_2 → F118
J70 NOR_2 → J70
H57 NOR_2 → H57
H61B NOR_2
H61A NAND_4 → H61A
H61A 842 010

CLKDIV8D_2 H59 INV
CLKDIV4D_4 H63 INV H62 INV
CLKDIV2D_3 H60 INV

D96 INV
TRIGC
D87 INV D86 INV → TRIGC_BUF2
TRIGC D92 BUF D97 INV D93 INV D98 INV → TRIGC_BUF
A114 INV
TRIGB A115 INV A116 INV → TRIGB_BUF2
C93 INV
TRIGB C91 INV C90 INV → TRIGB_BUF

CLKDIV2D_2 N42 BUF
CLKDIV4D_2 N43 NAND_2 → N43
CLK_BUF N41 CLK D Q Q DFF → IRAM_INT
N44 INV N70 INV → IRAM_INT

A124 INV H57
CLKDIV8D_2
CLKDIV4D_4 A123 INV A118 INV
CLKDIV2D_3 A120 INV A121 INV
A117 842 010
A122 001
A119 000
A117 NAND_4
B98 BUF → B98
B99 BUF → B99
A122 NAND_4 B77 BUF → B77
A119 NAND_4 A117B BUF → A117B

CLKDIV8D_2 K47 INV K44 INV J70
CLKDIV4D_4 K45 INV K48 INV
CLKDIV2D_3 K46 INV J66 INV
K50 NAND_4 → K50
J64 NAND_4 → J64
J65 NAND_4 → J65 B74 BUF → B74
J62 NAND_4 K54 BUF K2 INV K1 INV
J63 NAND_4 J72 BUF → J72
K49 NAND_4 → K49
L9 INV → L9

84.2
K50 101
J64 010
J65 110
J62 100
J63 000
K49 001

CLKDIV8D_2 H98 INV F123 INV F118
CLKDIV4D_4 H99 INV J107 INV
CLKDIV2D_3 A126 INV N139 INV
N144 NAND_4 N147 BUF → N147
N145 NAND_4 → N145
N149 NAND_4 → N149
N146 NAND_4 → N146
N152 NAND_4 → N152
M93 NAND_4 → M93

84.2
N144 110
N145 010
N149 000
N146 100
N152 001
M93 101

TITLE: Konami 054539 TRIGGERS
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BY: Sean Gonsalves
REV: @REV

PIN_AB09
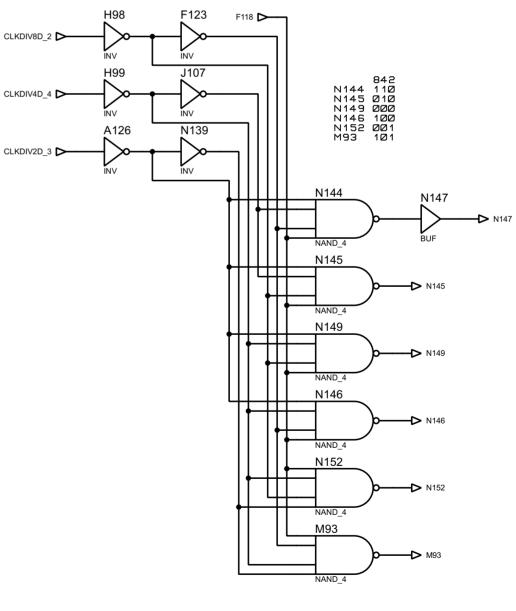
R7 INV
R10 INV

P13 INV

P14 BUF
IRAM_INT
P16 INV
P15 INV

P141 INV
PIN_AB00
P142 INV

P29 INV
P28 INV
PIN_AB00

P133 MUX21ND
RAM_A_DOUT
RAM_B_DOUT
A B S S̄ Z

P2 DFFNNQ
CLK D̄ Q

N2 MUX21ND
CH7_ACTIVE
PIN_RD07_IN
A B S S̄ Z

R9 MUX21ND
A B S S̄ Z
PIN_DB7_OUT

P132 MUX21ND
P3 DFFNNQ
N13 MUX21ND
CH6_ACTIVE
PIN_RD06_IN
R8 MUX21ND
PIN_DB6_OUT

P131 MUX21ND
P4 DFFNNQ
N12 MUX21ND
CH5_ACTIVE
PIN_RD05_IN
R12 MUX21ND
PIN_DB5_OUT

P130 MUX21ND
P5 DFFNNQ
N11 MUX21ND
CH4_ACTIVE
PIN_RD04_IN
R11 MUX21ND
PIN_DB4_OUT

P137 MUX21ND
P6 DFFNNQ
N17 MUX21ND
CH3_ACTIVE
PIN_RD03_IN
R16 MUX21ND
PIN_DB3_OUT

P136 MUX21ND
P9 DFFNNQ
N16 MUX21ND
CH2_ACTIVE
PIN_RD02_IN
R15 MUX21ND
PIN_DB2_OUT

P135 MUX21ND
P10 DFFNNQ
N15 MUX21ND
CH1_ACTIVE
PIN_RD01_IN
R14 MUX21ND
PIN_DB1_OUT

P134 MUX21ND
P11 DFFNNQ
N14 MUX21ND
CH0_ACTIVE
PIN_RD00_IN
R13 MUX21ND
PIN_DB0_OUT

RAM_A_DOUT / RAM_B_DOUT

R91 INV   PIN_DB7_IN_BUF → PIN_DB7_IN_INV
AC53 INV   PIN_DB7_IN_BUF → PIN_DB7_IN_INV2
J46 BUF   PIN_DB7_IN → PIN_DB7_IN_BUF

R95 INV   PIN_DB6_IN_BUF → PIN_DB6_IN_INV
AC54 INV   PIN_DB6_IN_BUF → PIN_DB6_IN_INV2
R3 BUF   PIN_DB6_IN → PIN_DB6_IN_BUF

R94 INV   PIN_DB5_IN_BUF → PIN_DB5_IN_INV
AC57 INV   PIN_DB5_IN_BUF → PIN_DB5_IN_INV2
S24 BUF   PIN_DB5_IN → PIN_DB5_IN_BUF

R93 INV   PIN_DB4_IN_BUF → PIN_DB4_IN_INV
AC56 INV   PIN_DB4_IN_BUF → PIN_DB4_IN_INV2
S23 BUF   PIN_DB4_IN → PIN_DB4_IN_BUF

R90 INV   PIN_DB3_IN_BUF → PIN_DB3_IN_INV
AC60 INV   PIN_DB3_IN_BUF → PIN_DB3_IN_INV2
S18 BUF   PIN_DB3_IN → PIN_DB3_IN_BUF

R92 INV   PIN_DB2_IN_BUF → PIN_DB2_IN_INV
AC55 INV   PIN_DB2_IN_BUF → PIN_DB2_IN_INV2
S22 BUF   PIN_DB2_IN → PIN_DB2_IN_BUF

R96 INV   PIN_DB1_IN_BUF → PIN_DB1_IN_INV
AC67 INV   PIN_DB1_IN_BUF → PIN_DB1_IN_INV2
S21 BUF   PIN_DB1_IN → PIN_DB1_IN_BUF

S88 INV   PIN_DB0_IN_BUF → PIN_DB0_IN_INV
AC61 INV   PIN_DB0_IN_BUF → PIN_DB0_IN_INV2
S9 BUF   PIN_DB0_IN → PIN_DB0_IN_BUF

P18 INV   PIN_DB5_IN_BUF → PIN_DB5_IN_INV3
R23 INV   PIN_DB4_IN_BUF → PIN_DB4_IN_INV3
P19 INV   PIN_DB2_IN_BUF → PIN_DB2_IN_INV3
V26 INV   PIN_DB0_IN_BUF → PIN_DB0_IN_INV3

S86 OR_2
PIN_NCS
PIN_NRD
→ PIN_DB_DIR

CLKDIV512T
A113 INV
A112 BUF

N82 BUF
CLKDIV16
P90 NAND_2
VCC
ROMA_A4
MUX_ACTIVE
P89B NAND_6

P85 BUF
CLKDIV8
ROMA_A4
ROMA_A3
P84B NAND_3
P89A OR_2
P88 NAND_2
CLK_BUF

P83 BUF
CLKDIV4
P84A NAND_2

ROMA_A5
P91 CLK D Q Q̄ DFF

Internal RAM write pulse gen
From internal source
REG22F_D7
P86 NOR_2

P87 CLK D Q Q̄ DFF

Internal RAM write pulse gen
From CPU access source
IRAM_INT

P72 CLK D Q̄ R̄ DFFR
VCC
CPU_WR_IRAM
N43
P67
P73 CLK_BUF
NOR_3
P74 CLK D Q̄ R̄ DFFR
N45 AND_2

N46 A B S Z MUX21N
M37
S8
N47 AOI
N48 INV
RAM_A_WR

Sub-clk pulse gen ?

PIN_AB00
P75A NOR_2
P75B A B S Z MUX21ND
P76 AOI
P77 INV
RAM_B_WR

R79 OR_2
PIN_AB09
PIN_NCS
PIN_NWR
R86 NOR_2
R84 OR_2
CPU_WR_IRAM
PIN_NRD
R85 NOR_2
CPU_IRAM
R83_NQ
R82 OR_2
PIN_WAIT

P59 A B X0 X1 X2 X3 DEC2
CLKDIV2D_3
CLKDIV4D_2
P60 NOR_2
P62 NOR_4
P66 OR_2
P67 AND_2
P67

P64 NOR_2
P61 A B X0 X1 X2 X3 DEC2
PIN_DTS1
PIN_DTS2

P65 NOR_2

P63 NOR_2

P69 D Q̄ SET RESET CLK DFFSR
CPU_IRAM
TESTREG2_D5
VCC
CLK_BUF

R83 D Q̄ Q̄ SET RESET CLK DFFSR
P67
CPU_IRAM
VCC
CLK_BUF
R83_NQ

R74 INV
R72 AND_2
CPU_REGS
PIN_DTAC

L13 INV
K10 INV K11 INV
CLK_BUF

N43
P70 INV
P55 INV
AA52 INV

Select between CPU or internal access

AA82 A B S S Z MUX21ND
ROMA_D0
PIN_AB01
AA79 BUF
AA83 CLK D Q DFFQ
AA54 INV
RAM_A0

Z45 A B S S Z MUX21ND
ROMA_D1
PIN_AB02
AA76 BUF
Z46 CLK D Q DFFQ
AA56 INV
RAM_A1

Z40 A B S S Z MUX21ND
ROMA_D2
PIN_AB03
AA73 BUF
Z41 CLK D Q DFFQ
AA57 INV
RAM_A2

Z42 A B S S Z MUX21ND
ROMA_D3
PIN_AB04
AA71 BUF
Z43 CLK D Q DFFQ
AA61 INV
RAM_A3

Z32 A B S S Z MUX21ND
ROMA_D4
PIN_AB05
AA66 BUF
Z31 CLK D Q DFFQ
AA51 INV
RAM_A4

Z33 A B S S Z MUX21ND
ROMA_D5
PIN_AB06
AA69 BUF
Z34 CLK D Q DFFQ
AA59 INV
RAM_A5

Z35 A B S S Z MUX21ND
ROMA_D6
PIN_AB07
AA68 BUF
Z36 CLK D Q DFFQ
AA62 INV
RAM_A6

RAMA
RAM_A_DIN0 D0 Q0 RAM_A_DOUT0
RAM_A_DIN1 D1 Q1 RAM_A_DOUT1
RAM_A_DIN2 D2 Q2 RAM_A_DOUT2
RAM_A_DIN3 D3 Q3 RAM_A_DOUT3
RAM_A_DIN4 D4 Q4 RAM_A_DOUT4
RAM_A_DIN5 D5 Q5 RAM_A_DOUT5
RAM_A_DIN6 D6 Q6 RAM_A_DOUT6
RAM_A_DIN7 D7 Q7 RAM_A_DOUT7
RAM_A0 A0
RAM_A1 A1
RAM_A2 A2
RAM_A3 A3
RAM_A4 A4
RAM_A5 A5
RAM_A6 A6
RAM_A_WR W̄Ē
RAM8_7

RAMB
RAM_B_DIN0 D0 Q0 RAM_B_DOUT0
RAM_B_DIN1 D1 Q1 RAM_B_DOUT1
RAM_B_DIN2 D2 Q2 RAM_B_DOUT2
RAM_B_DIN3 D3 Q3 RAM_B_DOUT3
RAM_B_DIN4 D4 Q4 RAM_B_DOUT4
RAM_B_DIN5 D5 Q5 RAM_B_DOUT5
RAM_B_DIN6 D6 Q6 RAM_B_DOUT6
RAM_B_DIN7 D7 Q7 RAM_B_DOUT7
RAM_B0 A0
RAM_B1 A1
RAM_B2 A2
RAM_B3 A3
RAM_B4 A4
RAM_B5 A5
RAM_B6 A6
RAM_B_WR W̄Ē
RAM8_7

TITLE:
Konami 054539
RAM A DATA
BY: Sean Gonsalves   REV: @REV
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CLKDIV2_BUF
N112 INV
T107 INV
CLKDIV8
T105 INV
T111 INV
CLKDIV4_BUF
T104 INV
T106 INV
S122
CLK_BUF3
IRAM_INT
H70
H69

MUXD15 ADDA15 ADDA39 BASE15
S148 MUX41N
S146 INV
S147 MUX21ND
N125 MUX21D
N129 DFFNNQ
PIN_DB7_IN_BUF
N121 MUX21D
RAM_A_DIN7
ADDA31
C96 LATCHN
ADDD14 TRIGB_BUF2
G91 MUX41N
D91 LATCHN ADDD30 TRIGC_BUF
G98 LATCHN ADDD14 TRIGC_BUF2
H82 LATCHN ADDD30 TRIGB_BUF

MUXD14 ADDA14 ADDA38 BASE14
S149 MUX41N
S151 INV
S150 MUX21ND
N117 MUX21D
N127 DFFNNQ
PIN_DB6_IN_BUF
N123 MUX21D
RAM_A_DIN6
ADDA30
C85 LATCHN ADDD13
E88 MUX41N
D82 LATCHN ADDD29
D81 LATCHN ADDD13
E84 LATCHN ADDD29

MUXD13 ADDA13 ADDA37 BASE13
S140 MUX41N
S142 INV
S141 MUX21ND
N115 MUX21D
N128 DFFNNQ
PIN_DB5_IN_BUF
N119 MUX21D
RAM_A_DIN5
ADDA29
C92 LATCHN ADDD12
G90 MUX41N
G93 LATCHN ADDD28
D90 LATCHN ADDD12
H81 LATCHN ADDD28

MUXD12 ADDA12 ADDA36 BASE12
S137 MUX41N
S139 INV
S138 MUX21ND
P108 MUX21D
P105 DFFNNQ
PIN_DB4_IN_BUF
N113 MUX21D
RAM_A_DIN4
ADDA28
C86 LATCHN ADDD11
G87 MUX41N
G89 LATCHN ADDD11
D83 LATCHN ADDD11
H66 LATCHN ADDD27

MUXD11 ADDA11 ADDA35 BASE11
T121 MUX41N
T123 INV
T122 MUX21ND
N104 MUX21D
N69 DFFNNQ
PIN_DB3_IN_BUF
N67 MUX21D
RAM_A_DIN3
ADDA27
ADDD10 TRIGB_BUF2
C84 LATCHN
E86 MUX41N
E80 LATCHN ADDD26 TRIGC_BUF
D80 LATCHN ADDD10 TRIGC_BUF2
E83 LATCHN ADDD26 TRIGB_BUF

MUXD10 ADDA10 ADDA34 BASE10
S145 MUX41N
S143 INV
S144 MUX21ND
N102 MUX21D
N66 DFFNNQ
PIN_DB2_IN_BUF
N64 MUX21D
RAM_A_DIN2
ADDA26
C81 LATCHN ADDD9
E75 MUX41N
E71 LATCHN ADDD25
D79 LATCHN ADDD9
E72 LATCHN ADDD25

MUXD9 ADDA9 ADDA33 BASE9
T108 MUX41N
T110 INV
T109 MUX21ND
N100 MUX21D
N55 DFFNNQ
PIN_DB1_IN_BUF
N56 MUX21D
RAM_A_DIN1
ADDA25
B90 LATCHN ADDD8
E87 MUX41N
E79 LATCHN ADDD24
D78 LATCHN ADDD8
E82 LATCHN ADDD24

MUXD8 ADDA8 ADDA32 BASE8
T112 MUX41N
T114 INV
T113 MUX21ND
P110 MUX21D
P106 DFFNNQ
PIN_DB0_IN_BUF
P113 MUX21D
RAM_A_DIN0
ADDA24
B89 LATCHN ADDD7
E89 MUX41N
E78 LATCHN ADDD23
D77 LATCHN ADDD7
E81 LATCHN ADDD23

TESTREG2_D0
RAM_A_DOUT7 PIN_RD07_IN
Z173 MUX21ND
Z172 INV
MUX_A_D7
RAM_A_DOUT6 PIN_RD06_IN
Z171 MUX21ND
Z170 INV
MUX_A_D6
RAM_A_DOUT5 PIN_RD05_IN
Z169 MUX21ND
Z168 INV
MUX_A_D5
RAM_A_DOUT4 PIN_RD04_IN
Z167 MUX21ND
Z166 INV
MUX_A_D4
RAM_A_DOUT3 PIN_RD03_IN
W129 MUX21ND
W128 INV
MUX_A_D3
RAM_A_DOUT2 PIN_RD02_IN
Z178 MUX21ND
Z179 INV
MUX_A_D2
RAM_A_DOUT1 PIN_RD01_IN
Z177 MUX21ND
Z176 INV
MUX_A_D1
RAM_A_DOUT0 PIN_RD00_IN
Z175 MUX21ND
Z174 INV
MUX_A_D0

Konami 054539
RAM B DATA
BY: Sean Gonsalves   REV: @REV   PAGE: 7/56   DATE: 10/11/2025

TESTREG1_D2
TESTREG2_D4
Y74 OR_2
Y93 INV
AA119 INV

TESTREG1_D0
T93 INV
T92 NAND_2
T89 INV
AA124 INV
T91 NAND_2
PIN_AXDA

TESTREG1_D3
TESTREG1_D1
Y100 OR_2
Y99 INV
X98 INV

W88 OR_2
W86 INV
X96 INV
TESTREG2_D2

T127
N77 INV
N74 INV

T130
N83 INV
N79 INV

T127 S109 INV S102 INV
T130 S121 INV S103 INV

L60 AND TESTREG1_D3 MULA_OUT23 N85 REG22E_D6 GND ADDB23 MUX41N N84 INV PIN_RA23
L59 AND MULA_OUT22 N86 REG22E_D5 GND ADDB22 MUX41N N87 INV PIN_RA22
K55 AND MULA_OUT21 N89 REG22E_D4 GND ADDB21 MUX41N N88 INV PIN_RA21
L80 AND MULA_OUT20 M62 REG22E_D3 GND ADDB20 MUX41N M61 INV PIN_RA20
L79 AND MULA_OUT19 M65 REG22E_D2 ADDB19 MUX41N M66 INV PIN_RA19
L78 AND MULA_OUT18 M63 REG22E_D1 GND ADDB18 MUX41N M64 INV PIN_RA18
L73 AND MULA_OUT17 M59 REG22E_D0 GND ADDB17 MUX41N M60 INV PIN_RA17
L72 AND MULA_OUT16 M52 ADDRCNT16 AG83 ADDB16 MUX41N M51 INV PIN_RA16

Y95 MUX41N MULA_OUT15 MULB_OUT15 AB185 MUXD15 Y94 INV
Y92 MUXE15 ROMB_D15 GND MUX41N Y91 INV
M53 ADDRCNT15 ACCC14 ADDB15 MUX41N M54 INV PIN_RA15

X77 MUX41N MULA_OUT14 MULB_OUT14 AB184 MUXD14 X78 INV
Y88 MUXE14 ROMB_D14 GND MUX41N Y87 INV
N80 ADDRCNT14 ACCC13 ADDB14 MUX41N N81 INV PIN_RA14

X81 MUX41N MULA_OUT13 MULB_OUT13 AB183 MUXD13 X82 INV
Y79 MUXE13 ROMB_D13 GND MUX41N Y80 INV
M57 ADDRCNT13 ACCC12 ADDB13 MUX41N M58 INV PIN_RA13

X79 MUX41N MULA_OUT12 MULB_OUT12 AB181 MUXD12 X80 INV
Y82 MUXE12 ROMB_D12 GND MUX41N Y81 INV
N75 ADDRCNT12 ACCC11 ADDB12 MUX41N N76 INV PIN_RA12

X89 MUX41N MULA_OUT11 MULB_OUT11 AB204 MUXD11 X88 INV
Y90 MUXE11 ROMB_D11 GND MUX41N Y89 INV
V87 ADDRCNT11 ACCC10 ADDB11 MUX41N V88 INV PIN_RA11

Y84 MUX41N MULA_OUT10 MULB_OUT10 AB188 MUXD10 Y83 INV
Y75 MUXE10 ROMB_D10 GND MUX41N Y76 INV
V79 ADDRCNT10 ACCC9 ADDB10 MUX41N V80 INV PIN_RA10

Y85 MUX41N MULA_OUT9 MULB_OUT9 AB202 MUXD9 Y86 INV
Y77 MUXE9 ROMB_D9 GND MUX41N Y78 INV
V81 ADDRCNT9 ACCC8 ADDB9 MUX41N V82 INV PIN_RA09

Z98 MUX41N MULA_OUT8 MULB_OUT8 AB187 MUXD8 Z97 INV
AA115 MUXE8 ROMB_D8 GND MUX41N AA116 INV
V85 ADDRCNT8 ACCC7 ADDB8 MUX41N V86 INV PIN_RA08

Z99 MUX41N MULA_OUT7 MULB_OUT7 AB193 MUXD7 Z100 INV
AA122 MUXE7 ROMB_D7 GND MUX41N AA123 INV
V89 ADDRCNT7 ACCC6 ADDB7 MUX41N V90 INV PIN_RA07

Z106 MUX41N MULA_OUT6 MULB_OUT6 AC148 MUXD6 Z105 INV
AA113 MUXE6 ROMB_D6 ROMA_D6 MUX41N AA114 INV
S107 ADDRCNT6 ACCC5 ADDB6 MUX41N S108 INV PIN_RA06

Z104 MUX41N MULA_OUT5 MULB_OUT5 AB189 MUXD5 Z103 INV
AA112 MUXE5 ROMB_D5 ROMA_D5 MUX41N AA111 INV
S104 ADDRCNT5 ACCC4 ADDB5 MUX41N S105 INV PIN_RA05

Z102 MUX41N MULA_OUT4 MULB_OUT4 AB191 MUXD4 Z101 INV
Z89 MUXE4 ROMB_D4 ROMA_D4 MUX41N Z90 INV
S110 ADDRCNT4 ACCC3 ADDB4 MUX41N S111 INV PIN_RA04

Z113 MUX41N MULA_OUT3 MULB_OUT3 AB206 MUXD3 Z114 INV
Z95 MUXE3 ROMB_D3 ROMA_D3 MUX41N Z96 INV
S115 ADDRCNT3 ACCC2 ADDB3 MUX41N S114 INV PIN_RA03

Z112 MUX41N MULA_OUT2 MULB_OUT2 AC152 MUXD2 Z111 INV
Z94 MUXE2 ROMB_D2 ROMA_D2 MUX41N Z93 INV
T83 ADDRCNT2 ACCC1 ADDB2 MUX41N T84 INV PIN_RA02

Z110 MUX41N MULA_OUT1 MULB_OUT1 AB205 MUXD1 Z109 INV
Z91 MUXE1 ROMB_D1 ROMA_D1 MUX41N Z92 INV
T87 ADDRCNT1 ACCC0 ADDB1 MUX41N T88 INV PIN_RA01

Z108 MUX41N MULA_OUT0 MULB_OUT0 AC149 MUXD0 Z107 INV
AA117 MUXE0 ROMB_D0 ROMA_D0 MUX41N AA118 INV
S113 ADDRCNT0 CLKDIV16D_5 ADDB0 MUX41N S112 INV PIN_RA00

M17
INV

M16
INV

M15
INV

CLKDIV8D_2

P56
TESTREG2_D2
MUX_ACTIVE
OR_2

M26
INV

M20
PIN_RD07_IN
CLK   Q
D
S
DFFSNNQ
RD_REG7

M21
PIN_RD06_IN
CLK   Q
D
S
DFFSNNQ
RD_REG6

M18
PIN_RD05_IN
CLK   Q
D
S
DFFSNNQ
RD_REG5

M25
PIN_RD04_IN
CLK   Q
D
S
DFFSNNQ
RD_REG4

M22
PIN_RD03_IN
CLK   Q
D
S
DFFSNNQ
RD_REG3

M23
PIN_RD02_IN
CLK   Q
D
S
DFFSNNQ
RD_REG2

M24
PIN_RD01_IN
CLK   Q
D
S
DFFSNNQ
RD_REG1

M27
PIN_RD00_IN
CLK   Q
D
S
DFFSNNQ
RD_REG0

G115

AS113
AS118   AS117
INV
INV   INV

AS116
AS115   AS114
INV
INV   INV

AR79
PIN_RD07_IN
CLK   Q
D
DFFNNQ
RD7_REG1

AS106
PIN_RD06_IN
CLK   Q
D
DFFNNQ
RD6_REG1

AS100
PIN_RD05_IN
CLK   Q
D
DFFNNQ
RD5_REG1

AR75
PIN_RD04_IN
CLK   Q
D
DFFNNQ
RD4_REG1

AS101
PIN_RD03_IN
CLK   Q
D
DFFNNQ
RD3_REG1

AS102
PIN_RD02_IN
CLK   Q
D
DFFNNQ
RD2_REG1

AS103
PIN_RD01_IN
CLK   Q
D
DFFNNQ
RD1_REG1

AS104
PIN_RD00_IN
CLK   Q
D
DFFNNQ
RD0_REG1

AR81
RD7_REG1
CLK   Q
D
DFFNNQ
RD7_REG2

AR82
RD6_REG1
CLK   Q
D
DFFNNQ
RD6_REG2

AR78
RD5_REG1
CLK   Q
D
DFFNNQ
RD5_REG2

AR80
RD4_REG1
CLK   Q
D
DFFNNQ
RD4_REG2

AP76
RD3_REG1
CLK   Q
D
DFFNNQ
RD3_REG2

AP74
RD2_REG1
CLK   Q
D
DFFNNQ
RD2_REG2

AP75
RD1_REG1
CLK   Q
D
DFFNNQ
RD1_REG2

AP77
RD0_REG1
CLK   Q
D
DFFNNQ
RD0_REG2

Registers 200~22F

PIN_AB09 — R76 INV
PIN_NCS — R75 NOR_2 — CPU_REGS

PIN_AB03 — S54 INV — S81 INV
PIN_AB04 — S69 INV — S74 INV
PIN_AB05 — S55 INV — S73 INV

PIN_NWR

S75 011xxx 18~1F NAND_4 — S90 NOR_2 — WR181F
S76 001xxx 08~0F NAND_4 — S84 NOR_2 — WR080F
S77 101xxx 28~2F NAND_4 — S77 V83 NOR_2 — WR282F
S78 000xxx 00~07 NAND_4 — S85 NOR_2 — WR0007
S79 100xxx 20~27 NAND_4 — S89 NOR_2 — WR2027
S80 010xxx 10~17 NAND_4 — S83 NOR_2 — WR1017

PIN_AB00 — W73 INV — W79 INV
PIN_AB01 — V84 INV — V92 INV
PIN_AB02 — W68 INV — W77 INV

WR282F

S77 — V94 INV

V91 101111 2F NAND_4 — WR22F
W81 101110 2E NAND_4 — WR22E
V95 101101 2D NAND_4 — ACCESS22D
W70 101011 2B NAND_4 — WR22B
W74 101010 2A NAND_4 — WR22A
W69 101001 29 NAND_4 — WR229
W75 101000 28 NAND_4 — WR228

PIN_AB00 — AA126 INV — AA138 INV
PIN_AB01 — AA127 INV — AA137 INV
PIN_AB02 — AA125 INV — AA136 INV

WR181F

AA133 011111 1F NAND_4 — WR21F
AA135 011110 1E NAND_4 — WR21E
AA132 011101 1D NAND_4 — WR21D
AA134 011100 1C NAND_4 — WR21C
AA129 011011 1B NAND_4 — WR21B
AA131 011010 1A NAND_4 — WR21A
AA128 011001 19 NAND_4 — WR219
AA130 011000 18 NAND_4 — WR218

PIN_AB00 — W82 INV — X73 INV
PIN_AB01 — W83 INV — X97 INV
PIN_AB02 — X95 INV — X101 INV

WR2027

X87 100111 27 NAND_4 — WR227
X91 100101 25 NAND_4 — WR225
X75 100100 24 NAND_4 — WR224
X93B 100011 23 NAND_4 — WR223
X74 100010 22 NAND_4 — WR222
X90 100001 21 NAND_4 — WR221
X76 100000 20 NAND_4 — WR220

PIN_AB00 — R77 INV — T55 INV
PIN_AB01 — R78 INV — S82 INV
PIN_AB02 — R81 INV — R80 INV

WR1017

T61 010111 17 NAND_4 — WR217
T56 010110 16 NAND_4 — WR216
T60 010101 15 NAND_4 — WR215
T54 010100 14 NAND_4 — WR214
T62 010011 13 NAND_4 — WR213
T58 010010 12 NAND_4 — WR212
T59 010001 11 NAND_4 — WR211
T57 010000 10 NAND_4 — WR210

PIN_AB00 — AA88 INV — AA78 INV
PIN_AB01 — AA81 INV — AA77 INV
PIN_AB02 — AA85 INV — AA75 INV

WR0007

AA55 000111 07 NAND_4 — WR207
AA72 000110 06 NAND_4 — WR206
AA60 000101 05 NAND_4 — WR205
AA70 000100 04 NAND_4 — WR204
AA58 000011 03 NAND_4 — WR203
AA67 000010 02 NAND_4 — WR202
AA63 000001 01 NAND_4 — WR201
AA65 000000 00 NAND_4 — WR200

PIN_AB00 — Z51 INV — Y49 INV
PIN_AB01 — AA53 INV — AA84 INV
PIN_AB02 — AA87 INV — AA86 INV

WR080F

Z49 001111 0F NAND_4 — WR20F
Y48 001110 0E NAND_4 — WR20E
Z37 001101 0D NAND_4 — WR20D
Y46A 001100 0C NAND_4 — WR20C
Y30 001011 0B NAND_4 — WR20B
Y47 001010 0A NAND_4 — WR20A
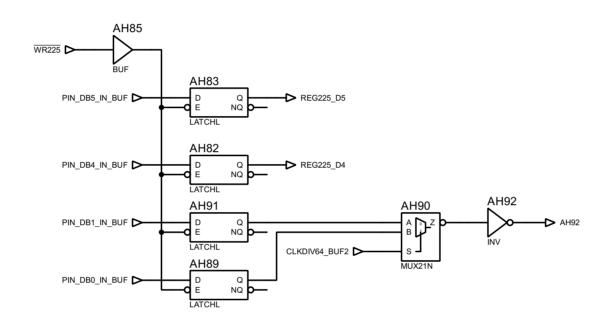W30 001001 09 NAND_4 — WR209
Y45 001000 08 NAND_4 — WR208

TITLE:
Konami 054539
REGS 200~20F EVEN
DATE:
10/11/2025
PAGE:
14/56
BY: Sean Gonsalves
REV: @REV

Schematic — REGS 200~20F EVEN register latches.

Column 1 (WR213 / WR212 / WR211 / WR210):

WR213 — T76 (INV), T73 (INV), T77 (INV)
- T68: D/E, NQ → REG213_D7 (PIN_DB7_IN_INV)
- T70: D/E, NQ → REG213_D6 (PIN_DB6_IN_INV)
- T78: D/E, NQ → REG213_D1 (PIN_DB1_IN_INV)
- T67: D/E, NQ → REG213_D0 (PIN_DB0_IN_INV)

WR212 — T63 (INV), T53 (INV), T64 (INV)
- V56: D/E, NQ → REG212_D7 (PIN_DB7_IN_INV)
- V60: D/E, NQ → REG212_D6 (PIN_DB6_IN_INV)
- V59: D/E, NQ → REG212_D1 (PIN_DB1_IN_INV)
- V58: D/E, NQ → REG212_D0 (PIN_DB0_IN_INV)

WR211 — V54 (INV), V57 (INV), V53 (INV)
- V55: D/E, NQ → REG211_D7 (PIN_DB7_IN_INV)
- V66: D/E, NQ → REG211_D6 (PIN_DB6_IN_INV)
- V76: D/E, NQ → REG211_D1 (PIN_DB1_IN_INV)
- V63: D/E, NQ → REG211_D0 (PIN_DB0_IN_INV)

WR210 — T74 (INV), T72 (INV), T75 (INV)
- T66: D/E, NQ → REG210_D7 (PIN_DB7_IN_INV)
- T69: D/E, NQ → REG210_D6 (PIN_DB6_IN_INV)
- T71: D/E, NQ → REG210_D1 (PIN_DB1_IN_INV)
- T65: D/E, NQ → REG210_D0 (PIN_DB0_IN_INV)

Column 2 (WR208 / WR200):

WR208 — V50 (INV), V52 (INV), V51 (INV)
- W41: D/E, NQ → REG208_D7 (PIN_DB7_IN_INV)
- V62: D/E, NQ → REG208_D6 (PIN_DB6_IN_INV)
- X66: D/E, NQ → REG208_D5 (PIN_DB5_IN_INV)
- Y67: D/E, NQ → REG208_D4 (PIN_DB4_IN_INV)
- Y66: D/E, NQ → REG208_D3 (PIN_DB3_IN_INV)
- X65: D/E, NQ → REG208_D2 (PIN_DB2_IN_INV)
- W52: D/E, NQ → REG208_D1 (PIN_DB1_IN_INV)
- V61: D/E, NQ → REG208_D0 (PIN_DB0_IN_INV)

WR200 — AA96 (INV), AA102 (INV), AA95 (INV)
- AA93: D/E, NQ → REG200_D7 (PIN_DB7_IN_INV)
- AA105: D/E, NQ → REG200_D6 (PIN_DB6_IN_INV)
- AA108: D/E, NQ → REG200_D5 (PIN_DB5_IN_INV)
- AA99: D/E, NQ → REG200_D4 (PIN_DB4_IN_INV)
- AA104: D/E, NQ → REG200_D3 (PIN_DB3_IN_INV)
- AA98: D/E, NQ → REG200_D2 (PIN_DB2_IN_INV)
- AA107: D/E, NQ → REG200_D1 (PIN_DB1_IN_INV)
- AA103: D/E, NQ → REG200_D0 (PIN_DB0_IN_INV)

Column 3 (WR20A / WR202):

WR20A — Y53 (INV), Y50 (INV), Y54 (INV)
- W42: D/E, NQ → REG20A_D7 (PIN_DB7_IN_INV)
- W54: D/E, NQ → REG20A_D6 (PIN_DB6_IN_INV)
- X64: D/E, NQ → REG20A_D5 (PIN_DB5_IN_INV)
- Y65: D/E, NQ → REG20A_D4 (PIN_DB4_IN_INV)
- Y64: D/E, NQ → REG20A_D3 (PIN_DB3_IN_INV)
- Y63: D/E, NQ → REG20A_D2 (PIN_DB2_IN_INV)
- W55: D/E, NQ → REG20A_D1 (PIN_DB1_IN_INV)
- X53: D/E, NQ → REG20A_D0 (PIN_DB0_IN_INV)

WR202 — Z61 (INV), S87 (INV), Z62 (INV)
- Z67: D/E, NQ → REG202_D7 (PIN_DB7_IN_INV)
- Z88: D/E, NQ → REG202_D6 (PIN_DB6_IN_INV)
- Z86: D/E, NQ → REG202_D5 (PIN_DB5_IN_INV)
- Z85: D/E, NQ → REG202_D4 (PIN_DB4_IN_INV)
- Z81: D/E, NQ → REG202_D3 (PIN_DB3_IN_INV)
- Z82: D/E, NQ → REG202_D2 (PIN_DB2_IN_INV)
- Z87: D/E, NQ → REG202_D1 (PIN_DB1_IN_INV)
- Z77: D/E, NQ → REG202_D0 (PIN_DB0_IN_INV)

Column 4 (WR20C / WR204):

WR20C — Z54 (INV), Z57 (INV), Z53 (INV)
- X50: D/E, NQ → REG20C_D7 (PIN_DB7_IN_INV)
- X68: D/E, NQ → REG20C_D6 (PIN_DB6_IN_INV)
- X67: D/E, NQ → REG20C_D5 (PIN_DB5_IN_INV)
- Y70: D/E, NQ → REG20C_D4 (PIN_DB4_IN_INV)
- Y69: D/E, NQ → REG20C_D3 (PIN_DB3_IN_INV)
- Y68: D/E, NQ → REG20C_D2 (PIN_DB2_IN_INV)
- X71: D/E, NQ → REG20C_D1 (PIN_DB1_IN_INV)
- X54: D/E, NQ → REG20C_D0 (PIN_DB0_IN_INV)

WR204 — S91 (INV), S93 (INV), S92 (INV)
- S95: D/E, NQ → REG204_D7 (PIN_DB7_IN_INV)
- S99: D/E, NQ → REG204_D6 (PIN_DB6_IN_INV)
- S101: D/E, NQ → REG204_D5 (PIN_DB5_IN_INV)
- S98: D/E, NQ → REG204_D4 (PIN_DB4_IN_INV)
- S96: D/E, NQ → REG204_D3 (PIN_DB3_IN_INV)
- S97: D/E, NQ → REG204_D2 (PIN_DB2_IN_INV)
- S100: D/E, NQ → REG204_D1 (PIN_DB1_IN_INV)
- S94: D/E, NQ → REG204_D0 (PIN_DB0_IN_INV)

Column 5 (WR20E / WR206):

WR20E — Z56 (INV), Z58 (INV), Z55 (INV)
- X51: D/E, NQ → REG20E_D7 (PIN_DB7_IN_INV)
- X70: D/E, NQ → REG20E_D6 (PIN_DB6_IN_INV)
- X69: D/E, NQ → REG20E_D5 (PIN_DB5_IN_INV)
- Y73: D/E, NQ → REG20E_D4 (PIN_DB4_IN_INV)
- Y72: D/E, NQ → REG20E_D3 (PIN_DB3_IN_INV)
- Y71: D/E, NQ → REG20E_D2 (PIN_DB2_IN_INV)
- X72: D/E, NQ → REG20E_D1 (PIN_DB1_IN_INV)
- X55: D/E, NQ → REG20E_D0 (PIN_DB0_IN_INV)

WR206 — AA89 (INV), AA91 (INV), AA90 (INV)
- AA94: D/E, NQ → REG206_D7 (PIN_DB7_IN_INV)
- AA106: D/E, NQ → REG206_D6 (PIN_DB6_IN_INV)
- AA110: D/E, NQ → REG206_D5 (PIN_DB5_IN_INV)
- AA101: D/E, NQ → REG206_D4 (PIN_DB4_IN_INV)
- AA97: D/E, NQ → REG206_D3 (PIN_DB3_IN_INV)
- AA100: D/E, NQ → REG206_D2 (PIN_DB2_IN_INV)
- AA109: D/E, NQ → REG206_D1 (PIN_DB1_IN_INV)
- AA92: D/E, NQ → REG206_D0 (PIN_DB0_IN_INV)

(All latches labeled LATCHN.)

AH85 BUF

WR225

V77 DFF4Q

WR22F — CLK
PIN_DB0_IN_BUF — D0   Q0 — REG22F_D0
PIN_DB1_IN_BUF — D1   Q1 — REG22F_D1
PIN_DB4_IN_BUF — D2   Q2 — REG22F_D4
PIN_DB5_IN_BUF — D3   Q3 — REG22F_D5

V78 LATCHR

PIN_DB7_IN_BUF — D   Q — REG22F_D7
WR22F — E   NQ
RES — R

AH83 LATCHL

PIN_DB5_IN_BUF — D   Q — REG225_D5
E   NQ

AH82 LATCHL

PIN_DB4_IN_BUF — D   Q — REG225_D4
E   NQ

AH91 LATCHL

PIN_DB1_IN_BUF — D   Q
E   NQ

AH90 MUX21N

A   Z
B
S

CLKDIV64_BUF2

AH89 LATCHL

PIN_DB0_IN_BUF — D   Q
E   NQ

AH92 INV — AH92

WR22E

T117 INV
T128 INV
T129 INV

T119 INV
PIN_DB7_IN_BUF

T118 LATCHN
D   NQ — REG22E_D7
E

M75 LATCHNN
PIN_DB6_IN_BUF — D   NQ — REG22E_D6
E

N98 LATCHNN
PIN_DB5_IN_BUF — D   NQ — REG22E_D5
E

N96 LATCHNN
PIN_DB4_IN_BUF — D   NQ — REG22E_D4
E

M73 LATCHNN
PIN_DB3_IN_BUF — D   NQ — REG22E_D3
E

M69 LATCHNN
PIN_DB2_IN_BUF — D   NQ — REG22E_D2
E

M67 LATCHNN
PIN_DB1_IN_BUF — D   NQ — REG22E_D1
E

M71 LATCHNN
PIN_DB0_IN_BUF — D   NQ — REG22E_D0
E

WR217

AB73 INV
AB75 INV
AB74 INV

AE52 LATCHN
PIN_DB7_IN_INV2 — D   NQ — REG217_D7
E

AE48 LATCHN
PIN_DB6_IN_INV2 — D   NQ — REG217_D6
E

AE41 LATCHN
PIN_DB5_IN_INV2 — D   NQ — REG217_D5
E

AE51 LATCHN
PIN_DB4_IN_INV2 — D   NQ — REG217_D4
E

AE50 LATCHN
PIN_DB3_IN_INV2 — D   NQ — REG217_D3
E

AE47 LATCHN
PIN_DB2_IN_INV2 — D   NQ — REG217_D2
E

AC64 LATCHN
PIN_DB1_IN_INV2 — D   NQ — REG217_D1
E

AC66 LATCHN
PIN_DB0_IN_INV2 — D   NQ — REG217_D0
E

REGISTERS 2

Block WR21F

AB61 INV — AB63 INV — AB62 INV — WR21F

Ref	Input	Output
AG44	PIN_DB7_IN_INV2	REG21F_D7
AH40	PIN_DB6_IN_INV2	REG21F_D6
AG43	PIN_DB5_IN_INV2	REG21F_D5
AG42	PIN_DB4_IN_INV2	REG21F_D4
AH38	PIN_DB3_IN_INV2	REG21F_D3
AG41	PIN_DB2_IN_INV2	REG21F_D2
AG40	PIN_DB1_IN_INV2	REG21F_D1
AF59	PIN_DB0_IN_INV2	REG21F_D0

(D / E / NQ / LATCHN)

Block WR21E

AB55 INV — AB57 INV — AB56 INV — WR21E

Ref	Input	Output
AC52	PIN_DB7_IN_INV2	REG21E_D7
AC58	PIN_DB6_IN_INV2	REG21E_D6
AC46	PIN_DB5_IN_INV2	REG21E_D5
AC49	PIN_DB4_IN_INV2	REG21E_D4
AC48	PIN_DB3_IN_INV2	REG21E_D3
AC47	PIN_DB2_IN_INV2	REG21E_D2
AC63	PIN_DB1_IN_INV2	REG21E_D1
AC65	PIN_DB0_IN_INV2	REG21E_D0

Block WR21D

AB58 INV — AB60 INV — AB59 INV — WR21D

Ref	Input	Output
AG39	PIN_DB7_IN_INV2	REG21D_D7
AH39	PIN_DB6_IN_INV2	REG21D_D6
AG38	PIN_DB5_IN_INV2	REG21D_D5
AG37	PIN_DB4_IN_INV2	REG21D_D4
AH51	PIN_DB3_IN_INV2	REG21D_D3
AG36	PIN_DB2_IN_INV2	REG21D_D2
AG35	PIN_DB1_IN_INV2	REG21D_D1
AF58	PIN_DB0_IN_INV2	REG21D_D0

Block WR221

AB118 INV — AB126 INV — AB125 INV — WR221

Ref	Input	Output
AH73	PIN_DB7_IN_INV2	REG221_D7
AH71	PIN_DB6_IN_INV2	REG221_D6
AE76	PIN_DB5_IN_INV2	REG221_D5
AD105	PIN_DB4_IN_INV2	REG221_D4
AD103	PIN_DB3_IN_INV2	REG221_D3
AD102	PIN_DB2_IN_INV2	REG221_D2
AD104	PIN_DB1_IN_INV2	REG221_D1
AC85	PIN_DB0_IN_INV2	REG221_D0

Block WR220

AB67 INV — AB69 INV — AB68 INV — WR220

Ref	Input	Output
AC51	PIN_DB7_IN_INV2	REG220_D7
AC50	PIN_DB6_IN_INV2	REG220_D6
AC62	PIN_DB5_IN_INV2	REG220_D5
AC59	PIN_DB4_IN_INV2	REG220_D4
AE49	PIN_DB3_IN_INV2	REG220_D3
AE46	PIN_DB2_IN_INV2	REG220_D2
AE59	PIN_DB1_IN_INV2	REG220_D1
AD63	PIN_DB0_IN_INV2	REG220_D0

Block WR21A

AB85 INV — AB82 INV — AB81 INV — WR21A

Ref	Input	Output
AD85	PIN_DB7_IN_INV2	REG21A_D7
AD84	PIN_DB6_IN_INV2	REG21A_D6
AD79	PIN_DB5_IN_INV2	REG21A_D5
AD70	PIN_DB4_IN_INV2	REG21A_D4
AC69	PIN_DB3_IN_INV2	REG21A_D3
AC68	PIN_DB2_IN_INV2	REG21A_D2
AC73	PIN_DB1_IN_INV2	REG21A_D1
AC72	PIN_DB0_IN_INV2	REG21A_D0

Block WR219

AB76 INV — AB78 INV — AB77 INV — WR219

Ref	Input	Output
AF53	PIN_DB7_IN_INV2	REG219_D7
AF51	PIN_DB6_IN_INV2	REG219_D6
AF55	PIN_DB5_IN_INV2	REG219_D5
AF54	PIN_DB4_IN_INV2	REG219_D4
AE58	PIN_DB3_IN_INV2	REG219_D3
AE64	PIN_DB2_IN_INV2	REG219_D2
AE65	PIN_DB1_IN_INV2	REG219_D1
AF56	PIN_DB0_IN_INV2	REG219_D0

Block WR218

AB70 INV — AB72 INV — AB71 INV — WR218

Ref	Input	Output
AG54	PIN_DB7_IN_INV2	REG218_D7
AH50	PIN_DB6_IN_INV2	REG218_D6
AG53	PIN_DB0_IN_INV2	REG218_D5
AG52	PIN_DB4_IN_INV2	REG218_D4
AH53	PIN_DB3_IN_INV2	REG218_D3
AG51	PIN_DB2_IN_INV2	REG218_D2
AG50	PIN_DB1_IN_INV2	REG218_D1
AF61	PIN_DB0_IN_INV2	REG218_D0

Block WR224

AB110 INV — AB115 INV — AB114 INV — WR224

Ref	Input	Output
AB112	PIN_DB6_IN_BUF	REG224_D6
AB92	PIN_DB5_IN_BUF	REG224_D5
AB97	PIN_DB4_IN_BUF	REG224_D4
AB108	PIN_DB3_IN_BUF	REG224_D3
AB106	PIN_DB2_IN_BUF	REG224_D2
AB93	PIN_DB1_IN_BUF	REG224_D1
AB95	PIN_DB0_IN_BUF	REG224_D0

(D / E / NQ / LATCHNN)

Block WR216

AB64 INV — AB65 INV — AB66 INV — WR216

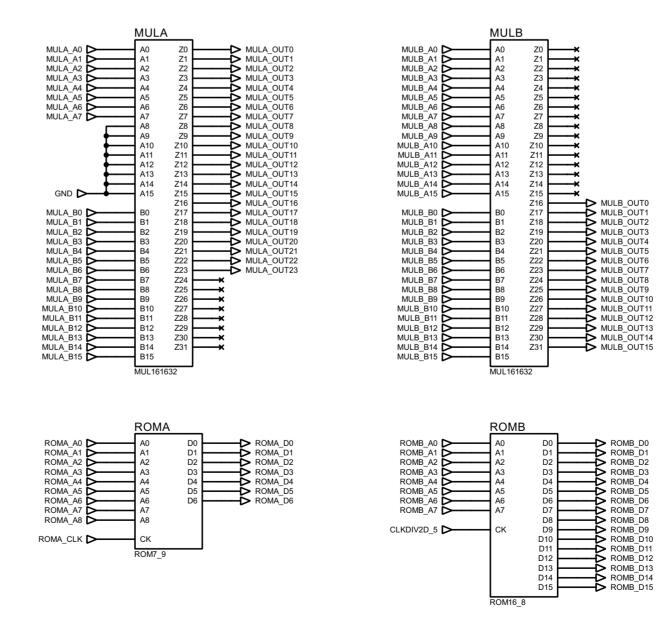| Ref	Input	Output
AG49	PIN_DB7_IN_INV2	REG216_D7
AG34	PIN_DB6_IN_INV2	REG216_D6
AG48	PIN_DB5_IN_INV2	REG216_D5
AG47	PIN_DB4_IN_INV2	REG216_D4
AH52	PIN_DB3_IN_INV2	REG216_D3
AG46	PIN_DB2_IN_INV2	REG216_D2
AG45	PIN_DB1_IN_INV2	REG216_D1
AF60	PIN_DB0_IN_INV2	REG216_D0

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Channel volume
and
Reverb volume ?

External memory
address up-counter
for CPU access

K50

B69 BUF
B56 INV
B58 INV
B55 INV
C64 INV
C61 INV
C62 INV
B72 BUF

TESTREG1_D3
A106 INV
A96 INV

TRIGE
C71 INV
B73 INV

MUX_A_D7   C76 D E NQ LATCHN
MUX_B_D7   B83 D E NQ LATCHN
B76 A B Z S SO MUX21ND   PIN_RD07_IN
A84 A B Z SO MUX21D   MULA_A7

MUX_A_D6   C75 D E NQ LATCHN
MUX_B_D6   B65 D E NQ LATCHN
B68 A B Z S S MUX21ND   PIN_RD06_IN
A82 A B Z S MUX21D   MULA_A6

MUX_A_D5   C74 D E NQ LATCHN
MUX_B_D5   B59 D E NQ LATCHN
B67 A B Z S S MUX21ND   PIN_RD05_IN
A80 A B Z S MUX21D   MULA_A5

MUX_A_D4   C73 D E NQ LATCHN
MUX_B_D4   B61 D E NQ LATCHN
B66 A B Z S S MUX21ND   PIN_RD04_IN
A78 A B Z S MUX21D   MULA_A4

MUX_A_D3   C70 D E NQ LATCHN
MUX_B_D3   B64 D E NQ LATCHN
B75 A B Z S S MUX21ND   PIN_RD03_IN
A94 A B Z S MUX21D   MULA_A3

MUX_A_D2   B60 D E NQ LATCHN
MUX_B_D2   B80 D E NQ LATCHN
B71 A B Z S SO MUX21ND   PIN_RD02_IN
A90 A B Z SO MUX21D   MULA_A2

MUX_A_D1   B62 D E NQ LATCHN
MUX_B_D1   B79 D E NQ LATCHN
B70 A B Z S S MUX21ND   PIN_RD01_IN
A88 A B Z S MUX21D   MULA_A1

MUX_A_D0   B81 D E NQ LATCHN
MUX_B_D0   B82 D E NQ LATCHN
B78 A B Z S S MUX21ND   PIN_RD00_IN
A86 A B Z S MUX21D   MULA_A0

AJ130
AR39 INV
AP21 INV   AP22 INV
AR40 INV
AP24 INV   AP23 INV

J64
AJ63 INV   AJ64 INV
AJ62 INV

MUX_B_D7   AJ81 D E NQ LATCHNN
AP40 CLK D Q Q̄ DFFNNQ   AP40
MUX_B_D6   AJ73 D E NQ LATCHNN
AP20 CLK D Q Q̄ DFFNNQ   AP20
MUX_B_D5   AJ69 D E NQ LATCHNN
AN28 CLK D Q Q̄ DFFNNQ   AN28
MUX_B_D4   AJ67 D E NQ LATCHNN
AN27 CLK D Q Q̄ DFFNNQ   AN27
MUX_B_D3   AJ79 D E NQ LATCHNN
AP39 CLK D Q Q̄ DFFNNQ   AP39
MUX_B_D2   AJ71 D E NQ LATCHNN
AP26 CLK D Q Q̄ DFFNNQ   AP26
MUX_B_D1   AJ65 D E NQ LATCHNN
AN26 CLK D Q Q̄ DFFNNQ   AN26
MUX_B_D0   AJ77 D E NQ LATCHNN
AP25 CLK D Q Q̄ DFFNNQ   AP25

CLKDIV2D_2   AB90 BUF   AB91 INV

AJ106 CLK D Q Q̄ DFF   AJ106
AB167

AF44 CLK D Q Q̄ DFF   SRA11
AF49 CLK D Q Q̄ DFF   SRA10
AF50 CLK D Q Q̄ DFF   SRA9
AJ1 CLK D Q Q̄ DFF   SRA8
AJ2 CLK D Q Q̄ DFF
AJ105 CLK D Q Q̄ DFF   SRA6
AH112 CLK D Q Q̄ DFF   SRA5
AH113 CLK D Q Q̄ DFF   SRA4
AH114 CLK D Q Q̄ DFF   SRA3
AH115 CLK D Q Q̄ DFF
AK77 CLK D Q Q̄ DFF   SRA1
AK76 CLK D Q Q̄ DFF   SRA0
AJ117 INV
AJ114 CLK D Q Q̄ DFF   AJ114
AB167 CLK D Q Q̄ DFF   AB167

CLKDIV4   AB128 BUF
CLKDIV8   AB124 BUF
CLKDIV16   AB164 BUF
CLKDIV32   AB163 BUF
AB166 NAND_4
CLKDIV4_BUF
CLKDIV8_BUF

REG22F_D4
N78 BUF
ACCESS22D   T96 INV
CLKDIV2D_3   N71 INV
TESTREG2_D3

T95 A B S Z MUX21N
T94 CLK D Q Q̄ DFFR   ADDRCNT0
T90 CLK D Q Q̄ R DFFR   ADDRCNT1
T85 CLK D Q Q̄ R DFFR   ADDRCNT2
T86 CLK D Q Q̄ R DFFR   ADDRCNT3

S116 A B S Z MUX21N
S117 CLK D Q Q̄ DFFR   ADDRCNT4
S118 CLK D Q Q̄ DFFR   ADDRCNT5
S119 CLK D Q Q̄ DFFR   ADDRCNT6
S120 CLK D Q Q̄ R DFFR   ADDRCNT7

R111 A B S Z MUX21N
R112 CLK D Q Q̄ R DFFR   ADDRCNT8
P80 CLK D Q Q̄ DFFR   ADDRCNT9
P79 CLK D Q Q̄ DFFR   ADDRCNT10
P78 CLK D Q Q̄ DFFR   ADDRCNT11

N73 A B S Z MUX21N
N72 CLK D Q Q̄ R DFFR   ADDRCNT12
M55 CLK D Q Q̄ DFFR   ADDRCNT13
M56 CLK D Q Q̄ DFFR   ADDRCNT14
M50 CLK D Q Q̄ R DFFR   ADDRCNT15
M49 CLK D Q Q̄ R DFFR   ADDRCNT16

CLKDIV8D_3
CLKDIV16D_3
F70 NOR_2
CLKDIV32D
F69 OR_2
CLKDIV4D_5
F68 CLK D Q Q̄ DFF
F67 BUF
CLKDIV2D_2
F66 CLK D Q Q̄ DFF   F66
F3 INV   F3
F42 INV
CLKDIV16D_3
F74 BUF
F73 CLK D Q Q̄ DFF
F72 BUF
F71 CLK D Q Q̄ DFF   F71
F17 INV   F17
F45 INV

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TESTEN

Y107
INV

T127
NAND_2
T127

T120
INV

REG22F_D4

CLKDIV512D_3

T131
NAND_2

T130
NAND_2
T130

CLKDIV4D_5
CLKDIV16D_3

D66
AND_2

CLKDIV32D

D65
AND_2

CLKDIV2D_2

D64
AND_2

D62
CLK D Q Q
DFF

B17
INV
B17

A16
INV

CLKDIV4D_5
CLKDIV32D_3

D63
AND_2

TRIGA
TRIGJ

D11
NAND_2

D10
BUF
D10

D12A
OR_2
D12A

TRIGF

D12B
INV

D14
BUF
D14

MULA

A0	Z0	MULA_OUT0
MULA_A0 A0	Z0	MULA_OUT0
MULA_A1 A1	Z1	MULA_OUT1
MULA_A2 A2	Z2	MULA_OUT2
MULA_A3 A3	Z3	MULA_OUT3
MULA_A4 A4	Z4	MULA_OUT4
MULA_A5 A5	Z5	MULA_OUT5
MULA_A6 A6	Z6	MULA_OUT6
MULA_A7 A7	Z7	MULA_OUT7
A8	Z8	MULA_OUT8
A9	Z9	MULA_OUT9
A10	Z10	MULA_OUT10
A11	Z11	MULA_OUT11
A12	Z12	MULA_OUT12
A13	Z13	MULA_OUT13
A14	Z14	MULA_OUT14
GND A15	Z15	MULA_OUT15
	Z16	MULA_OUT16
MULA_B0 B0	Z17	MULA_OUT17
MULA_B1 B1	Z18	MULA_OUT18
MULA_B2 B2	Z19	MULA_OUT19
MULA_B3 B3	Z20	MULA_OUT20
MULA_B4 B4	Z21	MULA_OUT21
MULA_B5 B5	Z22	MULA_OUT22
MULA_B6 B6	Z23	MULA_OUT23
MULA_B7 B7	Z24	
MULA_B8 B8	Z25	
MULA_B9 B9	Z26	
MULA_B10 B10	Z27	
MULA_B11 B11	Z28	
MULA_B12 B12	Z29	
MULA_B13 B13	Z30	
MULA_B14 B14	Z31	
MULA_B15 B15		

MUL161632

MULB

MULB_A0 A0	Z0	
MULB_A1 A1	Z1	
MULB_A2 A2	Z2	
MULB_A3 A3	Z3	
MULB_A4 A4	Z4	
MULB_A5 A5	Z5	
MULB_A6 A6	Z6	
MULB_A7 A7	Z7	
MULB_A8 A8	Z8	
MULB_A9 A9	Z9	
MULB_A10 A10	Z10	
MULB_A11 A11	Z11	
MULB_A12 A12	Z12	
MULB_A13 A13	Z13	
MULB_A14 A14	Z14	
MULB_A15 A15	Z15	
	Z16	MULB_OUT0
MULB_B0 B0	Z17	MULB_OUT1
MULB_B1 B1	Z18	MULB_OUT2
MULB_B2 B2	Z19	MULB_OUT3
MULB_B3 B3	Z20	MULB_OUT4
MULB_B4 B4	Z21	MULB_OUT5
MULB_B5 B5	Z22	MULB_OUT6
MULB_B6 B6	Z23	MULB_OUT7
MULB_B7 B7	Z24	MULB_OUT8
MULB_B8 B8	Z25	MULB_OUT9
MULB_B9 B9	Z26	MULB_OUT10
MULB_B10 B10	Z27	MULB_OUT11
MULB_B11 B11	Z28	MULB_OUT12
MULB_B12 B12	Z29	MULB_OUT13
MULB_B13 B13	Z30	MULB_OUT14
MULB_B14 B14	Z31	MULB_OUT15
MULB_B15 B15		

MUL161632

ROMA

ROMA_A0 A0	D0	ROMA_D0
ROMA_A1 A1	D1	ROMA_D1
ROMA_A2 A2	D2	ROMA_D2
ROMA_A3 A3	D3	ROMA_D3
ROMA_A4 A4	D4	ROMA_D4
ROMA_A5 A5	D5	ROMA_D5
ROMA_A6 A6	D6	ROMA_D6
ROMA_A7 A7		
ROMA_A8 A8		
ROMA_CLK CK		

ROM7_9

ROMB

ROMB_A0 A0	D0	ROMB_D0
ROMB_A1 A1	D1	ROMB_D1
ROMB_A2 A2	D2	ROMB_D2
ROMB_A3 A3	D3	ROMB_D3
ROMB_A4 A4	D4	ROMB_D4
ROMB_A5 A5	D5	ROMB_D5
ROMB_A6 A6	D6	ROMB_D6
ROMB_A7 A7	D7	ROMB_D7
	D8	ROMB_D8
	D9	ROMB_D9
CLKDIV2D_5 CK	D10	ROMB_D10
	D11	ROMB_D11
	D12	ROMB_D12
	D13	ROMB_D13
	D14	ROMB_D14
	D15	ROMB_D15

ROM16_8

G99
PIN_AXXA
PIN_AXDA
CLK
D
Q
Q̄
DFF

F102
BUF
AXDA_SYNC

D120 INV
D123 INV
D124 INV
PIN_AXXA

C131 INV
C130 INV
PIN_YMD

PIN_AXWA

PIN_ALRA

C127B INV

C127A AND_2

B128
A
B
Z
S
S̄
MUX21D

A139
CLK
D
Q
Q̄
DFF

CLK_BUF
E110
CLK
D
Q
Q̄
DFF
E110

B130
A
B
Z
S
S̄
MUX21D

B132
CLK
D
Q
Q̄
DFF

J108 INV
J108

C126 AND_2

C128
A
B
Z
S
S̄
MUX21D

D121
CLK
D
Q
Q̄
DFF

D122 INV
D122

CLKDIV8_BUF
H80 INV

H69 NOR_2

E73 INV
H69

CLKDIV4_BUF

H70 NOR_2

E74 INV
H70

CLKDIV2_BUF

L89 INV
L83 INV
L82 INV
CLK_BUF
CLK_BUF3

ROMA_A1
ROMA_A2
T97A OR_2

T97B AND_2
ROMA_A3

T98 INV
S122 INV
S122

AA121 INV
AB103A

AA120 NOR_2
AB79

CLKDIV128D_3
CLKDIV512D
CLKDIV64D
AH107 OR_4

SRA0

AH108 OR_2
AH108

CLKDIV128D_4
AH103 OR_4

AH104 OR_2
AH104

W87 BUF
CLKDIV128_BUF

W90 AND_2
REG224_D3

REG22F_D4

CLKDIV16D_4

W91 NOR_4
PIN_DLY

W92
CLK
D
R
Q
Q̄
DFFR
RES
CLKDIV512D3

W93 OR_2
W93

AUX DATA LATCHES schematic — Konami 054539

CLKDIV256D_3

S50
INV

Z27
INV

CLKDIV128D_3

AA44
INV

AA43
INV

CLKDIV64D_3

AA74
INV

Z47
INV

REG207_D0
T18_NQ
T11
NAND_2

REG205_D0
R35_NQ
S40
NAND_2

REG203_D0
AA25_NQ
AA35
NAND_2

REG201_D0
W15_NQ
W18
NAND_2

Z28
D0
D1
D2
D3
Z
S0
S1
MUX41N

Z29
A
B
Z
MUX21ND

LOOPFLAG

REG20F_D0
Y38_NQ
Z50
NAND_2

Z30
D0
D1
D2
D3
Z
S0
S1
MUX41N

REG20D_D0
Y37_NQ
Z44
NAND_2

REG20B_D0
S34_NQ
S46
NAND_2

REG209_D0
N4_NQ
S44
NAND_2

CLKDIV256D_3
P27
INV
P24
INV

CLKDIV128D_3
P26
INV
P20
INV

CLKDIV64D_3
P41
INV
P25
INV

CH3_ACTIVE
CH2_ACTIVE
CH1_ACTIVE
CH0_ACTIVE
P23
D0
D1
D2
D3
Z
S0
S1
MUX41N

P22
A
B
Z
S
S
MUX21ND

MUX_ACTIVE

CH7_ACTIVE
CH6_ACTIVE
CH5_ACTIVE
CH4_ACTIVE
P21
D0
D1
D2
D3
Z
S0
S1
MUX41N

PIN_RRMD
V133
INV
PIN_RRMD

CLKDIV256D_3
T23
INV
T30
INV

CLKDIV128D_3
V31
INV
V32
INV

CLKDIV64D_3
V25
INV
T24
INV

Y23_Q
T35_Q
Y20_Q
W26_Q
T31
D0
D1
D2
D3
Z
S0
S1
MUX41N

T32
A
B
Z
S
S
MUX21ND

R88
INV
R88

V20_Q
Z24_Q
X16_Q
Z16_Q
T33
D0
D1
D2
D3
Z
S0
S1
MUX41N

AB111
CLKDIV128_BUF2
BUF

AB101
AB102

XOR_2
OR_2

PIN_ADDA
TESTREG1_D6

AJ57
A
B
Z
S
Q/Q
MUX21D

Y110
AJ57

B104   B105   R87
CLKDIV512T   INV   INV   BUF   ROMA_A8

L101   L100   R98
CLKDIV256   INV   INV   BUF   ROMA_A7

CLKDIV128_BUF

L87   L86   R99
CLKDIV128   INV   INV   BUF   ROMA_A6

L96   L97   CLKDIV64_BUF   L90
CLKDIV64   INV   INV   BUF   ROMA_A5

L85   L84   CLKDIV32_BUF   P82
CLKDIV32   INV   INV   BUF   ROMA_A4

L99   L98   CLKDIV16_BUF   P81
CLKDIV16   INV   INV   BUF   ROMA_A3

L109   L110   CLKDIV8_BUF   T82
CLKDIV8   INV   INV   BUF   ROMA_A2

H75   H76   CLKDIV4_BUF   V98
CLKDIV4   INV   INV   BUF   ROMA_A1

H79   H78   CLKDIV2_BUF   M35
CLKDIV2   INV   INV   BUF   ROMA_A0

CLKDIV64_BUF
PIN_USE2

AJ59
A
B
Z
S
Q/Q
MUX21D

L92
CLKDIV128   INV

PIN_RRMD

AJ55
A
B
Z
S
Q/Q
MUX21D

AJ92
A
B
X0
X1
X2
X3
DEC2

AJ91
OR_3

AJ93
OR_3

AJ94
AND_2
AJ94

ADDER B - SAMPLE ADDRESS

Left column adders (FA1):

Ref	Inputs	Output
V106	OFFS11, BASE11	ADDB11
V107	OFFS10, BASE10	ADDB10
V108	OFFS9, BASE9	ADDB9
V109	OFFS8, BASE8	ADDB8
V110	OFFS7, BASE7	ADDB7
R105	OFFS6, BASE6	ADDB6
R106	OFFS5, BASE5	ADDB5
R107	OFFS4, BASE4	ADDB4
R108	OFFS3, BASE3	ADDB3
R109	OFFS2, BASE2	ADDB2
R110	OFFS1, BASE1	ADDB1
R104	OFFS0, BASE0, REVERSE	ADDB0

Second column adders (FA1):

Ref	Inputs	Output
R115	OFFS23, BASE23	ADDB23
R116	OFFS22, BASE22	ADDB22
R117	OFFS21, BASE21	ADDB21
R118	OFFS20, BASE20	ADDB20
R119	OFFS19, BASE19	ADDB19
M82	OFFS18, BASE18	ADDB18
M81	OFFS17, BASE17	ADDB17
M80	OFFS16, BASE16	ADDB16
M79	OFFS15, BASE15	ADDB15
M78	OFFS14, BASE14	ADDB14
M77	OFFS13, BASE13	ADDB13
V105	OFFS12, BASE12	ADDB12

Clock / logic section:

- $\overline{\text{CLKDIV32D\_2}}$ → L1 (INV) → L2 (INV)
- CLKDIV192 → H6 (CLK/D, DFF)
- H5 (DFF), H4 (DFF)
- CLKDIV32D_2 → L4 (INV) → L3 (INV)
- CLKDIV384 → H3 (DFF)
- H2 (DFF)
- PIN_DTCK
- H1 (DFF)
- P1 (DFF) → PIN_WDCK
- S1 (DFF) → PIN_ADDA → AH66 (NAND_2) → AH66
- S7 (DFF)
- S3 (A, B, Z — MUX21N), PIN_ADDA → PIN_LRCK
- S4 (DFF)
- S2 (NOR_2), PIN_DTCK
- S10 (DFF)
- S11 (NOR_2), SRA3
- AH95 (OR_2) → AH95
- S11

Buffer section:

- REG22F_D0 → AC119 (INV) → AC120 (INV) → REG22F_D0_BUF3
- AB51 (INV) → AB50 (INV) → REG22F_D0_BUF
- AB54 (INV) → AB53 (INV) → REG22F_D0_BUF2
- PIN_CLK → S6 (BUF) → S5 (OR_2) → ROMA_CLK
- S8 (BUF) → M31 (INV) → M32 (BUF) → M33 (INV) → CLK_BUF
- S8
- M36 (INV) → M37 (BUF) → M37

AA40
AA47

Block	Labels
M19 DFFSNNQ	R69, MUX_A_D7, L9, CLK, D, S, Q, Q̄
R62 FA1	A, B, CI, S, CO, STEP15
R58 AOI22	RD_REG7
R59 INV	MUXD15
R68 DFFSNNQ	MUX_A_D6, STEP14
R61 FA1	A, B, CI, S, CO
R56 AOI22	RD_REG6
R57 INV	MUXD14
R64 DFFSNNQ	MUX_A_D5, STEP13
R60 FA1	A, B, CI, S, CO
R55 AOI22	RD_REG5
R54 INV	MUXD13
S70 DFFSNNQ	MUX_A_D4, STEP12
T47 FA1	A, B, CI, S, CO
T39 AOI22	RD_REG4
T40 INV	MUXD12
R67 DFFSNNQ	MUX_A_D3, STEP11
T48 FA1	A, B, CI, S, CO
T38 AOI22	RD_REG3
T37 INV	MUXD11
R70 DFFSNNQ	MUX_A_D2, STEP10
T49 FA1	A, B, CI, S, CO
V48 AOI22	RD_REG2
V49 INV	MUXD10
S71 DFFSNNQ	MUX_A_D1, STEP9
T50 FA1	A, B, CI, S, CO
T45 AOI22	RD_REG1
T46 INV	MUXD9
S72 DFFSNNQ	MUX_A_D0, STEP8
T51 FA1	A, B, CI, S, CO
R65 AOI22	RD_REG0
R66 INV	MUXD8
P51 DFFSNNQ	MUX_B_D7, STEP7
T52 FA1	A, B, CI, S, CO
S65 AOI22	RD_REG2_7
S66 INV	MUXD7
P52 DFFSNNQ	MUX_B_D6, STEP6
W38 FA1	A, B, CI, S, CO
W31 AOI22	RD_REG2_6
W32 INV	MUXD6
P53 DFFSNNQ	MUX_B_D5, STEP5
W37 FA1	A, B, CI, S, CO
X27 AOI22	RD_REG2_5
X28 INV	MUXD5
P57 DFFSNNQ	MUX_B_D4, STEP4
W36 FA1	A, B, CI, S, CO
X25 AOI22	RD_REG2_4
X26 INV	MUXD4
P58 DFFSNNQ	MUX_B_D3, STEP3
W35 FA1	A, B, CI, S, CO
Z38 AOI22	RD_REG2_3
Z39 INV	MUXD3
P49 DFFSNNQ	MUX_B_D2, STEP2
W34 FA1	A, B, CI, S, CO
X31 AOI22	RD_REG2_2
X32 INV	MUXD2
P50 DFFSNNQ	MUX_B_D1, STEP1
W33 FA1	A, B, CI, S, CO
X29 AOI22	RD_REG2_1
X30 INV	MUXD1
P45 DFFSNNQ	MUX_B_D0, STEP0, GND
W27 FA1	A, B, CI, S, CO
X24 AOI22	RD_REG2_0
X23 INV	MUXD0

Right-side logic:

- AA50 OR_2: inputs DTYPE2, DTYPE1 → AA50
- AA49 INV: input TESTREG2_D2
- AA48 AND_2
- AA45 NOR_2: input V38A
- AA46 INV
- AA40 NOR_2 → AA40
- AA47 NOR_2 → AA47

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STEP TYPE MUX

DTYPE2 — AA42 INV — S60 INV — DTYPE2_BUF

DTYPE1 — AA41 INV — S61 INV — DTYPE1_BUF

DPCM_STEP7 — S63 — RD_REG7 — A B S MUX21N — S62 INV — STEP15

DTYPE2_BUF — S64 OR_2
DTYPE1_BUF —

S53 INV

RD_REG6 / DPCM_STEP6 — S59 A B S GND MUX21ND — S58 A B S MUX21ND — STEP14
DTYPE1_BUF

RD_REG5 / DPCM_STEP5 — S52 A B S MUX21ND — S51 A B S MUX21ND — STEP13

RD_REG4 / DPCM_STEP4 — T42 A B S MUX21ND — T41 A B S MUX21ND — STEP12

RD_REG3 / DPCM_STEP3 — T43 A B S MUX21ND — T44 A B S MUX21ND — STEP11

TESTREG2_D2 — R73 OR_2 — R71 BUF
DTYPE0 —

CLKDIV8D_2 — S47 INV — S48 INV — S49 INV

RD_REG7 — S67 CLK D S Q̄ DFFSNNQ — RD_REG2_7
RD_REG6 — S68 CLK D S Q̄ DFFSNNQ — RD_REG2_6
RD_REG5 — X34 CLK D S Q̄ DFFSNNQ — RD_REG2_5
RD_REG4 — X33 CLK D S Q̄ DFFSNNQ — RD_REG2_4
RD_REG3 — Z48 CLK D S Q̄ DFFSNNQ — RD_REG2_3
RD_REG1 — X36 CLK D S Q̄ DFFSNNQ — RD_REG2_1
RD_REG2 — X35 CLK D S Q̄ DFFSNNQ — RD_REG2_2
RD_REG0 — X37 CLK D S Q̄ DFFSNNQ — RD_REG2_0

DPCM_STEP7 / DPCM_STEP6 / DPCM_STEP2 / RD_REG_2 — V45 D0 D1 D2 D3 S0 S1 Z MUX41N — V44 INV — STEP10

DPCM_STEP5 / DPCM_STEP1 / RD_REG_1 — V41 D0 D1 D2 D3 S0 S1 Z MUX41N — V40 INV — STEP9

DPCM_STEP4 / DPCM_STEP0 / RD_REG_0 — V42 D0 D1 D2 D3 S0 S1 Z MUX41N — V43 INV — STEP8

DPCM_STEP3 / GND / RD_REG2_7 — S56 D0 D1 D2 D3 S0 S1 Z MUX41N — S57 INV — STEP7

DPCM_STEP6 / DPCM_STEP2 / RD_REG2_6 — V46 D0 D1 D2 D3 S0 S1 Z MUX41N — V47 INV — STEP6

DPCM_STEP5 / DPCM_STEP1 / RD_REG2_5 — X46 D0 D1 D2 D3 S0 S1 Z MUX41N — X47 INV — STEP5

DPCM_STEP4 / DPCM_STEP0 / RD_REG2_4 — W29 D0 D1 D2 D3 S0 S1 Z MUX41N — W28 INV — STEP4

DPCM_STEP3 / RD_REG2_3 — X44 D0 D1 D2 D3 S0 S1 Z MUX41N — X45 INV — STEP3

DPCM_STEP2 / RD_REG2_2 — X42 D0 D1 D2 D3 S0 S1 Z MUX41N — X43 INV — STEP2

DPCM_STEP1 / RD_REG2_1 — X41 D0 D1 D2 D3 S0 S1 Z MUX41N — X40 INV — STEP1

DPCM_STEP0 / RD_REG2_0 — X39 D0 D1 D2 D3 S0 S1 Z MUX41N — X38 INV — STEP0

DTYPE2 / DTYPE1 — Z26 NAND_2
STEP7 — V39 AND_2

STEP6 STEP5 STEP4 STEP3 STEP2 STEP1 STEP0 — V38C NOR_8 — V38B INV — V38A NAND_2 — V38A
Stop marker detect ?

DTYPE2 — Y46B INV
STEP12 — V34 AND_2
STEP13 — V35 AND_2
STEP14 — V33D AND_2
STEP9 — V37 AND_2
STEP11 — V36 AND_2
STEP10 — V33C AND_2
STEP8 — V33B AND_2
STEP15 — V33 INV

V34B NOR_8

Weird but STEP9 and 10
don't seem swapped

FINAL OUTPUT PISO

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Signals:
S11
PIN_AXXA
TESTREG2_D6
PIN_DTCK
REG22F_D0_BUF3
PIN_AXDT

REGEF0T, GND, REGEF1T, REGEF2T, REGEF3T, REGEF4T, REGEF5T, REGEF6T, REGEF7T
REGEF8T, REGEF9T, REGEF10T, REGEF11T, REGEF12T, REGEF13T, REGEF14T, REGEF15T
REGEE0T, REGEE1T, REGEE2T, REGEE3T, REGEE4T, REGEE5T, REGEE6T, REGEE7T
REGEE8T, REGEE9T, REGEE10T, REGEE11T, REGEE12T, REGEE13T, REGEE14T, REGEE15T

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Konami 054539 — MUX C

Input signals (left): SRA6, SRA5, SRA1, AJ106, AJ83, AM47B

Inverter chain:
- AR51 (INV), AP49 (INV), AP48 (INV)
- AS97 (INV), AP66 (INV), AP65 (INV)
- AJ115 (INV), AJ128 (INV), AJ129 (INV)
- AJ96 (INV), AJ104 (INV), AJ103 (INV)
- AL62 (INV), AN48 (INV)
- AN45 (INV), AN49 (INV)

Column 1 (MULB_OUT15 … MULB_OUT12):
- AR54, AS85, AJ99, AL78 (LATCHN) → AK61 (MUX41N) → AK60 (BUF) → MUXC15
- AR65, AS84, AJ98, AL77 (LATCHN) → AK63 (MUX41N) → AK62 (BUF) → MUXC14
- AR62, AS81, AJ97, AL74 (LATCHN) → AK65 (MUX41N) → AK64 (BUF) → MUXC13
- AR63, AS82, AJ101, AL75 (LATCHN) → AK66 (MUX41N) → AK67 (BUF) → MUXC12

Column 2 (MULB_OUT11 … MULB_OUT8):
- AR64 (AR51), AS83 (AS97), AJ88 (AJ115), AL76 (AJ96) (LATCHN) → AK69 (MUX41N) → AK68 (BUF) → MUXC11
- AR61, AS80, AJ87, AL73 (LATCHN) → AK70 (MUX41N) → AK71 (BUF) → MUXC10
- AR60, AS79, AJ86, AL72 (LATCHN) → AK72 (MUX41N) → AK73 (BUF) → MUXC9
- AR59, AS78, AJ79, AL71 (LATCHN) → AK74 (MUX41N) → AK75 (BUF) → MUXC8

Column 3 (MULB_OUT7 … MULB_OUT4):
- AS89 (AR51), AS92 (AS97), AL70 (AJ115), AR67 (AJ96) (LATCHN) → AM59 (MUX41N) → AM58 (BUF) → MUXC7
- AS88 (AR51), AS91 (AS97), AL69 (AJ115), AR58 (AJ96) (LATCHN) → AM57 (MUX41N) → AM56 (BUF) → MUXC6
- AS87 (AR51), AS90 (AS97), AL68 (AJ115), AR57 (AJ96) (LATCHN) → AM55 (MUX41N) → AM54 (BUF) → MUXC5
- AS77 (AR51), AS86 (AS97), AK57 (AJ115), AL67 (AJ96) (LATCHN) → AK58 (MUX41N) → AK59 (BUF) → MUXC4

Column 4 (MULB_OUT3 … MULB_OUT0):
- AR66 (AR51), AS96 (AS97), AJ100 (AJ115), AR50 (AJ96) (LATCHN) → AM66 (MUX41N) → AM67 (BUF) → MUXC3
- AR68 (AR51), AS95 (AS97), AJ102 (AJ115), AL79 (AJ96) (LATCHN) → AM65 (MUX41N) → AM64 (BUF) → MUXC2
- AR56 (AR51), AS94 (AS97), AJ90 (AJ115), AR49 (AJ96) (LATCHN) → AM62 (MUX41N) → AM63 (BUF) → MUXC1
- AR55 (AR51), AS93 (AS97), AJ89 (AJ115), AR48 (AJ96) (LATCHN) → AM60 (MUX41N) → AM61 (BUF) → MUXC0

Mux select lines: AN45, AL62 → S0/S1

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AD157
BUF
CLKDIV32D_2

AD158
OR_6
CLKDIV64D
GND
CLKDIV4D_4
CLKDIV8D_4
CLKDIV16D_3

AG115
BUF
CLKDIV2D_3

AD159
NAND_4
AE120
AE119

AG116
CLK Q
D Q̄
DFF

AG113
BUF
AG113

AD160
OR_3
CLKDIV16D_2
CLKDIV8D_2
CLKDIV4D_3

AE119
OR_6
CLKDIV64D_4
CLKDIV32D_2
CLKDIV16D_3
CLKDIV8D_4
CLKDIV4D_3
GND
AE119

AE120
OR_6
CLKDIV4D_4
GND
AE120

AE84A
INV
CLKDIV128D_4

AE84B
A Z
B
S
MUX21N
REG224_D3

AG83
CLK Q̄
D̄
DFFNNQ
AG83

AG97
INV
REG225_D4

AE86
INV

AE94
INV
REG225_D5

AE88
INV

AH105
INV

AH106
INV

AH99
INV
AF117

AB116
INV

AB117B AB117A
INV   INV

AB122
BUF
CLKDIV2D_2

AE87
D0 Z
D1
D2
D3
S0
S1
MUX41N

AC86
A S
B
CI CO
FA1
AD101

AF89
AND_2
AG113

AF77
CLK Q̄
D̄
DFFNNQ

AH74
CLK Q̄
D̄
DFFNNQ
ACCC7

AE77
A S
B
CI CO
FA1
AD97

AF81
AND_2

AF78
CLK Q̄
D̄
DFFNNQ

AH75
CLK Q̄
D̄
DFFNNQ
ACCC6

AE78
A S
B
CI CO
FA1
AD96

AF80
AND_2

AF79
CLK Q̄
D̄
DFFNNQ

AH76
CLK Q̄
D̄
DFFNNQ
ACCC5

AE79
A S
B
CI CO
FA1
AD100

AF96
AND_2

AG87
CLK Q̄
D̄
DFFNNQ

AH77
CLK Q̄
D̄
DFFNNQ
ACCC4

AE80
A S
B
CI CO
FA1
AD95

AF95
AND_2

AG88
CLK Q̄
D̄
DFFNNQ

AH78
CLK Q̄
D̄
DFFNNQ
ACCC3

AE81
A S
B
CI CO
FA1
AD99

AF94
AND_2

AG89
CLK Q̄
D̄
DFFNNQ

AH79
CLK Q̄
D̄
DFFNNQ
ACCC2

AE82
A S
B
CI CO
FA1
AD98

AF93
AND_2

AG90
CLK Q̄
D̄
DFFNNQ

AH80
CLK Q̄
D̄
DFFNNQ
ACCC1

AE83
A S
B
CI CO
FA1
AD94

AF92
AND_2

AG91
CLK Q̄
D̄
DFFNNQ

AH81
CLK Q̄
D̄
DFFNNQ
ACCC0

AE121
NAND_2
AE120
AE119

AE73
BUF
AE73

AD106
A S
B
CI CO
FA1
AD86
AG113

AF90
AND_2

AF82
CLK Q̄
D̄
DFFNNQ

AD107
A S
B
CI CO
FA1
AD87

AF91
AND_2

AG85
CLK Q̄
D̄
DFFNNQ

AG82
CLK Q̄
D̄
DFFNNQ
ACCC14

AD108
A S
B
CI CO
FA1
AD88

AF88
AND_2

AG86
CLK Q̄
D̄
DFFNNQ

AG84
CLK Q̄
D̄
DFFNNQ
ACCC13

AC91
A S
B
CI CO
FA1
AD89

AF87
AND_2

AG78
CLK Q̄
D̄
DFFNNQ

AG81
CLK Q̄
D̄
DFFNNQ
ACCC12

AC90
A S
B
CI CO
FA1
AD90

AF86
AND_2

AG79
CLK Q̄
D̄
DFFNNQ

AH68
CLK Q̄
D̄
DFFNNQ
ACCC11

AC89
A S
B
CI CO
FA1
AD91

AF85
AND_2

AG80
CLK Q̄
D̄
DFFNNQ

AH67
CLK Q̄
D̄
DFFNNQ
ACCC10

AC88
A S
B
CI CO
FA1
AD92

AF84
AND_2

AF75
CLK Q̄
D̄
DFFNNQ

AH69
CLK Q̄
D̄
DFFNNQ
ACCC9

AC87
A S
B
CI CO
FA1
AD93

AF83
AND_2

AF76
CLK Q̄
D̄
DFFNNQ

AH72
CLK Q̄
D̄
DFFNNQ
ACCC8

WR21C

AP8_Q
AP6 INV
AP5 INV

AL22 INV
AK27 INV
AK26 INV
RES

AL28
D
E
NQ
LATCHN
PIN_DB7_IN_BUF

AL27
D
E
NQ
LATCHN
PIN_DB6_IN_BUF

AK20
D
E
NQ
LATCHN
PIN_DB5_IN_BUF

AK22
D
E
NQ
LATCHN
PIN_DB4_IN_BUF

AK24
D
E
NQ
LATCHN
PIN_DB3_IN_BUF

AK19
D
E
NQ
LATCHN
PIN_DB2_IN_BUF

AL19
D
E
NQ
LATCHN
PIN_DB1_IN_BUF

AK25
D
E
NQ
LATCHN
PIN_DB0_IN_BUF

AL29
CLK
D
S
Q
DFFSNQ

AL26
CLK
D
S
Q
DFFSNQ

AK21
CLK
D
S
Q
DFFSNQ

AK23
CLK
D
S
Q
DFFSNQ

AK25
CLK
D
S
Q
DFFSNQ

AK18
CLK
D
S
Q
DFFSNQ

AK20
CLK
D
S
Q
DFFSNQ

AK24
CLK
D
S
Q
DFFSNQ

ACCB7
ACCB6
ACCB5
ACCB4
ACCB3
ACCB2
ACCB1
ACCB0

AK37 XNOR_2
AK38 XNOR_2
AK33 XNOR_2
AK32 XNOR_2
AK31 XNOR_2
AK39 XNOR_2
AK30 XNOR_2
AK34 XNOR_2

AK35 NAND_8

AL17 INV

AL18 NOR_8

AL16
CLK
J
K
R
Q
Q
JKFFR
AL23
RES
AL16

AK29 NOR_8
AK28 INV
AM15 BUF
AM15

AJ5 INV
AJ4 INV
AJ3 INV
AP16_Q

AJ12 INV
AJ14 INV
AJ13 INV
WR223
RES

AL11
D
E
NQ
LATCHN
PIN_DB7_IN_BUF

AL7
D
E
NQ
LATCHN
PIN_DB6_IN_BUF

AK15
D
E
NQ
LATCHN
PIN_DB5_IN_BUF

AK16
D
E
NQ
LATCHN
PIN_DB4_IN_BUF

AL9
D
E
NQ
LATCHN
PIN_DB3_IN_BUF

AJ7
D
E
NQ
LATCHN
PIN_DB2_IN_BUF

AJ11
D
E
NQ
LATCHN
PIN_DB1_IN_BUF

AJ9
D
E
NQ
LATCHN
PIN_DB0_IN_BUF

AL10
CLK
D
S
Q
DFFSNQ

AL6
CLK
D
S
Q
DFFSNQ

AK14
CLK
D
S
Q
DFFSNQ

AK17
CLK
D
S
Q
DFFSNQ

AL8
CLK
D
S
Q
DFFSNQ

AJ6
CLK
D
S
Q
DFFSNQ

AJ10
CLK
D
S
Q
DFFSNQ

AJ8
CLK
D
S
Q
DFFSNQ

ACCA7
ACCA6
ACCA5
ACCA4
ACCA3
ACCA2
ACCA1
ACCA0

AK3 XNOR_2
AK2 XNOR_2
AK7 XNOR_2
AK8 XNOR_2
AK9 XNOR_2
AK1 XNOR_2
AK10 XNOR_2
AK6 XNOR_2

AK4 NAND_8

AL4 INV

AL5 NOR_8

AL3
CLK
J
K
R
Q
Q
JKFFR
AK13
RES
AL3

AK12 NOR_8
AK11 INV
AL1 BUF
AL1

AB168

AB174 INV   AB173

CLKDIV2D_5   INV   INV

AB150
MUXE15   A B   S   ACCE15
CI   CO
FA1

AB158
MULB_OUT15   CLK   Q̄   MUXE14
D
DFFNNQ

AB151
A B   S   ACCE14
CI   CO
FA1

AB159
MULB_OUT14   CLK   Q̄   MUXE13
D
DFFNNQ

AB152
A B   S   ACCE13
CI   CO
FA1

AC117
MULB_OUT13   CLK   Q̄   MUXE12
D
DFFNNQ

AD140
A B   S   ACCE12
CI   CO
FA1

AC118
MULB_OUT12   CLK   Q̄   MUXE11
D
DFFNNQ

AD139
A B   S   ACCE11
CI   CO
FA1

AG106
MULB_OUT11   CLK   Q̄   MUXE10
D
DFFNNQ

AD138
A B   S   ACCE10
CI   CO
FA1

AG107
MULB_OUT10   CLK   Q̄   MUXE9
D
DFFNNQ

AD137
A B   S   ACCE9
CI   CO
FA1

AG108
MULB_OUT9   CLK   Q̄   MUXE8
D
DFFNNQ

AD136
A B   S   ACCE8
CI   CO
FA1

AG114
MULB_OUT8   CLK   Q̄   MUXE7
D
DFFNNQ

AD135
A B   S   ACCE7
CI   CO
FA1

AG109
MULB_OUT7   CLK   Q̄   MUXE6
D
DFFNNQ

AF109
A B   S   ACCE6
CI   CO
FA1

AG110
MULB_OUT6   CLK   Q̄   MUXE5
D
DFFNNQ

AF110
A B   S   ACCE5
CI   CO
FA1

AG111
MULB_OUT5   CLK   Q̄   MUXE4
D
DFFNNQ

AF111
A B   S   ACCE4
CI   CO
FA1

AG112
MULB_OUT4   CLK   Q̄   MUXE3
D
DFFNNQ

AF112
A B   S   ACCE3
CI   CO
FA1

AG117
MULB_OUT3   CLK   Q̄   MUXE2
D
DFFNNQ

AF113
A B   S   ACCE2
CI   CO
FA1

AG120
MULB_OUT2   CLK   Q̄   MUXE1
D
DFFNNQ

AF114
A B   S   ACCE1
CI   CO
FA1

AH100
MULB_OUT1   CLK   Q̄   MUXE0
D
DFFNNQ

AG105
A B   S   ACCE0
CI   CO
FA1

AH102
MULB_OUT0   CLK   Q̄
D
DFFNNQ

AS110

AS111 INV   AS112

SRA0   INV   INV

Reverb volume ?

AS98
MULB_OUT15   CLK   Q   RD7_REG1
D
DFFNNQ

AS109
A B   S   ACCD15
CI   CO
FA1

AS99
MULB_OUT14   CLK   Q   RD6_REG1
D
DFFNNQ

AS108
A B   S   ACCD14
CI   CO
FA1

AS105
MULB_OUT13   CLK   Q   RD5_REG1
D
DFFNNQ

AS107
A B   S   ACCD13
CI   CO
FA1

AP67
MULB_OUT12   CLK   Q   RD4_REG1
D
DFFNNQ

AJ112
A B   S   ACCD12
CI   CO
FA1

AP68
MULB_OUT11   CLK   Q   RD3_REG1
D
DFFNNQ

AJ111
A B   S   ACCD11
CI   CO
FA1

AP69
MULB_OUT10   CLK   Q   RD2_REG1
D
DFFNNQ

AJ110
A B   S   ACCD10
CI   CO
FA1

AP70
MULB_OUT9   CLK   Q   RD1_REG1
D
DFFNNQ

AJ109
A B   S   ACCD9
CI   CO
FA1

AP71
MULB_OUT8   CLK   Q   RD0_REG1
D
DFFNNQ

AJ108
A B   S   ACCD8
CI   CO
FA1

AR69
MULB_OUT7   CLK   Q   RD7_REG2
D
DFFNNQ

AJ107
A B   S   ACCD7
CI   CO
FA1

AR70
MULB_OUT6   CLK   Q   RD6_REG2
D
DFFNNQ

AK80
A B   S   ACCD6
CI   CO
FA1

AR71
MULB_OUT5   CLK   Q   RD5_REG2
D
DFFNNQ

AK81
A B   S   ACCD5
CI   CO
FA1

AR72
MULB_OUT4   CLK   Q   RD4_REG2
D
DFFNNQ

AK82
A B   S   ACCD4
CI   CO
FA1

AR76
MULB_OUT3   CLK   Q   RD3_REG2
D
DFFNNQ

AK83
A B   S   ACCD3
CI   CO
FA1

AR77
MULB_OUT2   CLK   Q   RD2_REG2
D
DFFNNQ

AK84
A B   S   ACCD2
CI   CO
FA1

AR73
MULB_OUT1   CLK   Q   RD1_REG2
D
DFFNNQ

AK85
A B   S   ACCD1
CI   CO
FA1

AR74
MULB_OUT0   CLK   Q   RD0_REG2
D
DFFNNQ

AJ113
A B   S   ACCD0
CI   CO
GND   FA1

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AL12

AL13 AL14
INV INV

AP16_Q

AL3

AP7
A
B
CI CO
FA1
AL1

AN1
CLK Q
D
S
DFFSNNQ
ACCA7

AM2
A S
B
CI CO
FA1

AM1
CLK Q
D
S
DFFSNNQ
ACCA6

AM3
A S
B
CI CO
FA1

AP1
CLK Q
D
S
DFFSNNQ
ACCA5

AM4
A S
B
CI CO
FA1

AP2
CLK Q
D
S
DFFSNNQ
ACCA4

AM5
A S
B
CI CO
FA1

AP3
CLK Q
D
S
DFFSNNQ
ACCA3

AM6
A S
B
CI CO
FA1

AP9
CLK Q
D
S
DFFSNNQ
ACCA2

AM7
A S
B
CI CO
FA1

AP10
CLK Q
D
S
DFFSNNQ
ACCA1

AR3
A S
B
CI CO
FA1
VCC
GND

AP11
CLK Q
D
S
DFFSNNQ
ACCA0

AL21

AM19 AM20
INV INV

AP8_Q

AL16

AN3
A S
B
CI CO
FA1
AM15

AM8
CLK Q
D
S
DFFSNNQ
ACCB7

AN8
A S
B
CI CO
FA1

AM9
CLK Q
D
S
DFFSNNQ
ACCB6

AN9
A S
B
CI CO
FA1

AM11
CLK Q
D
S
DFFSNNQ
ACCB5

AN10
A S
B
CI CO
FA1

AM12
CLK Q
D
S
DFFSNNQ
ACCB4

AN11
A S
B
CI CO
FA1

AM10
CLK Q
D
S
DFFSNNQ
ACCB3

AN12
A S
B
CI CO
FA1

AM13
CLK Q
D
S
DFFSNNQ
ACCB2

AN13
A S
B
CI CO
FA1

AM16
CLK Q
D
S
DFFSNNQ
ACCB1

AM18
A S
B
CI CO
FA1
VCC
GND

AM17
CLK Q
D
S
DFFSNNQ
ACCB0

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ACC A and B

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R4
INV

R2
INV

R1
INV

$\overline{WR227}$

R30
D
E
NQ
LATCHNN

PIN_DB7_IN_BUF

R5
D
E
NQ
LATCHNN

PIN_DB6_IN_BUF

X1
D
E
NQ
LATCHNN

PIN_DB5_IN_BUF

W7
D
E
NQ
LATCHNN

PIN_DB4_IN_BUF

R17
D
E
NQ
LATCHNN

PIN_DB3_IN_BUF

R19
D
E
NQ
LATCHNN

PIN_DB2_IN_BUF

T9
D
E
NQ
LATCHNN

PIN_DB1_IN_BUF

T7
D
E
NQ
LATCHNN

PIN_DB0_IN_BUF

V1
D0
D1
D2
D3
Q0
Q1
Q2
Q3
RCO
ENP
ENT
CLK
LOAD
MR
COUNT163

VCC

TESTREG2_D1

R100
INV

R101
NAND_2

R102
NAND_2

R97
BUF

CLKDIV128D_5

M40
BUF

CLKDIV2D_3

R103
NAND_2

$\overline{CLKDIV2D\_3}$

T3
D0
D1
D2
D3
Q0
Q1
Q2
Q3
RCO
ENP
ENT
CLK
LOAD
MR
COUNT163

Y3
INV

Y4
NOR_2

REG22F_D5

X4
XOR_2

X5
CLK
D
R
Q
DFFR

PIN_TIM

REG22F_D5

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ADDER E

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TESTREG1_D5
TESTREG1_D4
TESTREG1_D3
TESTREG1_D2
TESTREG1_D1
TESTREG1_D0

Y98
NOR_6

TESTREG2_D4
TESTREG2_D2
TESTREG2_D1

Y96
NOR_3

Y97
NAND_2

TESTEN

RES
Z118
BUF

Z126
INV

PIN_TS1
Z127
INV

Z128
INV

Y110
CLK
D
R
Q
DFFRQ
TESTREG1_D7
PIN_RD07_IN

Y106
CLK
D
R
Q
DFFRQ
PIN_RD06_IN
AJ54
INV
AJ61
INV
TESTREG1_D6

Y101
CLK
D
R
Q
DFFRQ
PIN_RD05_IN
TESTREG1_D5

Y102
CLK
D
R
Q
DFFRQ
PIN_RD04_IN
TESTREG1_D4

Y103
CLK
D
R
Q
DFFRQ
PIN_RD03_IN
TESTREG1_D3

Y104
CLK
D
R
Q
DFFRQ
PIN_RD02_IN
TESTREG1_D2

Y105
CLK
D
R
Q
DFFRQ
PIN_RD01_IN
TESTREG1_D1

Y112
CLK
D
R
Q
DFFRQ
PIN_RD00_IN
Y111
BUF
TESTREG1_D0

RES
AA151
BUF

AA142
INV

PIN_TS2
AA1145
INV
AA144
INV

AA141
CLK
D
R
Q
DFFRQ
PIN_RD07_IN
TESTREG2_D7

AA143
CLK
D
R
Q
DFFRQ
PIN_RD06_IN
TESTREG2_D6

Z119
CLK
D
R
Q
DFFRQ
PIN_RD05_IN
P68
INV
TESTREG2_D5

AA139
CLK
D
R
Q
DFFRQ
PIN_RD04_IN
TESTREG2_D4

Z120
CLK
D
R
Q
DFFRQ
PIN_RD03_IN
TESTREG2_D3

AA140
CLK
D
R
Q
DFFRQ
PIN_RD02_IN
TESTREG2_D2

Z121
CLK
D
R
Q
DFFRQ
PIN_RD01_IN
TESTREG2_D1

Z116
CLK
D
R
Q
DFFRQ
PIN_RD00_IN
Z115
BUF
Z185
INV
X143
INV
TESTREG2_D0

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TEST REGISTERS
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A108
INV

A103
INV

A102
INV

A117B

A108

H56
INV

H54
INV

H53
INV

H61A

F71

F21
INV

F61
INV

F66

F20
INV

F48
INV

D14

MUX_B_D7

F95
D NQ
E
LATCHN

ADDE15

F53
D0 Z
D1
D2
D3
S0
S1
MUX41N

F47
XOR_2

F47

DLAT_D22

MUXD8

H45
D NQ
E
LATCHN

MUX_B_D6

F89
D NQ
E
LATCHN

ADDE14

F54
D0 Z
D1
D2
D3
S0
S1
MUX41N

D48
XOR_2

D48

DLAT_D21

MUXD7

H52
D NQ
E
LATCHN

MUX_B_D5

F94
D NQ
E
LATCHN

ADDE13

F58
D0 Z
D1
D2
D3
S0
S1
MUX41N

D51
XOR_2

D51

DLAT_D20

MUXD6

H51
D NQ
E
LATCHN

H51

MUX_B_D4

F93
D NQ
E
LATCHN

ADDE12

F59
D0 Z
D1
D2
D3
S0
S1
MUX41N

D52
XOR_2

D52

DLAT_D19

MUXD5

H50
D NQ
E
LATCHN

H50

MUX_B_D3

F92
D NQ
E
LATCHN

ADDE11

F56
D0 Z
D1
D2
D3
S0
S1
MUX41N

D50
XOR_2

D50

DLAT_D18

MUXD4

H49
D NQ
E
LATCHN

MUX_B_D2

F91
D NQ
E
LATCHN

ADDE10

F50
D0 Z
D1
D2
D3
S0
S1
MUX41N

D42
XOR_2

D42

DLAT_D17

MUXD3

H48
D NQ
E
LATCHN

MUX_B_D1

F90
D NQ
E
LATCHN

ADDE9

F60
D0 Z
D1
D2
D3
S0
S1
MUX41N

D53
XOR_2

D53

DLAT_D16

MUXD2

H47
D NQ
E
LATCHN

MUX_B_D0

F96
D NQ
E
LATCHN

ADDE8

F55
D0 Z
D1
D2
D3
S0
S1
MUX41N

D49
XOR_2

D49

DLAT_D15

MUXD1

H38
D NQ
E
LATCHN

H38

MUXD0

H40
D NQ
E
LATCHN

H40

D14

MUX_A_D7

K63
D NQ
E
LATCHN

ADDE23

K32
D0 Z
D1
D2
D3
S0
S1
MUX41N

L48
XOR_2

L48

DLAT_D30

MUXD15

L74
D NQ
E
LATCHN

MUX_A_D6

K59
D NQ
E
LATCHN

ADDE22

K33
D0 Z
D1
D2
D3
S0
S1
MUX41N

L49
XOR_2

L49

DLAT_D29

MUXD14

L69
D NQ
E
LATCHN

MUX_A_D5

L91
D NQ
E
LATCHN

ADDE21

K34
D0 Z
D1
D2
D3
S0
S1
MUX41N

L42
XOR_2

L42

DLAT_D28

MUXD13

L77
D NQ
E
LATCHN

MUX_A_D4

K57
D NQ
E
LATCHN

ADDE20

K35
D0 Z
D1
D2
D3
S0
S1
MUX41N

J41
XOR_2

J41

DLAT_D27

MUXD12

L67
D NQ
E
LATCHN

MUX_A_D3

K58
D NQ
E
LATCHN

ADDE19

K36
D0 Z
D1
D2
D3
S0
S1
MUX41N

J40
XOR_2

J40

DLAT_D26

MUXD11

L68
D NQ
E
LATCHN

MUX_A_D2

L88
D NQ
E
LATCHN

ADDE18

L61
D0 Z
D1
D2
D3
S0
S1
MUX41N

J42
XOR_2

J42

DLAT_D25

MUXD10

L76
D NQ
E
LATCHN

MUX_A_D1

J73
D NQ
E
LATCHN

ADDE17

J53
D0 Z
D1
D2
D3
S0
S1
MUX41N

J52
XOR_2

J52

DLAT_D24

MUXD9

L75
D NQ
E
LATCHN

MUX_A_D0

J71
D NQ
E
LATCHN

ADDE16

J54
D0 Z
D1
D2
D3
S0
S1
MUX41N

J51
XOR_2

J51

DLAT_D23

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