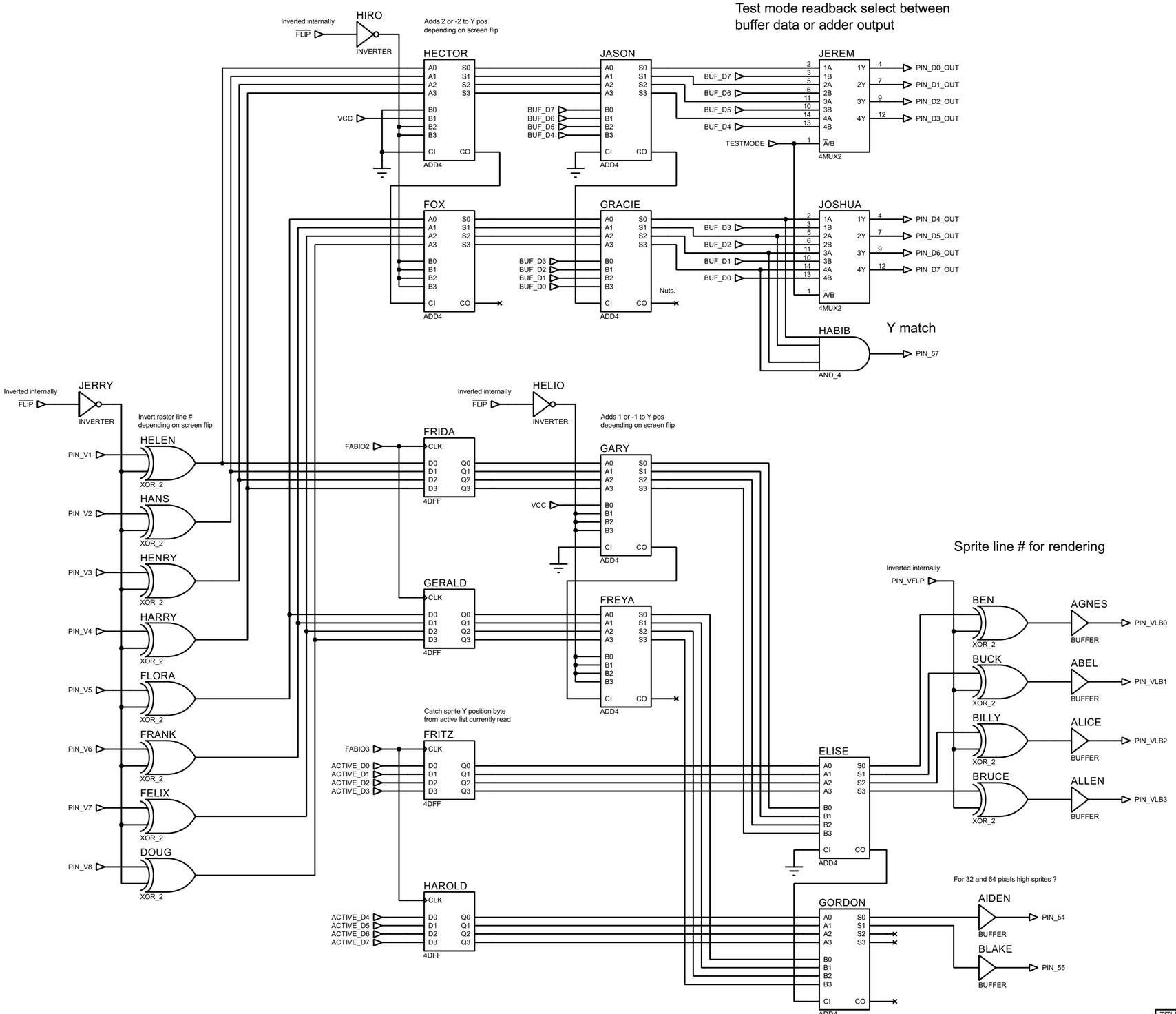


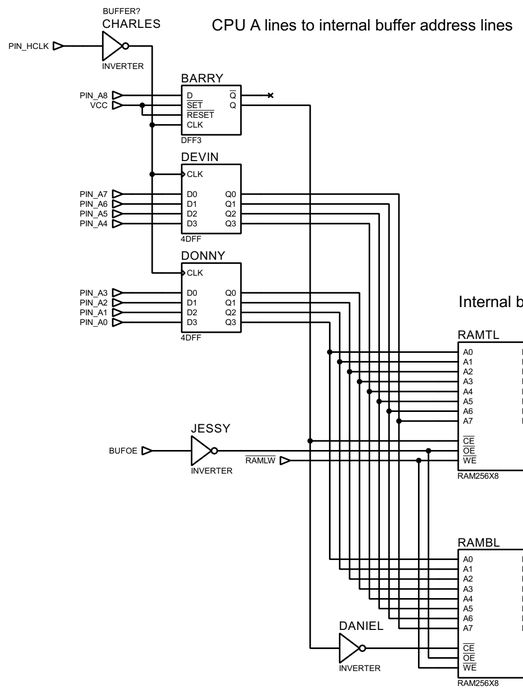
TITLE: Capcom 86S105 Y POSITION	DATE: 07/01/2025
BY: Sean Gonsalves REV: B	PAGE: 1/4

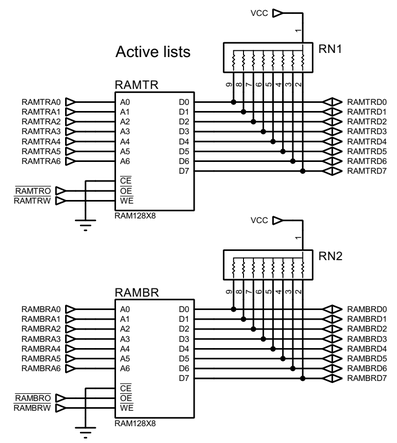
The internal buffer can hold 128 4-byte entries = 512 bytes
[0] is tile #
[1] is attributes (flags, palette...)
[2] is Y pos
[3] is X pos

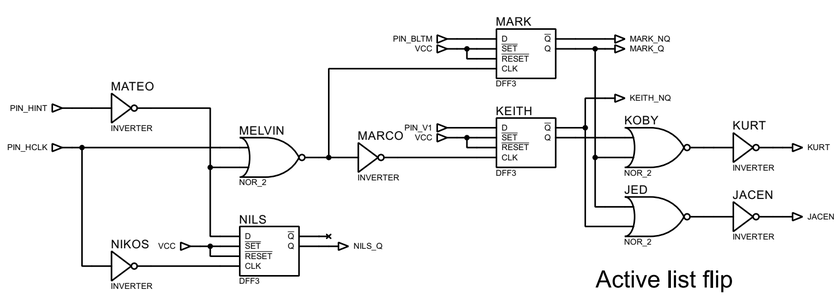
The two smaller RAM blocks are the active sprite lists
When one is used for rendering, the other is filled

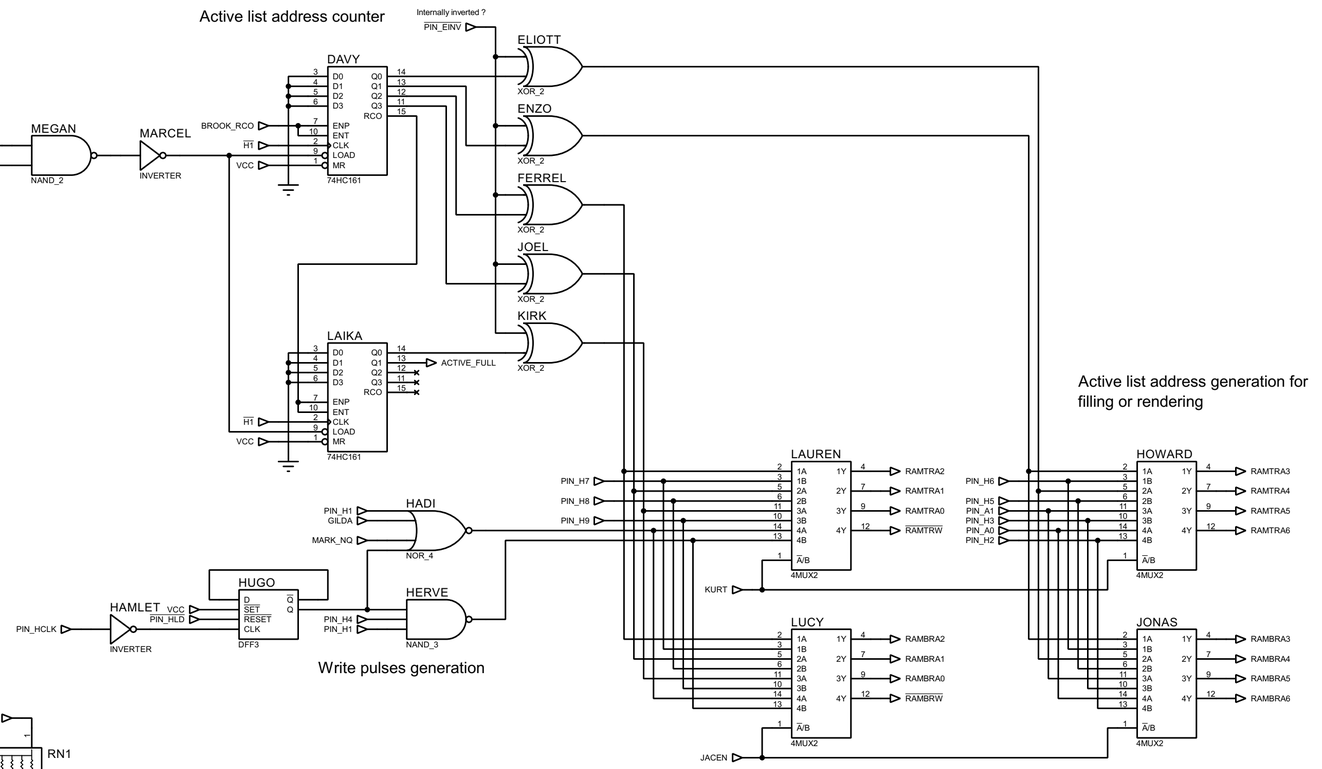
This chip DMAs the main work RAM to its internal buffer once per frame, and does Y matching to build active sprite lists each scanline.

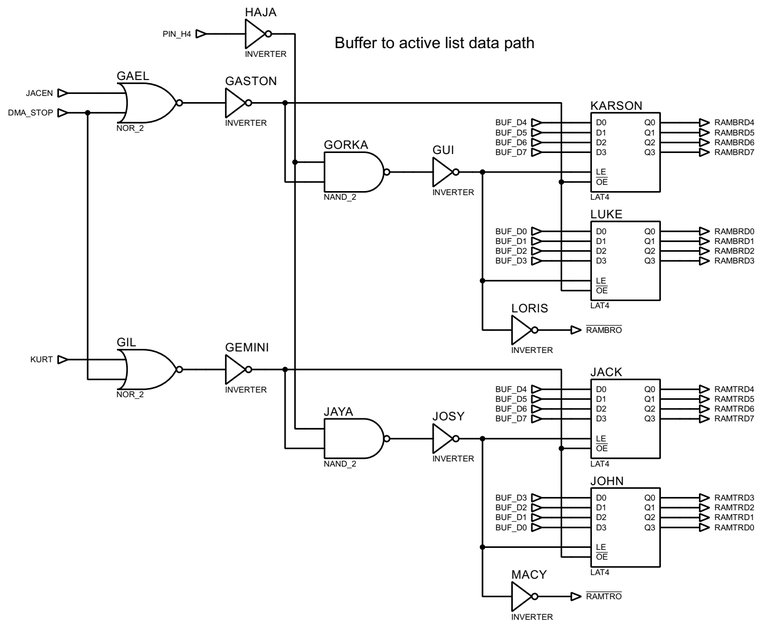
During rendering, the tile #, attributes and X pos bytes are output all at the same time (pipelines are used) for the external circuitry to fill the line buffers with the right pixels.







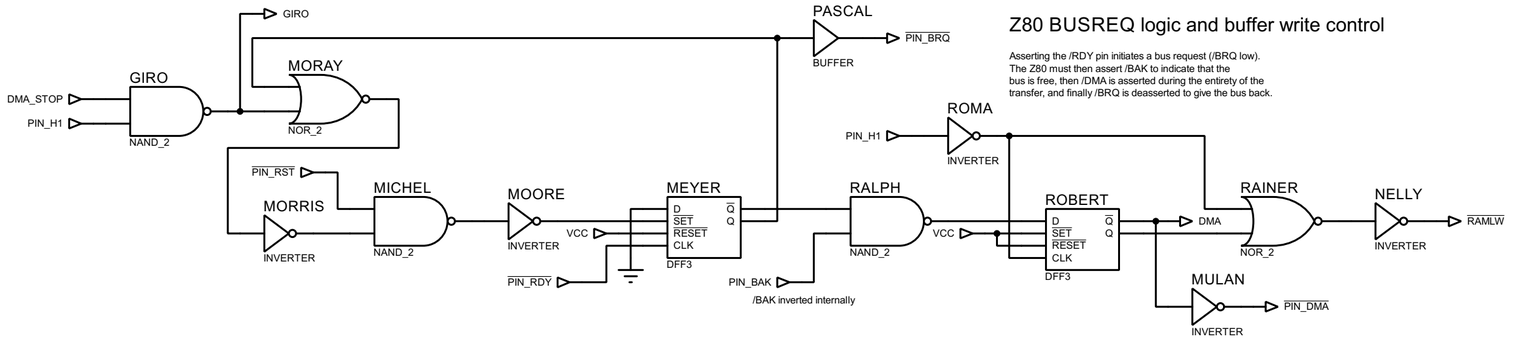




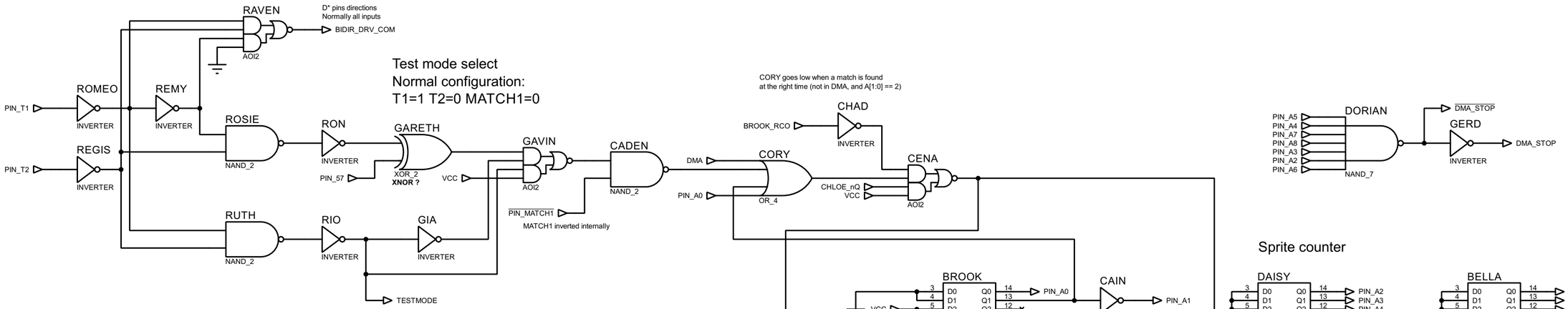
TITLE: Capcom 86S105 INTERNAL MEMORY	DATE: 07/01/2025
BY: Sean Gonsalves REV: B	PAGE: 2/4

Z80 BUSREQ logic and buffer write control

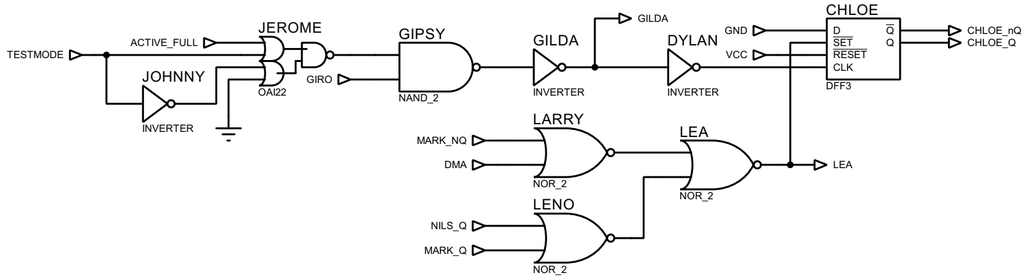
Asserting the /RDY pin initiates a bus request (/BRQ low).
The Z80 must then assert /BAK to indicate that the
bus is free, then /DMA is asserted during the entirety of the
transfer, and finally /BRQ is deasserted to give the bus back.



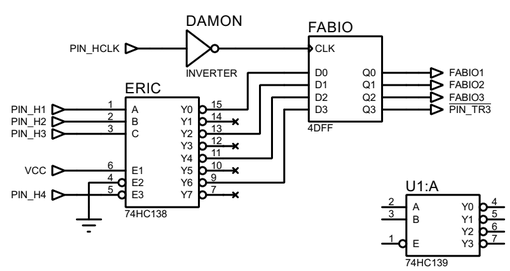
Test mode select
Normal configuration:
T1=1 T2=0 MATCH1=0



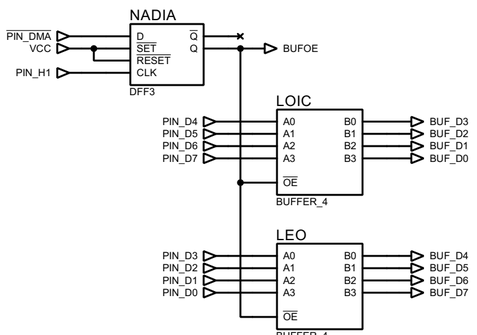
Buffer to active list copy sequencing



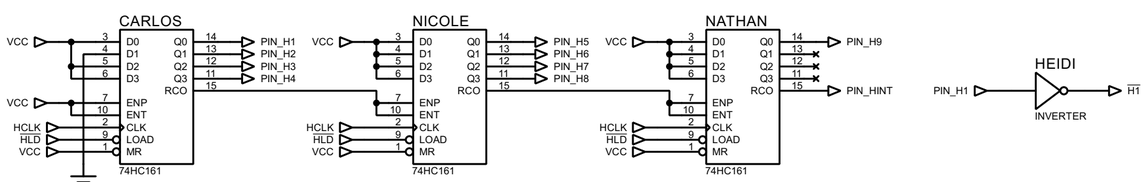
Final output sequencer



DMA Z80 data bus to internal buffer RAM

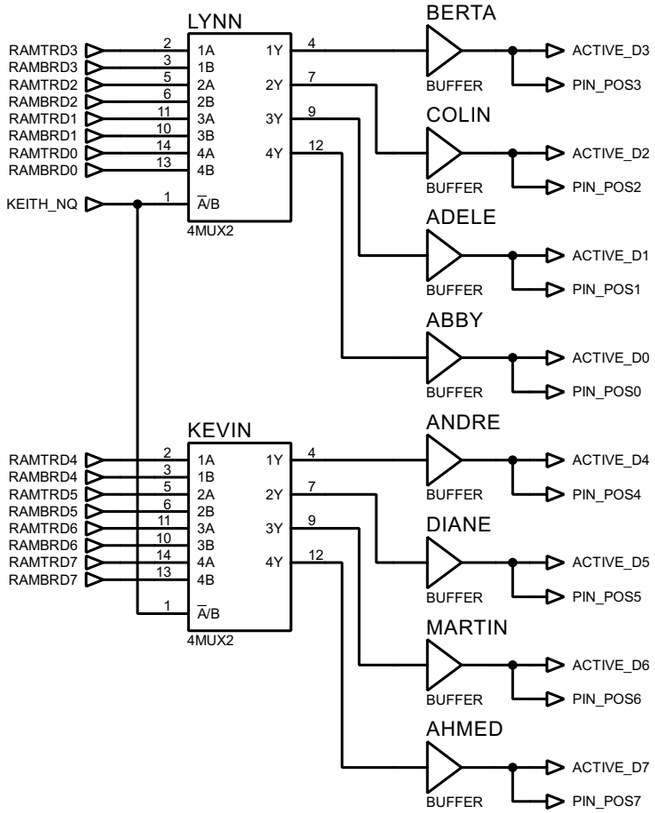


Internal horizontal counter

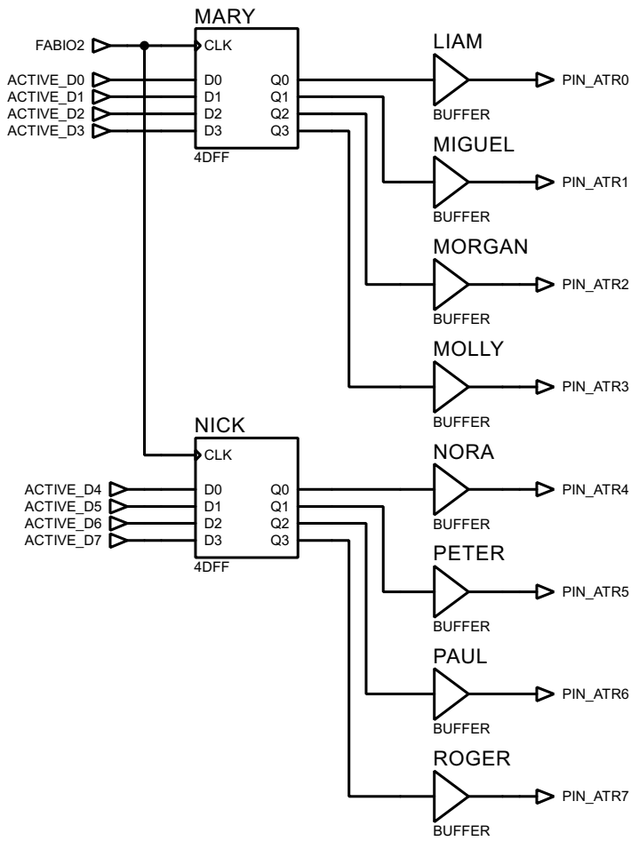


TITLE: Capcom 86S105 SEQUENCING	DATE: 07/01/2025
BY: Sean Gonsalves REV: B	PAGE: 3/4

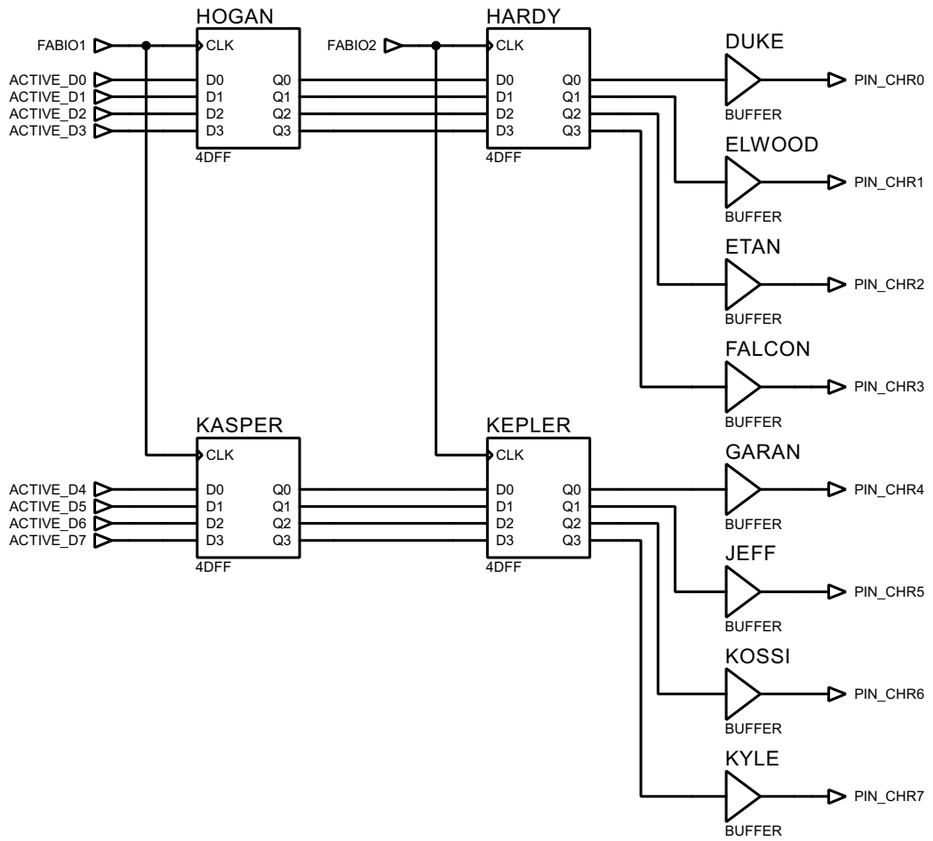
Active list selection for rendering
and x position byte output to POS pins



Active list attribute byte to ATR pins delay x1



Active list tile # byte to CHR pins delay x2



TITLE: Capcom 86S105 FINAL OUTPUTS	DATE: 07/01/2025
BY: Sean Gonsalves REV: B	PAGE: 4/4