CLK_BUF S45 CLK_BUF2
BUF

L14
INV

K13 K12
CLK_BUF INV INV

RES P31
P30
AND_2
NAND_8

CYCLERES
AB86
INV CYCLERES

PIN_NRES
R131 R130 R129
CLK_BUF CLK Q NAND_2 INV RES
D Q
DFF

P37B P37A P36 P35
XNOR_2 NAND_2 CLK Q CLKDIV384
NAND_8 D
DFFN

VCC

P38A P38B P39 P40
XNOR_2 NAND_2 CLK Q CLKDIV192
NAND_6 D
DFFN

P32A P32B P33 P34
XNOR_2 NAND_2 CLK Q
NAND_6 D
DFFN

VCC

M14 M13 M12 M10
XNOR_2 NAND_2 CLK Q
NAND_4 D
DFFN

R41 R42 R43 R44
XNOR_2 NAND_2 CLK Q
NAND_3 D
DFFN

R34B R34A R33 R32
XNOR_2 NAND_2 CLK Q CLKDIV12
NAND_2 D
DFFN

R47 R48 R49
XOR_2 NAND_2 CLK Q
D
DFFN

RES R51 R52 R53
XOR_2 NAND_2 CLK Q
D
DFFN

Divide by 3
R50 S36
NAND_2 INV

R45 R46
CLK Q
AND_3 D
DFFN

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CLOCK DIV HIGH

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Signal and component labels present on the schematic:

PIN_DTCK, PIN_DTCK, CLKDIV12, H7 DFF, P17 INV
G113 INV, F122 INV, F121 INV, CLK_BUF
L137 INV, F120 INV, F119 INV, CLK_BUF
L135 INV, L136 INV, L105 BUF, CLKDIV512D_3
L10 INV, L11 INV, K89 DFF, L115 INV, F19 BUF, F14 INV, CLKDIV512D_2
CLK_BUF, AB160 BUF, CLKDIV512D
K68 MUX21N (A B S Z), PIN_YMD, TESTREG1_D7, K69 INV, CLKDIV512T, CLKDIV512D2

K74A NAND_8, K74B XNOR_2, K75 NAND_2, K76 DFFN
K70A NAND_8, K70B XNOR_2, K71 NAND_2, K72 DFFN
L139 INV, L140 BUF, L138 INV, CLKDIV256D_2
A138 DFFNNQ, J111 INV, J112 INV, K102 BUF, CLKDIV256D_3, CLKDIV256
K66 NAND_6, K65B XNOR_2, K65A NAND_2, K64 DFFNNQ
L94 DFFNNQ, T81 INV, AB161 BUF, CLKDIV128D_3, R63 BUF, CLKDIV128D_3, CLKDIV128D_5, W76 BUF, W72 INV, CLKDIV128D_2
T80 INV, T79 INV, AB123 BUF, CLKDIV128D_4, CLKDIV128

J88B NAND_6, J88A XNOR_2, J87 NAND_2, J85 DFFN
L104 DFFNNQ, W80 INV, AB162 BUF, CLKDIV64D, AF118 BUF, CLKDIV64D_4, W78 BUF, W71 INV, CLKDIV64D_2
W84 INV, W85 INV, AA80 BUF, CLKDIV64D_3, CLKDIV64

J89A NAND_4, J89B XNOR_2, J90 NAND_2, J91 DFFNNQ
C87 DFFNNQ, C94 INV, E65 BUF, CLKDIV32D_2, CLKDIV32D, E61 BUF, CLKDIV32D_3
C89 INV, C88 INV, Z129 BUF, CLKDIV32D_5, AB179 BUF, CLKDIV32D_2, CLKDIV32D_4, H55 BUF, H55, CLKDIV32

AB176 BUF, CLKDIV16D_3, W89 BUF, CLKDIV16D_4, S106 BUF, CLKDIV16D_5, CLKDIV16D_4
B96 INV, E67 BUF, CLKDIV16D_2, AB180 BUF, CLKDIV16D_2
J84 NAND_3, J83 XNOR_2, J82B NAND_2, J82A DFFN
B100 DFFNNQ, B95 INV, B94 INV, F75 BUF, CLKDIV16D_3, CLKDIV16

G115 INV, M29 INV, PIN_CLK3, G115
E111 DFFNNQ, CLKDIV8D, M38 BUF, CLKDIV8D_2, E66 BUF, AG118 INV, CLKDIV8D_3, CLKDIV8D_4, CLKDIV8
H71 NAND_2, H72 XNOR_2, H73 NAND_2, H74 DFFN

M28 INV, PIN_CLK2, B97 INV, E62 BUF, CLKDIV4D_3, B102 INV, AB165 BUF, CLKDIV4D_4
AB177 BUF, CLKDIV4D_4, CLKDIV4D_3, M39 BUF, CLKDIV4D_2, B103 INV, D61 BUF, CLKDIV4D_5
J75A XOR_2, J75B NAND_2, J76 DFFN
B101 DFFNNQ, CLKDIV4

C72 BUF, C68 INV, C67 INV, CLKDIV2D_2
D88 DFFNNQ, D89 INV, CLKDIV2D_2, AB175 BUF, CLKDIV2D_5, CLKDIV2
D94 INV, D95 INV, CLKDIV2D_3
K60 OR_2, K62 DFFN, K56 INV, K67 INV, CYCLERES
VCC

CLKDIV32, L102 INV, CLKDIV32
CLKDIV16, L103 INV, CLKDIV16
CLKDIV8, L95 INV, CLKDIV8
CLKDIV4, L93 INV, CLKDIV4
CLKDIV8D, K101 INV, K100 INV, CLKDIV8D_2, E58 BUF, CLKDIV8D_3
CLKDIV4_BUF, AB127 BUF, CLKDIV4_BUF2

CLKDIV2D_2

CLKDIV32D
CLKDIV16D_2   D72
CLKDIV8D_3   NAND_4
CLKDIV4D_3

D71 CLK D Q Q̄ DFF → TRIGA

CLKDIV32D_3
CLKDIV16D_3   D68
CLKDIV8D_3   NAND_4
CLKDIV4D_5

D67 CLK D Q Q̄ DFF

D8 AND_2 → D8

CLKDIV32D
CLKDIV16D_2   D74
CLKDIV8D_3   NAND_4
CLKDIV4D_5

D73 CLK D Q Q̄ DFF

D9 AND_2 → D9

→ TRIGJ

CLKDIV32D
CLKDIV16D_3   D75
CLKDIV8D_3   NAND_4
CLKDIV4D_5

D76 CLK D Q Q̄ DFF → TRIGB

CLKDIV32D
CLKDIV16D_2   E63
CLKDIV8D_3   NAND_4
CLKDIV4D_3

E64 CLK D Q Q̄ DFF → TRIGC

CLKDIV32D_3
CLKDIV16D_2   D60
CLKDIV8D_3   NAND_4
CLKDIV4D_3

D59 CLK D Q Q̄ DFF → TRIGD

CLKDIV4D_5
CLKDIV8D_3   E50
CLKDIV16D_2   NAND_4
CLKDIV32D_3

E49 CLK D Q Q̄ DFF → TRIGF

CLKDIV32D
CLKDIV16D_2   E59
CLKDIV8D_3   NAND_4
CLKDIV4D_5

E60 CLK D Q Q̄ DFF → TRIGE

CLKDIV32D_3
CLKDIV4D_5   D69 AND_2

D70 CLK D Q Q̄ DFF → TRIGG

CLKDIV4D_5
CLKDIV8D_3   E56
CLKDIV16D_2   NAND_4
CLKDIV32D

E55 AND_2

CLKDIV8D_3
CLKDIV4D_3   E57
CLKDIV16D_3   NAND_4
CLKDIV32D

E54 CLK D Q Q̄ DFF
CLKDIV4_BUF

F63 XOR_2 → TRIGH

CLK_BUF

H58 A B X0 X1 X2 X3 DEC2
CLKDIV16D_4
CLKDIV32D_4

F118 NOR_2 → F118

J70 NOR_2 → J70

H57 NOR_2 → H57

H61B NOR_2

H61A NAND_4 → H61A
842
H61A 010

H59 INV
CLKDIV8D_2

H63 INV
CLKDIV4D_4   H62 INV

H60 INV
CLKDIV2D_3

D96 INV

TRIGC → D87 INV   D86 INV → TRIGC_BUF2

TRIGC → D92 BUF   D93 INV
D97 INV   D98 INV → TRIGC_BUF

A114 INV
TRIGB → A115 INV   A116 INV → TRIGB_BUF2

C93 INV
TRIGB → C91 INV   C90 INV → TRIGB_BUF

CLKDIV2D_2 → N42 BUF
N43 NAND_2 → N43
CLKDIV4D_2

CLK_BUF → N41 CLK D Q Q̄ DFF → IRAM_INT
N44 INV   N70 INV → IRAM_INT‾

K47 INV   K44 INV   J70
CLKDIV8D_2

K45 INV   K48 INV
CLKDIV4D_4

K46 INV   J66 INV
CLKDIV2D_3

K50 NAND_4 → K50
J64 NAND_4 → J64
J65 NAND_4 → B74 BUF → B74
J62 NAND_4 → K54 BUF   K2 INV
J63 NAND_4 → J72 BUF → J72
K49 NAND_4 → K49

K1 INV → L9
L9 INV

842
K50 101
J64 010
J65 110
J62 100
J63 000
K49 001

H98 INV   F123 INV   F118
CLKDIV8D_2

H99 INV   J107 INV
CLKDIV4D_4

A126 INV   N139 INV
CLKDIV2D_3

N144 NAND_4 → N147 BUF → N147
N145 NAND_4 → N145
N149 NAND_4 → N149
N146 NAND_4 → N146
N152 NAND_4 → N152
M93 NAND_4 → M93

842
N144 110
N145 010
N149 000
N146 100
N152 001
M93 101

A124 INV   H57
CLKDIV8D_2

A123 INV   A118 INV
CLKDIV4D_4

A120 INV   A121 INV
CLKDIV2D_3

A117 NAND_4
B98 BUF → B98
B99 BUF → B99

A122 NAND_4 → B77 BUF → B77

A119 NAND_4 → A117B BUF → A117B

842
A117 010
A122 001
A119 000

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PIN_AB09 R7 INV R10 INV

P13 INV
P14 BUF P16 INV P15 INV IRAM_INT

P141 INV P142 INV PIN_AB00

P29 INV P28 INV PIN_AB00

P133 MUX21ND P2 CLK D Q̄ DFFNNQ R9 MUX21ND PIN_DB7_OUT
RAM_A_DOUT RAM_B_DOUT

N2 MUX21ND CH7_ACTIVE PIN_RD07_IN

P132 MUX21ND P3 CLK D Q̄ DFFNNQ R8 MUX21ND PIN_DB6_OUT
RAM_A_DOUT RAM_B_DOUT

N13 MUX21ND CH6_ACTIVE PIN_RD06_IN

P131 MUX21ND P4 CLK D Q̄ DFFNNQ R12 MUX21ND PIN_DB5_OUT
RAM_A_DOUT RAM_B_DOUT

N12 MUX21ND CH5_ACTIVE PIN_RD05_IN

P130 MUX21ND P5 CLK D Q̄ DFFNNQ R11 MUX21ND PIN_DB4_OUT
RAM_A_DOUT RAM_B_DOUT

N11 MUX21ND CH4_ACTIVE PIN_RD04_IN

P137 MUX21ND P6 CLK D Q̄ DFFNNQ R16 MUX21ND PIN_DB3_OUT
RAM_A_DOUT RAM_B_DOUT

N17 MUX21ND CH3_ACTIVE PIN_RD03_IN

P136 MUX21ND P9 CLK D Q̄ DFFNNQ R15 MUX21ND PIN_DB2_OUT
RAM_A_DOUT RAM_B_DOUT

N16 MUX21ND CH2_ACTIVE PIN_RD02_IN

P135 MUX21ND P10 CLK D Q̄ DFFNNQ R14 MUX21ND PIN_DB1_OUT
RAM_A_DOUT RAM_B_DOUT

N15 MUX21ND CH1_ACTIVE PIN_RD01_IN

P134 MUX21ND P11 CLK D Q̄ DFFNNQ R13 MUX21ND PIN_DB0_OUT
RAM_A_DOUT RAM_B_DOUT

N14 MUX21ND CH0_ACTIVE PIN_RD00_IN

PIN_DB7_IN_BUF R91 INV PIN_DB7_IN_INV
PIN_DB6_IN_BUF R95 INV PIN_DB6_IN_INV
PIN_DB5_IN_BUF R94 INV PIN_DB5_IN_INV
PIN_DB4_IN_BUF R93 INV PIN_DB4_IN_INV
PIN_DB3_IN_BUF R90 INV PIN_DB3_IN_INV
PIN_DB2_IN_BUF R92 INV PIN_DB2_IN_INV
PIN_DB1_IN_BUF R96 INV PIN_DB1_IN_INV
PIN_DB0_IN_BUF S88 INV PIN_DB0_IN_INV

PIN_DB7_IN_BUF AC53 INV PIN_DB7_IN_INV2 PIN_DB7_IN J46 BUF PIN_DB7_IN_BUF
PIN_DB6_IN_BUF AC54 INV PIN_DB6_IN_INV2 PIN_DB6_IN R3 BUF PIN_DB6_IN_BUF
PIN_DB5_IN_BUF AC57 INV PIN_DB5_IN_INV2 PIN_DB5_IN S24 BUF PIN_DB5_IN_BUF
PIN_DB4_IN_BUF AC56 INV PIN_DB4_IN_INV2 PIN_DB4_IN S23 BUF PIN_DB4_IN_BUF
PIN_DB3_IN_BUF AC60 INV PIN_DB3_IN_INV2 PIN_DB3_IN S18 BUF PIN_DB3_IN_BUF
PIN_DB2_IN_BUF AC55 INV PIN_DB2_IN_INV2 PIN_DB2_IN S22 BUF PIN_DB2_IN_BUF
PIN_DB1_IN_BUF AC67 INV PIN_DB1_IN_INV2 PIN_DB1_IN S21 BUF PIN_DB1_IN_BUF
PIN_DB0_IN_BUF AC61 INV PIN_DB0_IN_INV2 PIN_DB0_IN S9 BUF PIN_DB0_IN_BUF

PIN_DB5_IN_BUF P18 INV PIN_DB5_IN_INV3
PIN_DB4_IN_BUF R23 INV PIN_DB4_IN_INV3
PIN_DB2_IN_BUF P19 INV PIN_DB2_IN_INV3
PIN_DB0_IN_BUF V26 INV PIN_DB0_IN_INV3

PIN_NCS PIN_NRD S86 OR_2 PIN_DB_DIR

Internal RAM write pulse gen
From internal source

Internal RAM write pulse gen
From CPU access source

Sub-clk pulse gen ?

Select between CPU or internal access

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EXT MEM ADDRESS
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EXT DATA REGISTERS

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EXT MEM CONTROL schematic diagram (page 12/54)

Registers 200~22F

PIN_AB09 — R76 INV
PIN_NCS — R75 NOR_2 — CPU_REGS
R75

PIN_AB03 — S54 INV — S81 INV
PIN_AB04 — S69 INV — S74 INV
PIN_AB05 — S55 INV — S73 INV

PIN_NWR

S75 011xxx 18~1F — NAND_4 — S90 NOR_2 — WR181F
S76 001xxx 08~0F — NAND_4 — S84 NOR_2 — WR080F
S77 101xxx 28~2F — NAND_4 — S77 — V83 NOR_2 — WR282F
S78 000xxx 00~07 — NAND_4 — S85 NOR_2 — WR0007
S79 100xxx 20~27 — NAND_4 — S89 NOR_2 — WR2027
S80 010xxx 10~17 — NAND_4 — S83 NOR_2 — WR1017

PIN_AB00 — W73 INV — W79 INV
PIN_AB01 — V84 INV — V92 INV
PIN_AB02 — W68 INV — W77 INV
WR282F

V91 101111 2F — NAND_4 — WR22F
W81 101110 2E — NAND_4 — WR22E
V95 101101 2D — NAND_4 — ACCESS22D
S77 — V94 INV
W70 101011 2B — NAND_4 — WR22B
W74 101010 2A — NAND_4 — WR22A
W69 101001 29 — NAND_4 — WR229
W75 101000 28 — NAND_4 — WR228

PIN_AB00 — AA126 INV — AA138 INV
PIN_AB01 — AA127 INV — AA137 INV
PIN_AB02 — AA125 INV — AA136 INV
WR181F
AA133 011111 1F — NAND_4 — WR21F
AA135 011110 1E — NAND_4 — WR21E
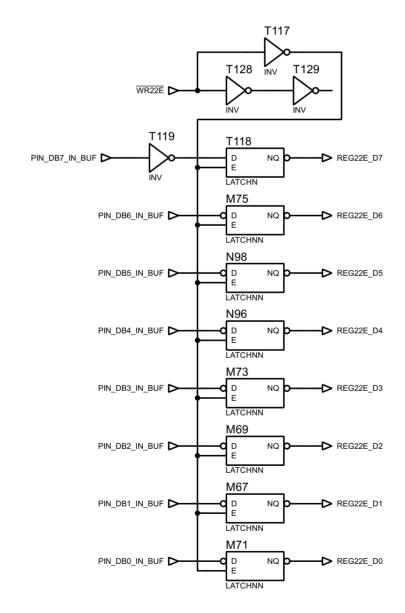AA132 011101 1D — NAND_4 — WR21D
AA134 011100 1C — NAND_4 — WR21C
AA129 011011 1B — NAND_4 — WR21B
AA131 011010 1A — NAND_4 — WR21A
AA128 011001 19 — NAND_4 — WR219
AA130 011000 18 — NAND_4 — WR218

PIN_AB00 — W82 INV — X73 INV
PIN_AB01 — W83 INV — X97 INV
PIN_AB02 — X95 INV — X101 INV
WR2027
X87 101111 27 — NAND_4 — WR227
X91 101101 25 — NAND_4 — WR225
X75 101100 24 — NAND_4 — WR224
X93B 101011 23 — NAND_4 — WR223
X74 101010 22 — NAND_4 — WR222
X90 101001 21 — NAND_4 — WR221
X76 101000 20 — NAND_4 — WR220

PIN_AB00 — R77 INV — T55 INV
PIN_AB01 — R78 INV — S82 INV
PIN_AB02 — R81 INV — R80 INV
WR1017
T61 010111 17 — NAND_4 — WR217
T56 010110 16 — NAND_4 — WR216
T60 010101 15 — NAND_4 — WR215
T54 010100 14 — NAND_4 — WR214
T62 010011 13 — NAND_4 — WR213
T58 010010 12 — NAND_4 — WR212
T59 010001 11 — NAND_4 — WR211
T57 010000 10 — NAND_4 — WR210

PIN_AB00 — AA88 INV — AA78 INV
PIN_AB01 — AA81 INV — AA77 INV
PIN_AB02 — AA85 INV — AA75 INV
WR0007
AA55 000111 07 — NAND_4 — WR207
AA72 000110 06 — NAND_4 — WR206
AA60 000101 05 — NAND_4 — WR205
AA70 000100 04 — NAND_4 — WR204
AA58 000011 03 — NAND_4 — WR203
AA67 000010 02 — NAND_4 — WR202
AA63 000001 01 — NAND_4 — WR201
AA65 000000 00 — NAND_4 — WR200

PIN_AB00 — Z51 INV — Y49 INV
PIN_AB01 — AA53 INV — AA84 INV
PIN_AB02 — AA87 INV — AA86 INV
WR080F
Z49 001111 0F — NAND_4 — WR20F
Y48 001110 0E — NAND_4 — WR20E
Z37 001101 0D — NAND_4 — WR20D
Y46A 001100 0C — NAND_4 — WR20C
Y30 001011 0B — NAND_4 — WR20B
Y47 001010 0A — NAND_4 — WR20A
W30 001001 09 — NAND_4 — WR209
Y45 001000 08 — NAND_4 — WR208

Konami 054539
REGS 200~20F EVEN

Schematic sheet — signal labels by block:

Top-left block (WR203 / REG203)
- AA6, AA10, AA9 (INV), AA19 (INV), AA25 (DFFSR: D, SET, RESET, CLK; V38A, AA27_Q, VCC, M3) → AA25_NQ
- WR203, PIN_DB5_IN_INV3, AA2 (LATCHN: D, E, NQ) → REG203_D5
- Z3 (LATCHN) → REG203_D4
- AA27_Q, AA23 (AND_2), VCC, AA24 (DFFR: CLK, D, R, Q, Q̄)
- PIN_DB2_IN_INV3, AA11 (LATCHN), AA22 (NAND_2), AA21 (NAND_2), AA20 (OR_2) → AA20
- PIN_DB0_IN_INV3, X6 (DFFNNQ: CLK, D̄, Q̄), X7 (INV) → REG203_D0

Top-right block (WR201 / REG201)
- AA4, AA8, AA7 (INV), W11 (INV), W15 (DFFSR; V38A, W16_Q, VCC, M4) → W15_NQ
- WR201, PIN_DB5_IN_INV3, Z6 (LATCHN) → REG201_D5
- Z2 (LATCHN) → REG201_D4
- W16_Q, W13 (AND_2), VCC, W14 (DFFR)
- PIN_DB2_IN_INV3, Z7 (LATCHN), W12B (NAND_2), W12A (NAND_2), W11B (OR_2) → W11B
- PIN_DB0_IN_INV3, W6 (DFFNNQ), W5 (INV) → REG201_D0

Second-left block (WR207 / REG207)
- N3, T22, T21 (INV), T12 (INV), T18 (DFFSR; V38A, X19_Q, VCC, M7) → T18_NQ
- WR207, PIN_DB5_IN_INV3, T4 (LATCHN) → REG207_D5
- S17 (LATCHN) → REG207_D4
- X19_Q, T16 (AND_2), VCC, T17 (DFFR)
- PIN_DB2_IN_INV3, S25 (LATCHN), T15 (NAND_2), T14 (NAND_2), T13 (OR_2) → T13
- PIN_DB0_IN_INV3, S27 (DFFNNQ), S26 (INV) → REG207_D0

Second-right block (WR205 / REG205)
- P42, P44, P43 (INV), R40 (INV), R35 (DFFSR; V38A, S35_Q, VCC, M6) → R35_NQ
- WR205, PIN_DB5_IN_INV3, S19 (LATCHN) → REG205_D5
- S16 (LATCHN) → REG205_D4
- S35_Q, R37 (AND_2), VCC, R36 (DFFR)
- PIN_DB2_IN_INV3, N1 (LATCHN), R38 (NAND_2), R39A (NAND_2), R39B (OR_2) → R39B
- PIN_DB0_IN_INV3, S41 (DFFNNQ), S42 (INV) → REG205_D0

Third-left block (WR20B / REG20B)
- X3, S13, S12 (INV), S28 (INV), S34 (DFFSR; V38A, X20_Q, VCC, M1) → S34_NQ
- WR20B, PIN_DB5_IN_INV3, Y5 (LATCHN) → REG20B_D5
- Y1 (LATCHN) → REG20B_D4
- X20_Q, S32 (AND_2), VCC, S33 (DFFR)
- PIN_DB2_IN_INV3, S20 (LATCHN), S31 (NAND_2), S30 (NAND_2), S29 (OR_2) → S29
- PIN_DB0_IN_INV3, S15 (DFFNNQ), S14 (INV) → REG20B_D0

Third-right block (WR209 / REG209)
- R28, R25, R24 (INV), N10 (INV), N4 (DFFSR; V38A, Z15_Q, VCC, M2) → N4_NQ
- WR209, PIN_DB5_IN_INV3, R22 (LATCHN) → REG209_D5
- R21 (LATCHN) → REG209_D4
- Z15_Q, N6 (AND_2), VCC, N5 (DFFR)
- PIN_DB2_IN_INV3, R29 (LATCHN), N7 (NAND_2), N8 (NAND_2), N9 (OR_2) → N9
- PIN_DB0_IN_INV3, R26 (DFFNNQ), R27 (INV) → REG209_D0

Bottom-left block (WR20F / REG20F)
- AA5, V6, V7 (INV), Y44 (INV), Y38 (DFFSR; V38A, V18_Q, VCC, M6) → Y38_NQ
- WR20F, PIN_DB5_IN_INV3, Z5 (LATCHN) → REG20F_D5
- Z1 (LATCHN) → REG20F_D4
- V18_Q, Y40 (AND_2), VCC, Y39 (DFFR)
- PIN_DB2_IN_INV3, Y8 (LATCHN), Y41 (NAND_2), Y42 (NAND_2), Y43 (OR_2) → Y43
- PIN_DB0_IN_INV3, V8 (DFFNNQ), V11 (INV) → REG20F_D0

Bottom-right block (WR20D / REG20D)
- Z4, T2, T1 (INV), Y31 (INV), Y37 (DFFSR; V38A, Z25_Q, VCC, M6) → Y37_NQ
- WR20D, PIN_DB5_IN_INV3, Y6 (LATCHN) → REG20D_D5
- Y2 (LATCHN) → REG20D_D4
- Z25_Q, Y35 (AND_2), VCC, Y36 (DFFR)
- PIN_DB2_IN_INV3, Y7 (LATCHN), Y34 (NAND_2), Y33 (NAND_2), Y32 (OR_2) → Y32
- PIN_DB0_IN_INV3, T6 (DFFNNQ), T5 (INV) → REG20D_D0

AH85

$\overline{WR225}$ ▷ —— BUF

V77

$\overline{WR22F}$ ▷ —— CLK
PIN_DB0_IN_BUF ▷ —— D0   Q0 —— ▷ REG22F_D0
PIN_DB1_IN_BUF ▷ —— D1   Q1 —— ▷ REG22F_D1
PIN_DB4_IN_BUF ▷ —— D2   Q2 —— ▷ REG22F_D4
PIN_DB5_IN_BUF ▷ —— D3   Q3 —— ▷ REG22F_D5
DFF4Q

V78
PIN_DB7_IN_BUF ▷ —— D   Q —— ▷ REG22F_D7
E   NQ
$\overline{RES}$ ▷ —— R
LATCHR

AH83
PIN_DB5_IN_BUF ▷ —— D   Q —— ▷ REG225_D5
E   NQ
LATCHL

AH82
PIN_DB4_IN_BUF ▷ —— D   Q —— ▷ REG225_D4
E   NQ
LATCHL

AH91
PIN_DB1_IN_BUF ▷ —— D   Q
E
LATCHL

AH89
PIN_DB0_IN_BUF ▷ —— D   Q
E   NQ
LATCHL

CLKDIV64_BUF2 ▷

AH90
A   Z
B
S
MUX21N

AH92
—— INV —— ▷ AH92

T117
INV

T128   T129
$\overline{WR22E}$ ▷ —— INV —— INV

T119
PIN_DB7_IN_BUF ▷ —— INV
T118
D   NQ —— ▷ REG22E_D7
E
LATCHN

M75
PIN_DB6_IN_BUF ▷ —— D   NQ —— ▷ REG22E_D6
E
LATCHNN

N98
PIN_DB5_IN_BUF ▷ —— D   NQ —— ▷ REG22E_D5
E
LATCHNN

N96
PIN_DB4_IN_BUF ▷ —— D   NQ —— ▷ REG22E_D4
E
LATCHNN

M73
PIN_DB3_IN_BUF ▷ —— D   NQ —— ▷ REG22E_D3
E
LATCHNN

M69
PIN_DB2_IN_BUF ▷ —— D   NQ —— ▷ REG22E_D2
E
LATCHNN

M67
PIN_DB1_IN_BUF ▷ —— D   NQ —— ▷ REG22E_D1
E
LATCHNN

M71
PIN_DB0_IN_BUF ▷ —— D   NQ —— ▷ REG22E_D0
E
LATCHNN

AB110
INV

AB115   AB114
$\overline{WR224}$ ▷ —— INV —— INV

AB112
PIN_DB6_IN_BUF ▷ —— D   NQ —— ▷ REG224_D6
E
LATCHNN

AB92
PIN_DB5_IN_BUF ▷ —— D   NQ —— ▷ REG224_D5
E
LATCHNN

AB97
PIN_DB4_IN_BUF ▷ —— D   NQ —— ▷ REG224_D4
E
LATCHNN

AB108
PIN_DB3_IN_BUF ▷ —— D   NQ —— ▷ REG224_D3
E
LATCHNN

AB106
PIN_DB2_IN_BUF ▷ —— D   NQ —— ▷ REG224_D2
E
LATCHNN

AB93
PIN_DB1_IN_BUF ▷ —— D   NQ —— ▷ REG224_D1
E
LATCHNN

AB95
PIN_DB0_IN_BUF ▷ —— D   NQ —— ▷ REG224_D0
E
LATCHNN

AB58
AB60 INV AB59
WR21D
INV INV

AG39 — D NQ — REG21D_D7 — E LATCHN — PIN_DB7_IN_INV2
AH39 — D NQ — REG21D_D6 — E LATCHN — PIN_DB6_IN_INV2
AG38 — D NQ — REG21D_D5 — E LATCHN — PIN_DB5_IN_INV2
AG37 — D NQ — REG21D_D4 — E LATCHN — PIN_DB4_IN_INV2
AH51 — D NQ — REG21D_D3 — E LATCHN — PIN_DB3_IN_INV2
AG36 — D NQ — REG21D_D2 — E LATCHN — PIN_DB2_IN_INV2
AG35 — D NQ — REG21D_D1 — E LATCHN — PIN_DB1_IN_INV2
AF58 — D NQ — REG21D_D0 — E LATCHN — PIN_DB0_IN_INV2

AB55
AB57 INV AB56
WR21E
INV INV

AC52 — REG21E_D7 — PIN_DB7_IN_INV2
AC58 — REG21E_D6 — PIN_DB6_IN_INV2
AC46 — REG21E_D5 — PIN_DB5_IN_INV2
AC49 — REG21E_D4 — PIN_DB4_IN_INV2
AC48 — REG21E_D3 — PIN_DB3_IN_INV2
AC47 — REG21E_D2 — PIN_DB2_IN_INV2
AC63 — REG21E_D1 — PIN_DB1_IN_INV2
AC65 — REG21E_D0 — PIN_DB0_IN_INV2

AB61
AB63 INV AB62
WR21F
INV INV

AG44 — REG21F_D7 — PIN_DB7_IN_INV2
AH40 — REG21F_D6 — PIN_DB6_IN_INV2
AG43 — REG21F_D5 — PIN_DB5_IN_INV2
AG42 — REG21F_D4 — PIN_DB4_IN_INV2
AH38 — REG21F_D3 — PIN_DB3_IN_INV2
AG41 — REG21F_D2 — PIN_DB2_IN_INV2
AG40 — REG21F_D1 — PIN_DB1_IN_INV2
AF59 — REG21F_D0 — PIN_DB0_IN_INV2

AB67
AB69 INV AB68
WR220
INV INV

AC51 — REG220_D7 — PIN_DB7_IN_INV2
AC50 — REG220_D6 — PIN_DB6_IN_INV2
AC62 — REG220_D5 — PIN_DB5_IN_INV2
AC59 — REG220_D4 — PIN_DB4_IN_INV2
AE49 — REG220_D3 — PIN_DB3_IN_INV2
AE46 — REG220_D2 — PIN_DB2_IN_INV2
AE59 — REG220_D1 — PIN_DB1_IN_INV2
AD63 — REG220_D0 — PIN_DB0_IN_INV2

AB118
AB126 INV AB125
WR221
INV INV

AH73 — REG221_D7 — PIN_DB7_IN_INV2
AH71 — REG221_D6 — PIN_DB6_IN_INV2
AE76 — REG221_D5 — PIN_DB5_IN_INV2
AD105 — REG221_D4 — PIN_DB4_IN_INV2
AD103 — REG221_D3 — PIN_DB3_IN_INV2
AD102 — REG221_D2 — PIN_DB2_IN_INV2
AD104 — REG221_D1 — PIN_DB1_IN_INV2
AC85 — REG221_D0 — PIN_DB0_IN_INV2

AB64
AB65 INV AB66
WR216
INV INV

AG49 — REG216_D7 — PIN_DB7_IN_INV2
AG34 — REG216_D6 — PIN_DB6_IN_INV2
AG48 — REG216_D5 — PIN_DB5_IN_INV2
AG47 — REG216_D4 — PIN_DB4_IN_INV2
AH52 — REG216_D3 — PIN_DB3_IN_INV2
AG46 — REG216_D2 — PIN_DB2_IN_INV2
AG45 — REG216_D1 — PIN_DB1_IN_INV2
AF60 — REG216_D0 — PIN_DB0_IN_INV2

AB73
AB75 INV AB74
WR217
INV INV

AE52 — REG217_D7 — PIN_DB7_IN_INV2
AE48 — REG217_D6 — PIN_DB6_IN_INV2
AE41 — REG217_D5 — PIN_DB5_IN_INV2
AE51 — REG217_D4 — PIN_DB4_IN_INV2
AE50 — REG217_D3 — PIN_DB3_IN_INV2
AE47 — REG217_D2 — PIN_DB2_IN_INV2
AC64 — REG217_D1 — PIN_DB1_IN_INV2
AC66 — REG217_D0 — PIN_DB0_IN_INV2

AB70
AB72 INV AB71
WR218
INV INV

AG54 — REG218_D7 — PIN_DB7_IN_INV2
AH50 — REG218_D6 — PIN_DB6_IN_INV2
AG53 — REG218_D5 — PIN_DB0_IN_INV2
AG52 — REG218_D4 — PIN_DB4_IN_INV2
AH53 — REG218_D3 — PIN_DB3_IN_INV2
AG51 — REG218_D2 — PIN_DB2_IN_INV2
AG50 — REG218_D1 — PIN_DB1_IN_INV2
AF61 — REG218_D0 — PIN_DB0_IN_INV2

AB76
AB78 INV AB77
WR219
INV INV

AF53 — REG219_D7 — PIN_DB7_IN_INV2
AF51 — REG219_D6 — PIN_DB6_IN_INV2
AF55 — REG219_D5 — PIN_DB5_IN_INV2
AF54 — REG219_D4 — PIN_DB4_IN_INV2
AE58 — REG219_D3 — PIN_DB3_IN_INV2
AE64 — REG219_D2 — PIN_DB2_IN_INV2
AE65 — REG219_D1 — PIN_DB1_IN_INV2
AF56 — REG219_D0 — PIN_DB0_IN_INV2

AB85
AB82 INV AB81
WR21A
INV INV

AD85 — REG21A_D7 — PIN_DB7_IN_INV2
AD84 — REG21A_D6 — PIN_DB6_IN_INV2
AD79 — REG21A_D5 — PIN_DB5_IN_INV2
AD70 — REG21A_D4 — PIN_DB4_IN_INV2
AC69 — REG21A_D3 — PIN_DB3_IN_INV2
AC68 — REG21A_D2 — PIN_DB2_IN_INV2
AC73 — REG21A_D1 — PIN_DB1_IN_INV2
AC72 — REG21A_D0 — PIN_DB0_IN_INV2

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MULA A INPUTS
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External memory
address up-counter
for CPU access

Channel volume
and
Reverb volume ?

K50

B69 BUF
B56 INV
B58 INV
B55 INV
B72 BUF
C64 INV
C61 INV
C62 INV

TESTREG1_D3
A106 INV
A96 INV
TRIGE
C71 INV
B73 INV

MUX_A_D7 — C76 LATCHN — B76 MUX21ND — PIN_RD07_IN — A84 MUX21D — MULA_A7
MUX_B_D7 — B83 LATCHN
MUX_A_D6 — C75 LATCHN — B68 MUX21ND — PIN_RD06_IN — A82 MUX21D — MULA_A6
MUX_B_D6 — B65 LATCHN
MUX_A_D5 — C74 LATCHN — B67 MUX21ND — PIN_RD05_IN — A80 MUX21D — MULA_A5
MUX_B_D5 — B59 LATCHN
MUX_A_D4 — C73 LATCHN — B66 MUX21ND — PIN_RD04_IN — A78 MUX21D — MULA_A4
MUX_B_D4 — B61 LATCHN
MUX_A_D3 — C70 LATCHN — B75 MUX21ND — PIN_RD03_IN — A94 MUX21D — MULA_A3
MUX_B_D3 — B64 LATCHN
MUX_A_D2 — B60 LATCHN — B71 MUX21ND — PIN_RD02_IN — A90 MUX21D — MULA_A2
MUX_B_D2 — B80 LATCHN
MUX_A_D1 — B62 LATCHN — B70 MUX21ND — PIN_RD01_IN — A88 MUX21D — MULA_A1
MUX_B_D1 — B79 LATCHN
MUX_A_D0 — B81 LATCHN — B78 MUX21ND — PIN_RD00_IN — A86 MUX21D — MULA_A0
MUX_B_D0 — B82 LATCHN

AJ130
AR39 INV
AP21 INV — AP22 INV
AR40 INV
AP24 INV — AP23 INV

J64 — AJ63 INV — AJ64 INV — AJ62 INV

MUX_B_D7 — AJ81 LATCHNN — AP40 DFFNNQ — AP40
MUX_B_D6 — AJ73 LATCHNN — AP20 DFFNNQ — AP20
MUX_B_D5 — AJ69 LATCHNN — AN28 DFFNNQ — AN28
MUX_B_D4 — AJ67 LATCHNN — AN27 DFFNNQ — AN27
MUX_B_D3 — AJ79 LATCHNN — AP39 DFFNNQ — AP39
MUX_B_D2 — AJ71 LATCHNN — AP26 DFFNNQ — AP26
MUX_B_D1 — AJ65 LATCHNN — AN26 DFFNNQ — AN26
MUX_B_D0 — AJ77 LATCHNN — AP25 DFFNNQ — AP25

CLKDIV2D_2 — AB90 BUF — AB91 INV
AJ106 DFF — AJ106
AB167

AF44 DFF — SRA11
AF49 DFF — SRA10
AF50 DFF — SRA9
AJ1 DFF — SRA8
AJ2 DFF
AJ105 DFF — SRA6
AH112 DFF — SRA5
AH113 DFF — SRA4
AH114 DFF — SRA3
AH115 DFF
AK77 DFF — SRA1
AK76 DFF — SRA0
AJ117 INV
AJ114 DFF — AJ114
AB167 DFF — AB167

CLKDIV4 — AB128 BUF
CLKDIV8 — AB124 BUF
CLKDIV16 — AB164 BUF
CLKDIV32 — AB163 BUF
AB166 NAND_4
CLKDIV4_BUF
CLKDIV8_BUF

REG22F_D4 — N78 BUF
ACCESS22D — T96 INV
CLKDIV2D_3 — N71 INV
TESTREG2_D3
T95 MUX21N

T94 DFFR — ADDRCNT0
T90 DFFR — ADDRCNT1
T85 DFFR — ADDRCNT2
T86 DFFR — ADDRCNT3
S116 MUX21N
S117 DFFR — ADDRCNT4
S118 DFFR — ADDRCNT5
S119 DFFR — ADDRCNT6
S120 DFFR — ADDRCNT7
R111 MUX21N
R112 DFFR — ADDRCNT8
P80 DFFR — ADDRCNT9
P79 DFFR — ADDRCNT10
P78 DFFR — ADDRCNT11
N73 MUX21N
N72 DFFR — ADDRCNT12
M55 DFFR — ADDRCNT13
M56 DFFR — ADDRCNT14
M50 DFFR — ADDRCNT15
M49 DFFR — ADDRCNT16

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D66
CLKDIV4D_5
CLKDIV16D_3
AND_2

D65
CLKDIV32D
OR_2

D64
AND_2

D62
CLKDIV2D_2
CLK
D
Q
Q
DFF
D62

D63
CLKDIV4D_5
CLKDIV32D_3
OR_2

D11
TRIGA
TRIGJ
NAND_2

D10
BUF
D10

D12A
OR_2
D12A

D12B
TRIGF
INV

D14
BUF
D14

MULA — MUL161632

A0	Z0
A1	Z1
A2	Z2
A3	Z3
A4	Z4
A5	Z5
A6	Z6
A7	Z7
A8	Z8
A9	Z9
A10	Z10
A11	Z11
A12	Z12
A13	Z13
A14	Z14
A15	Z15
	Z16
B0	Z17
B1	Z18
B2	Z19
B3	Z20
B4	Z21
B5	Z22
B6	Z23
B7	Z24
B8	Z25
B9	Z26
B10	Z27
B11	Z28
B12	Z29
B13	Z30
B14	Z31
B15	

MULA_A0–MULA_A7, MULA_B0–MULA_B15, GND
MULA_OUT0–MULA_OUT23

MULB — MUL161632

MULB_A0–MULB_A9, MULB_A10–MULB_A15, MULB_B0–MULB_B15
MULB_OUT0–MULB_OUT15

ROMA — ROM7_9

A0	D0
A1	D1
A2	D2
A3	D3
A4	D4
A5	D5
A6	D6
A7	
A8	
CK	

ROMA_A0–ROMA_A8, ROMA_CLK
ROMA_D0–ROMA_D6

ROMB — ROM16_8

A0	D0
A1	D1
A2	D2
A3	D3
A4	D4
A5	D5
A6	D6
A7	D7
	D8
	D9
	D10
	D11
	D12
	D13
	D14
	D15
CK	

ROMB_A0–ROMB_A7, CLKDIV2D_5
ROMB_D0–ROMB_D15

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CLKDIV8_BUF — H80 INV
CLKDIV4_BUF — H69 NOR_2
CLKDIV2_BUF — H70 NOR_2
E73 INV — H69
E74 INV — H70

CLK_BUF — L83 INV — L89 INV
L82 INV — CLK_BUF3

ROMA_A1, ROMA_A2 — T97A OR_2
ROMA_A3 — T97B AND_2
T98 INV — S122 INV — S122

PIN_AXXA, PIN_AXDA — G99 DFF (CLK, D, Q, Q̄) — F102 BUF — AXDA_SYNC

PIN_AXXA — D120 INV — D123 INV — D124 INV
PIN_YMD — C131 INV — C130 INV
PIN_AXWA
PIN_ALRA — C127B INV — C127A AND_2
C126 AND_2

B128 MUX21D (A, B, Z, S, S̄)
B130 MUX21D (A, B, Z, S, S̄)
C128 MUX21D (A, B, Z, S, S̄)

CLK_BUF — A139 DFF (CLK, D, Q, Q̄) — E110 DFF (CLK, D, Q, Q̄) — E110
B132 DFF — J108 INV — J108
D121 DFF — D122 INV — D122

AB103A — AA121 INV
AC74_Q0T — AA120 NOR_2

SRA0
CLKDIV128D_3
CLKDIV512D
CLKDIV64D — AH107 OR_4
CLKDIV128D_4 — AH103 OR_4
AH108 OR_2 — AH108
AH104 OR_2 — AH104

CLKDIV128_BUF — W87 BUF
REG224_D3 — W90 AND_2
REG22F_D4
CLKDIV16D_4
PIN_DLY — W91 NOR_4
W92 DFFR (CLK, D, R, Q, Q̄)
RES
CLKDIV512D3
W93 OR_2 — W93

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F101
INV

H100   H101
INV   INV

G104
INV
H87   H86
INV   INV
E110

G114
INV
H102   H103
INV   INV
D122

K99
INV
J109   J110
INV   INV
J108

L106   L124
INV   INV
ROMA_A5

Ref	Type		Ref	Type	Output

G112 DFFNNQ   H93 DFFNNQ   L129 MUX21ND   L130 BUF   AXWORD7
AXDMUX7
G110 DFFNNQ   H94 DFFNNQ

J106 DFFNNQ   J102 DFFNNQ   L128 MUX21ND   L127 BUF   AXWORD6
AXDMUX6
H97 DFFNNQ   H92 DFFNNQ

A135 DFFNNQ   F114 DFFNNQ   L126 MUX21ND   L125 BUF   AXWORD5
AXDMUX5
A132 DFFNNQ   H95 DFFNNQ

A125 DFFNNQ   F100 DFFNNQ   L107 MUX21ND   L108 BUF   AXWORD4
AXDMUX4
A127 DFFNNQ   H85 DFFNNQ

A130 DFFNNQ   F108 DFFNNQ   L117 MUX21ND   L116 BUF   AXWORD3
AXDMUX3
A131 DFFNNQ   K96 DFFNNQ

A129 DFFNNQ   H83 DFFNNQ   L122 MUX21ND   L123 BUF   AXWORD2
AXDMUX2
A128 DFFNNQ   K93 DFFNNQ

A136 DFFNNQ   G107 DFFNNQ   L133 MUX21ND   L134 BUF   AXWORD1
AXDMUX1
A133 DFFNNQ   K97 DFFNNQ

A137 DFFNNQ   G108 DFFNNQ   L131 MUX21ND   L132 BUF   AXWORD0
AXDMUX0
A134 DFFNNQ   K98 DFFNNQ

F107 DFFNNQ   F106 DFFNNQ   K81 MUX21ND   K80 BUF   AXWORD15
AXDMUX15
G100 DFFNNQ   H84 DFFNNQ

G111 DFFNNQ   K94 DFFNNQ   K86 MUX21ND   K85 BUF   AXWORD14
AXDMUX14
G109 DFFNNQ   H88 DFFNNQ

J105 DFFNNQ   J100 DFFNNQ   K92 MUX21ND   K91 BUF   AXWORD13
AXDMUX13
H96 DFFNNQ   H91 DFFNNQ

G106 DFFNNQ   J99 DFFNNQ   K79 MUX21ND   K78 BUF   AXWORD12
AXDMUX12
G105 DFFNNQ   J95 DFFNNQ

F109 DFFNNQ   J93 DFFNNQ   L118 MUX21ND   L119 BUF   AXWORD11
AXDMUX11
G101 DFFNNQ   J96 DFFNNQ

J103 DFFNNQ   J101 DFFNNQ   L121 MUX21ND   L120 BUF   AXWORD10
AXDMUX10
H89 DFFNNQ   J97 DFFNNQ

G103 DFFNNQ   J94 DFFNNQ   K83 MUX21ND   K82 BUF   AXWORD9
AXDMUX9
G102 DFFNNQ   J98 DFFNNQ

J104 DFFNNQ   K95 DFFNNQ   K88 MUX21ND   K87 BUF   AXWORD8
AXDMUX8
H90 DFFNNQ   K90 DFFNNQ

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AUX DATA LATCHES

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START/STOP

CLKDIV256D_3 — S50 (INV) — Z27 (INV)

CLKDIV128D_3 — AA44 (INV) — AA43 (INV)

CLKDIV64D_3 — AA74 (INV) — Z47 (INV)

REG207_D0, T18_NQ — T11 (NAND_2)

REG205_D0, R35_NQ — S40 (NAND_2)

REG203_D0, AA25_NQ — AA35 (NAND_2)

REG201_D0, W15_NQ — W18 (NAND_2)

REG20F_D0, Y38_NQ — Z50 (NAND_2)

REG20D_D0, Y37_NQ — Z44 (NAND_2)

REG20B_D0, S34_NQ — S46 (NAND_2)

REG209_D0, N4_NQ — S44 (NAND_2)

Z28 (MUX41N): D0 D1 D2 D3 S0 S1 → Z

Z30 (MUX41N): D0 D1 D2 D3 S0 S1 → Z

Z29 (MUX21ND): A B S → Z → LOOPFLAG

CLKDIV256D_3 — P27 (INV) — P24 (INV)

CLKDIV128D_3 — P26 (INV) — P20 (INV)

CLKDIV64D_3 — P41 (INV) — P25 (INV)

P23 (MUX41N): CH3_ACTIVE, CH2_ACTIVE, CH1_ACTIVE, CH0_ACTIVE → D0 D1 D2 D3, S0 S1 → Z

P21 (MUX41N): CH7_ACTIVE, CH6_ACTIVE, CH5_ACTIVE, CH4_ACTIVE → D0 D1 D2 D3, S0 S1 → Z

P22 (MUX21ND): A B S → Z → MUX_ACTIVE

V133 (INV): PIN_RRMD → PIN_RRMD

CLKDIV256D_3 — T23 (INV) — T30 (INV)

CLKDIV128D_3 — V31 (INV) — V32 (INV)

CLKDIV64D_3 — V25 (INV) — T24 (INV)

T31 (MUX41N): Y23_Q, T35_Q, Y20_Q, W26_Q → D0 D1 D2 D3, S0 S1 → Z

T33 (MUX41N): V20_Q, Z24_Q, X16_Q, Z16_Q → D0 D1 D2 D3, S0 S1 → Z

T32 (MUX21ND): A B S → Z → R88 (INV) → R88

AB111
BUF
CLKDIV128_BUF2

AB101
XOR_2

AB102
OR_2

AJ57
MUX21D
PIN_ADDA
TESTREG1_D6
A B S/O Z

Y110
AJ57

B104 INV
B105 INV
CLKDIV512T
R87 BUF
ROMA_A8

L101 INV
L100 INV
CLKDIV256
R98 BUF
ROMA_A7

CLKDIV128_BUF

L87 INV
L86 INV
CLKDIV128
R99 BUF
ROMA_A6

AJ59
MUX21D
CLKDIV64_BUF
PIN_USE2
A B S/O Z

AJ92
DEC2
A B X0 X1 X2 X3

AJ91
OR_3

AJ94
AND_2
AJ94

L96 INV
L97 INV
CLKDIV64
CLKDIV64_BUF
L90 BUF
ROMA_A5

L92 INV
CLKDIV128

AJ55
MUX21D
PIN_RRMD
A B S/O Z

AJ93
OR_3

L85 INV
L84 INV
CLKDIV32
CLKDIV32_BUF
P82 BUF
ROMA_A4

L99 INV
L98 INV
CLKDIV16
CLKDIV16_BUF
P81 BUF
ROMA_A3

L109 INV
L110 INV
CLKDIV8
CLKDIV8_BUF
T82 BUF
ROMA_A2

H75 INV
H76 INV
CLKDIV4
CLKDIV4_BUF
V98 BUF
ROMA_A1

H79 INV
H78 INV
CLKDIV2
CLKDIV2_BUF
M35 BUF
ROMA_A0

ROMB ADDRESS schematic diagram — Konami 054539

TITLE:
Konami 054539
ADDER A - FRAC
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Konami 054539

ADDER B - SAMPLE ADDRESS

R89

R69
BUF

MUX_A_D7
L9

M19
CLK
D
Q
Q̄
S
DFFSNNQ
STEP15

R62
A
B
CI
S
CO
FA1

RD_REGA7

AA40
AA47

R58
AOI22

R59
INV
MUXD15

MUX_A_D6

R68
CLK
D
Q
Q̄
S
DFFSNNQ
STEP14

R61
A
B
CI
S
CO
FA1

RD_REGA6

R56
AOI22

R57
INV
MUXD14

MUX_A_D5

R64
CLK
D
Q
Q̄
S
DFFSNNQ
STEP13

R60
A
B
CI
S
CO
FA1

RD_REGA5

R55
AOI22

R54
INV
MUXD13

MUX_A_D4

S70
CLK
D
Q
Q̄
S
DFFSNNQ
STEP12

T47
A
B
CI
S
CO
FA1

RD_REGA4

T39
AOI22

T40
INV
MUXD12

MUX_A_D3

R67
CLK
D
Q
Q̄
S
DFFSNNQ
STEP11

T48
A
B
CI
S
CO
FA1

RD_REGA3

T38
AOI22

T37
INV
MUXD11

MUX_A_D2

R70
CLK
D
Q
Q̄
S
DFFSNNQ
STEP10

T49
A
B
CI
S
CO
FA1

RD_REGA2

V48
AOI22

V49
INV
MUXD10

MUX_A_D1

S71
CLK
D
Q
Q̄
S
DFFSNNQ
STEP9

T50
A
B
CI
S
CO
FA1

RD_REGA1

T45
AOI22

T46
INV
MUXD9

MUX_A_D0

S72
CLK
D
Q
Q̄
S
DFFSNNQ
STEP8

T51
A
B
CI
S
CO
FA1

RD_REGA0

R65
AOI22

R66
INV
MUXD8

MUX_B_D7

P51
CLK
D
Q
Q̄
S
DFFSNNQ
STEP7

T52
A
B
CI
S
CO
FA1

RD_REGB7

S65
AOI22

S66
INV
MUXD7

MUX_B_D6

P52
CLK
D
Q
Q̄
S
DFFSNNQ
STEP6

W38
A
B
CI
S
CO
FA1

RD_REGB6

W31
AOI22

W32
INV
MUXD6

MUX_B_D5

P53
CLK
D
Q
Q̄
S
DFFSNNQ
STEP5

W37
A
B
CI
S
CO
FA1

RD_REGB5

X27
AOI22

X28
INV
MUXD5

MUX_B_D4

P57
CLK
D
Q
Q̄
S
DFFSNNQ
STEP4

W36
A
B
CI
S
CO
FA1

RD_REGB4

X25
AOI22

X26
INV
MUXD4

MUX_B_D3

P58
CLK
D
Q
Q̄
S
DFFSNNQ
STEP3

W35
A
B
CI
S
CO
FA1

RD_REGB3

Z38
AOI22

Z39
INV
MUXD3

MUX_B_D2

P49
CLK
D
Q
Q̄
S
DFFSNNQ
STEP2

W34
A
B
CI
S
CO
FA1

RD_REGB2

X31
AOI22

X32
INV
MUXD2

MUX_B_D1

P50
CLK
D
Q
Q̄
S
DFFSNNQ
STEP1

W33
A
B
CI
S
CO
FA1

RD_REGB1

X29
AOI22

X30
INV
MUXD1

MUX_B_D0

P45
CLK
D
Q
Q̄
S
DFFSNNQ
STEP0
GND

W27
A
B
CI
S
CO
FA1

RD_REGB0

X24
AOI22

X23
INV
MUXD0

DTYPE2
DTYPE1
AA50
OR_2
AA50

TESTREG2_D2

AA49
INV

AA48
AND_2
Normal:AA50

AA40
NOR_2
AA40

AA46
INV

AA45
V38A
NOR_2
Normal:~V38A

AA47
NOR_2
AA47

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ADDER E
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LATCHES AND MUX F
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DPCM STEP
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DTYPE2 ▷— AA42 INV — S60 INV —▷ DTYPE2_BUF

DTYPE1 ▷— AA41 INV — S61 INV —▷ DTYPE1_BUF

V45 MUX41N
DPCM_STEP7 D0
DPCM_STEP6 D1
DPCM_STEP2 D2
RD_REGA2 D3
S0 S1
Z — V44 INV — STEP10

V41 MUX41N
DPCM_STEP5 D0
DPCM_STEP1 D1
RD_REGA1 D3
S0 S1
Z — V40 INV — STEP9

V42 MUX41N
DPCM_STEP4 D0
DPCM_STEP0 D1
RD_REGA0 D3
S0 S1
Z — V43 INV — STEP8

S56 MUX41N
DPCM_STEP3 D0
GND D2
RD_REGB7 D3
S0 S1
Z — S57 INV — STEP7

V46 MUX41N
DPCM_STEP6 D0
DPCM_STEP2 D2
RD_REGB6 D3
S0 S1
Z — V47 INV — STEP6

X46 MUX41N
DPCM_STEP5 D0
DPCM_STEP1 D2
RD_REGB5 D3
S0 S1
Z — X47 INV — STEP5

W29 MUX41N
DPCM_STEP4 D0
DPCM_STEP0 D1
RD_REGB4 D3
S0 S1
Z — W28 INV — STEP4

X44 MUX41N
DPCM_STEP3 D0
RD_REGB3 D3
S0
Z — X45 INV — STEP3

X42 MUX41N
DPCM_STEP2 D0
RD_REGB2 D3
S0
Z — X43 INV — STEP2

X41 MUX41N
DPCM_STEP1 D0
RD_REGB1 D3
S0
Z — X40 INV — STEP1

X39 MUX41N
DPCM_STEP0 D0
RD_REGB0 D3
S0 S1
Z — X38 INV — STEP0

Weird but STEP9 and 10 don't seem swapped

DPCM_STEP7 ▷
RD_REGA7
S63 MUX21N A B S Z — S62 INV — STEP15

DTYPE2_BUF ▷
DTYPE1_BUF ▷
S64 OR_2

DTYPE2_BUF ▷ S53 INV

S59 MUX21ND
RD_REGA6 A
DPCM_STEP6 B
DTYPE1_BUF
Z — S58 MUX21ND A B Z — STEP14

S52 MUX21ND
RD_REGA5 A
DPCM_STEP5 B
Z — S51 MUX21ND A B Z — STEP13

T42 MUX21ND
RD_REGA4 A
DPCM_STEP4 B
Z — T41 MUX21ND Z — STEP12

T43 MUX21ND
RD_REGA3 A
DPCM_STEP3 B
Z — T44 MUX21ND Z — STEP11

DTYPE2 ▷
DTYPE1 ▷
Z26 NAND_2

STEP7 ▷
V39 AND_2

V38C NOR_8
STEP6
STEP5
STEP4
STEP3
STEP2
STEP1
STEP0
— V38B INV — V38A NAND_2 —▷ V38A
Stop marker detect ?

DTYPE2 ▷— Y46B INV

STEP12 ▷— V34 AND_2
STEP13 ▷— V35 AND_2
STEP14 ▷— V33D AND_2
STEP9 ▷— V37 AND_2
STEP11 ▷— V36 AND_2
STEP10 ▷— V33C AND_2
STEP8 ▷— V33B AND_2
STEP15 ▷— V33 INV
V34B NOR_8

TITLE: Konami 054539 STEP TYPE MUX
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FINAL OUTPUT PISO

Konami 054539
ADDR OFFSET SELECT

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COMPARATORS

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Reverb volume ?

Left block signals:

CLKDIV2D_5 — AB174 INV — AB173 INV — AB168

MULB_OUT15 — AB158 DFFNNQ — MUXE14 — AB151 FA1 — ACCE14
MULB_OUT14 — AB159 DFFNNQ — MUXE13 — AB152 FA1 — ACCE13
MULB_OUT13 — AC117 DFFNNQ — MUXE12 — AD140 FA1 — ACCE12
MULB_OUT12 — AC118 DFFNNQ — MUXE11 — AD139 FA1 — ACCE11
MULB_OUT11 — AG106 DFFNNQ — MUXE10 — AD138 FA1 — ACCE10
MULB_OUT10 — AG107 DFFNNQ — MUXE9 — AD137 FA1 — ACCE9
MULB_OUT9 — AG108 DFFNNQ — MUXE8 — AD136 FA1 — ACCE8
MULB_OUT8 — AG114 DFFNNQ — MUXE7 — AD135 FA1 — ACCE7
MULB_OUT7 — AG109 DFFNNQ — MUXE6 — AF109 FA1 — ACCE6
MULB_OUT6 — AG110 DFFNNQ — MUXE5 — AF110 FA1 — ACCE5
MULB_OUT5 — AG111 DFFNNQ — MUXE4 — AF111 FA1 — ACCE4
MULB_OUT4 — AG112 DFFNNQ — MUXE3 — AF112 FA1 — ACCE3
MULB_OUT3 — AG117 DFFNNQ — MUXE2 — AF113 FA1 — ACCE2
MULB_OUT2 — AG120 DFFNNQ — MUXE1 — AF114 FA1 — ACCE1
MULB_OUT1 — AH100 DFFNNQ — MUXE0 — AG105 FA1 — ACCE0
MULB_OUT0 — AH102 DFFNNQ

AB150 FA1 — MUXE15 — ACCE15

Right block signals:

SRA0 — AS111 INV — AS112 INV — AS110

MULB_OUT15 — AS98 DFFNNQ — RD_REG2A7 — AS109 FA1 — ACCD15
MULB_OUT14 — AS99 DFFNNQ — RD_REG2A6 — AS108 FA1 — ACCD14
MULB_OUT13 — AS105 DFFNNQ — RD_REG2A5 — AS107 FA1 — ACCD13
MULB_OUT12 — AP67 DFFNNQ — RD_REG2A4 — AJ112 FA1 — ACCD12
MULB_OUT11 — AP68 DFFNNQ — RD_REG2A3 — AJ111 FA1 — ACCD11
MULB_OUT10 — AP69 DFFNNQ — RD_REG2A2 — AJ110 FA1 — ACCD10
MULB_OUT9 — AP70 DFFNNQ — RD_REG2A1 — AJ109 FA1 — ACCD9
MULB_OUT8 — AP71 DFFNNQ — RD_REG2A0 — AJ108 FA1 — ACCD8
MULB_OUT7 — AR69 DFFNNQ — RD_REG2B7 — AJ107 FA1 — ACCD7
MULB_OUT6 — AR70 DFFNNQ — RD_REG2B6 — AK80 FA1 — ACCD6
MULB_OUT5 — AR71 DFFNNQ — RD_REG2B5 — AK81 FA1 — ACCD5
MULB_OUT4 — AR72 DFFNNQ — RD_REG2B4 — AK82 FA1 — ACCD4
MULB_OUT3 — AR76 DFFNNQ — RD_REG2B3 — AK83 FA1 — ACCD3
MULB_OUT2 — AR77 DFFNNQ — RD_REG2B2 — AK84 FA1 — ACCD2
MULB_OUT1 — AR73 DFFNNQ — RD_REG2B1 — AK85 FA1 — ACCD1
MULB_OUT0 — AR74 DFFNNQ — RD_REG2B0 — AJ113 FA1 — ACCD0
GND

R4
INV

R2   R1
INV   INV

WR227

R30
D NQ
E
LATCHNN
PIN_DB7_IN_BUF

R5
D NQ
E
LATCHNN
PIN_DB6_IN_BUF

X1
D NQ
E
LATCHNN
PIN_DB5_IN_BUF

W7
D NQ
E
LATCHNN
PIN_DB4_IN_BUF

R17
D NQ
E
LATCHNN
PIN_DB3_IN_BUF

R19
D NQ
E
LATCHNN
PIN_DB2_IN_BUF

T9
D NQ
E
LATCHNN
PIN_DB1_IN_BUF

T7
D NQ
E
LATCHNN
PIN_DB0_IN_BUF

V1
D0 Q0
D1 Q1
D2 Q2
D3 Q3
ENP
ENT   RCO
CLK
LOAD
MR
COUNT163

VCC

TESTREG2_D1

R100
INV

R101
NAND_2

R102
NAND_2

R97
BUF

CLKDIV128D_5

R103
NAND_2

M40
BUF

CLKDIV2D_3

CLKDIV2D_3

T3
D0 Q0
D1 Q1
D2 Q2
D3 Q3
ENP
ENT   RCO
CLK
LOAD
MR
COUNT163

Y3   Y4
INV
REG22F_D5

NOR_2

X4
XOR_2

X5
CLK Q
D
R
DFFR
REG22F_D5

PIN_TIM

Konami 054539 — TEST REGISTERS schematic

Top logic block:
- Y98 (NOR_6): inputs TESTREG1_D5, TESTREG1_D4, TESTREG1_D3, TESTREG1_D2, TESTREG1_D1, TESTREG1_D0
- Y96 (NOR_3): inputs TESTREG2_D4, TESTREG2_D2, TESTREG2_D1
- Y97 (NAND_2): output TESTEN

Left register chain:
- Z118 (BUF): input RES
- Z126 (INV)
- Z127 (INV): input PIN_TS1
- Z128 (INV)
- Y110 (DFFRQ): PIN_RD07_IN → TESTREG1_D7
- Y106 (DFFRQ): PIN_RD06_IN → AJ54 (INV) → AJ61 (INV) → TESTREG1_D6
- Y101 (DFFRQ): PIN_RD05_IN → TESTREG1_D5
- Y102 (DFFRQ): PIN_RD04_IN → TESTREG1_D4
- Y103 (DFFRQ): PIN_RD03_IN → TESTREG1_D3
- Y104 (DFFRQ): PIN_RD02_IN → TESTREG1_D2
- Y105 (DFFRQ): PIN_RD01_IN → TESTREG1_D1
- Y112 (DFFRQ): PIN_RD00_IN → Y111 (BUF) → TESTREG1_D0

Right register chain:
- AA151 (BUF): input RES
- AA142 (INV)
- AA1145 (INV): input PIN_TS2
- AA144 (INV)
- AA141 (DFFRQ): PIN_RD07_IN → TESTREG2_D7
- AA143 (DFFRQ): PIN_RD06_IN → TESTREG2_D6
- Z119 (DFFRQ): PIN_RD05_IN → P68 (INV) → TESTREG2_D5
- AA139 (DFFRQ): PIN_RD04_IN → TESTREG2_D4
- Z120 (DFFRQ): PIN_RD03_IN → TESTREG2_D3
- AA140 (DFFRQ): PIN_RD02_IN → TESTREG2_D2
- Z121 (DFFRQ): PIN_RD01_IN → TESTREG2_D1
- Z116 (DFFRQ): PIN_RD00_IN → Z115 (BUF) → Z185 (INV) → X143 (INV) → TESTREG2_D0

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TEST REGISTERS
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TESTREG2_D6

AE117 INV
AE109 INV

AE112
REGEE_0 / REG202_D0
A B S Q QS
MUX21D
REGEE0T

AF107
REGEE_1 / REG202_D1
MUX21D
REGEE1T

AF99
REGEE_2 / REG202_D2
MUX21D
REGEE2T

AF101
REGEE_3 / REG202_D3
MUX21D
REGEE3T

AF97
REGEE_4 / REG202_D4
MUX21D
REGEE4T

AF115
REGEE_5 / REG202_D5
MUX21D
REGEE5T

AF103
REGEE_6 / REG202_D6
MUX21D
REGEE6T

AF105
REGEE_7 / REG202_D7
MUX21D
REGEE7T

AE97
REGEE_8 / REG200_D0
MUX21D
REGEE8T

AE107
REGEE_9 / REG200_D1
MUX21D
REGEE9T

AE114
REGEE_10 / REG200_D2
MUX21D
REGEE10T

AE95
REGEE_11 / REG200_D3
MUX21D
REGEE11T

AE99
REGEE_12 / REG200_D4
MUX21D
REGEE12T

AE101
REGEE_13 / REG200_D5
MUX21D
REGEE13T

AE103
REGEE_14 / REG200_D6
MUX21D
REGEE14T

AE105
REGEE_15 / REG200_D7
MUX21D
REGEE15T

TESTREG2_D6

AC100 INV
AC104 INV

AD126
REGEF_0 / REG206_D0
MUX21D
REGEF0T

AD133
REGEF_1 / REG206_D1
MUX21D
REGEF1T

AD131
REGEF_2 / REG206_D2
MUX21D
REGEF2T

AD128
REGEF_3 / REG206_D3
MUX21D
REGEF3T

AC107
REGEF_4 / REG206_D4
MUX21D
REGEF4T

AC95
REGEF_5 / REG206_D5
MUX21D
REGEF5T

AC97
REGEF_6 / REG206_D6
MUX21D
REGEF6T

AC109
REGEF_7 / REG206_D7
MUX21D
REGEF7T

AC101
REGEF_8 / REG204_D0
MUX21D
REGEF8T

AB138
REGEF_9 / REG204_D1
MUX21D
REGEF9T

AC105
REGEF_10 / REG204_D2
MUX21D
REGEF10T

AC94
REGEF_11 / REG204_D3
MUX21D
REGEF11T

AB129
REGEF_12 / REG204_D4
MUX21D
REGEF12T

AB131
REGEF_13 / REG204_D5
MUX21D
REGEF13T

AB133
REGEF_14 / REG204_D6
MUX21D
REGEF14T

AB136
REGEF_15 / REG204_D7
MUX21D
REGEF15T

AC165
PIN_DTCK
AC167 INV
AC168

AD161 INV
AG103
AD163 INV

AC161A
REGEF15T
MUX21ND
AC161B CLK D Q QN DFFN AC161B

AC145A
REGEF14T
MUX21ND
AC145B CLK D QN DFFN AC145B

AD164A
REGEF13T
MUX21ND
AD164B CLK D Q DFFN AD164B

AD166A
REGEF12T
MUX21ND
AD166B CLK D Q DFFN AD166B

AC147A
REGEF11T
MUX21ND
AC147B CLK D DFFN AC147B

AC160A
REGEF10T
MUX21ND
AC160B CLK D Q DFFN AC160B

AC146A
REGEE9T
MUX21ND
AC146B CLK D DFFN AC146B

AD167A
REGEE8T
MUX21ND
AD167B CLK D QN DFFN AD167B

AD171A
REGEF7T
MUX21ND
AD171B CLK D QN DFFN AD171B

AD162A
REGEF6T
MUX21ND
AD162B CLK D DFFN AD162B

AD165A
REGEF5T
MUX21ND
AD165B CLK D DFFN AD165B

AD170A
REGEF4T
MUX21ND
AD170B CLK D DFFN AD170B

AD173A
REGEF3T
MUX21ND
AD173B CLK D DFFN AD173B

AD169A
REGEF2T
MUX21ND
AD169B CLK D QN DFFN AD169B

AD172A
REGEF1T
MUX21ND
AD172B CLK D DFFN AD172B

AD168A
REGEF0T
MUX21ND
AD168B CLK D DFFN AD168B

AB100
PIN_DTCK
AF154 INV
AF155 INV

AE140 INV
AG103
AE142

AE137A
REGEE15T
MUX21ND
AE137B CLK D Q DFFN AE137B

AE136A
REGEE14T
MUX21ND
AE136B CLK D DFFN AE136B

AE135A
REGEE13T
MUX21ND
AE135B CLK D Q DFFN AE135B

AE134B
REGEE12T
MUX21ND
AE134A CLK D DFFN AE134A

AE144A
REGEE11T
MUX21ND
AE144B CLK D DFFN AE144B

AE139A
REGEE10T
MUX21ND
AE139B CLK D DFFN AE139B

AE143A
REGEE9T
MUX21ND
AE143B CLK D DFFN AE143B

AE138A
REGEE8T
MUX21ND
AE138B CLK D DFFN AE138B

AF165
REGEE7T
MUX21ND
AF164 CLK D DFFN AF164

AF159
REGEE6T
MUX21ND
AF158 CLK D DFFN AF158

AF156
REGEE5T
MUX21ND
AF157 CLK D DFFN AF157

AF162
REGEE4T
MUX21ND
AF163 CLK D DFFN AF163

AF168
REGEE3T
MUX21ND
AF169 CLK D DFFN AF169

AF160
REGEE2T
MUX21ND
AF161 CLK D DFFN AF161

AF167
REGEE1T
MUX21ND
AF166 CLK D DFFN AF166

AE141B
REGEE0T
MUX21ND
AE141A CLK D DFFN AE141A