

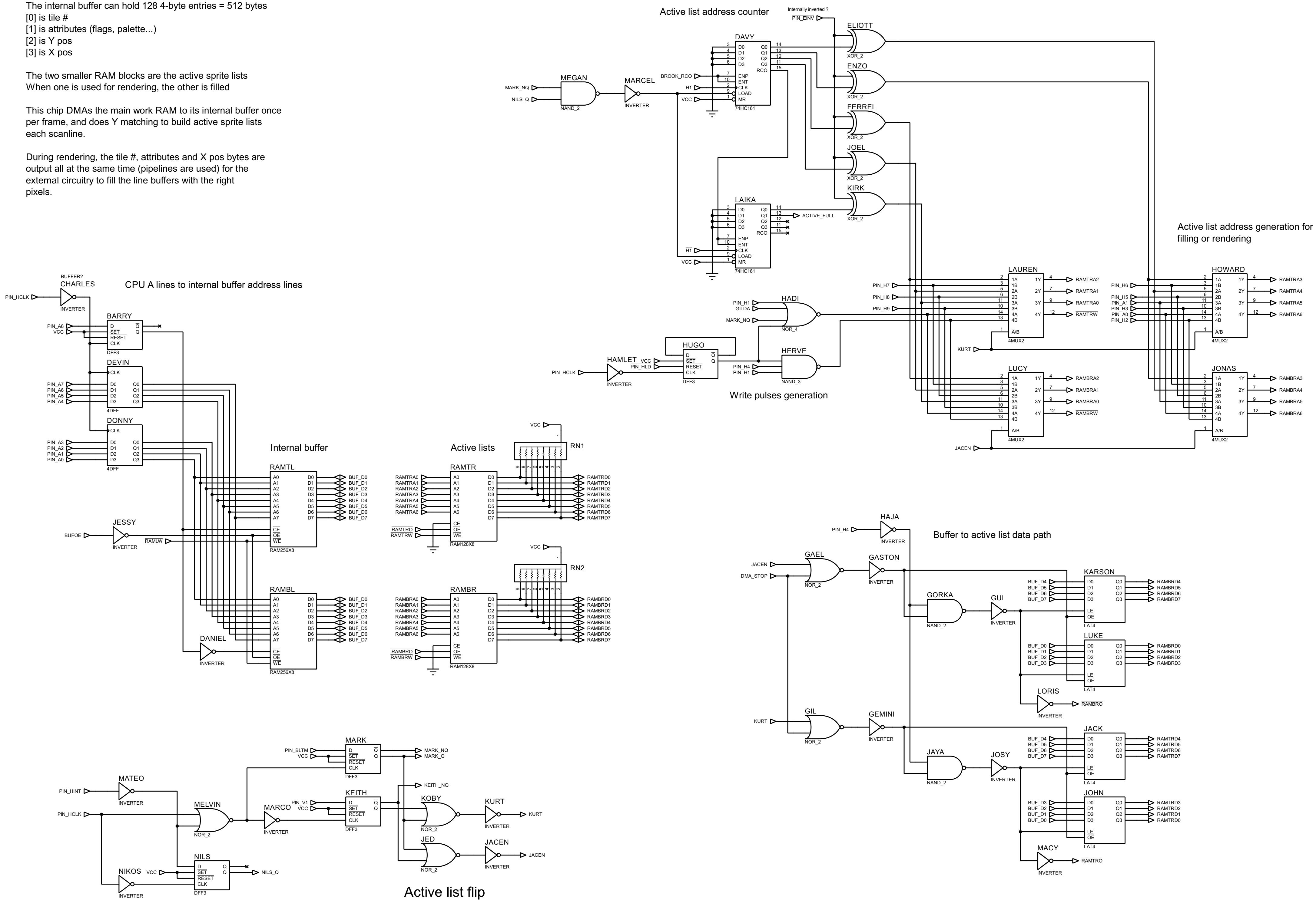
The internal buffer can hold 128 4-byte entries = 512 bytes

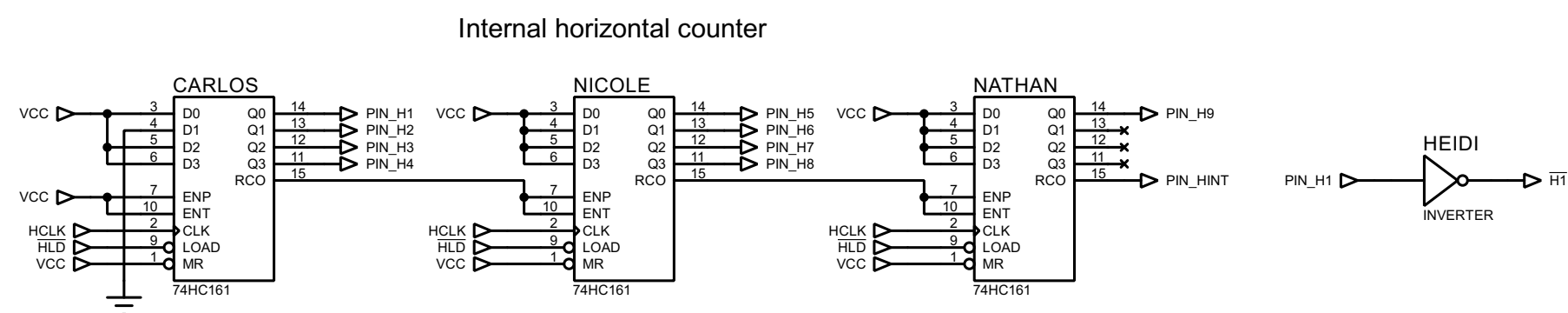
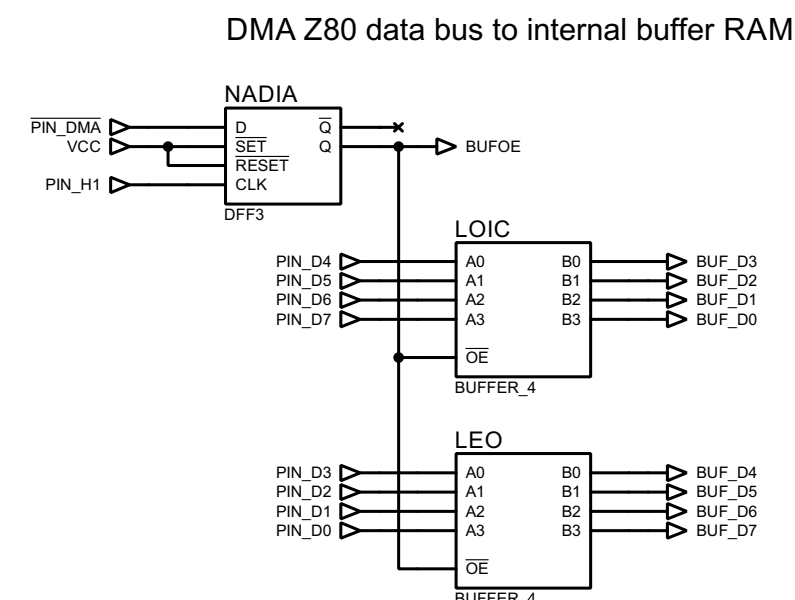
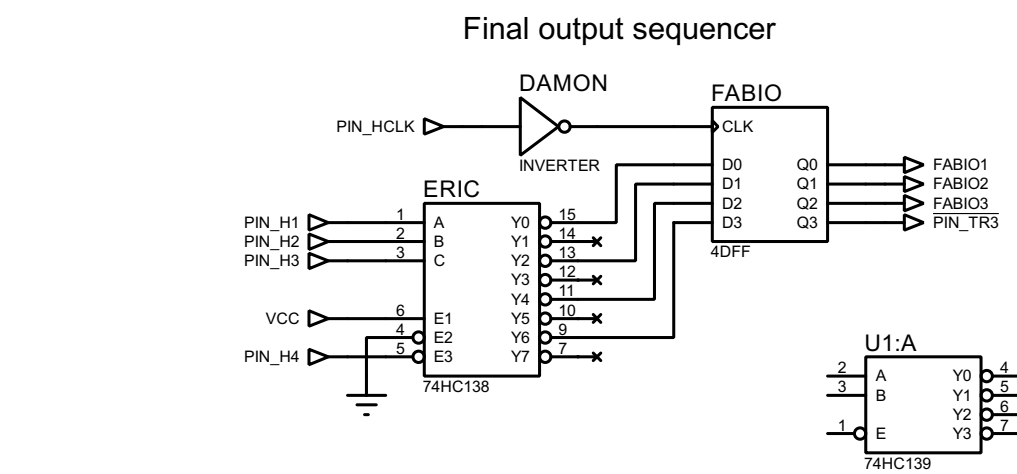
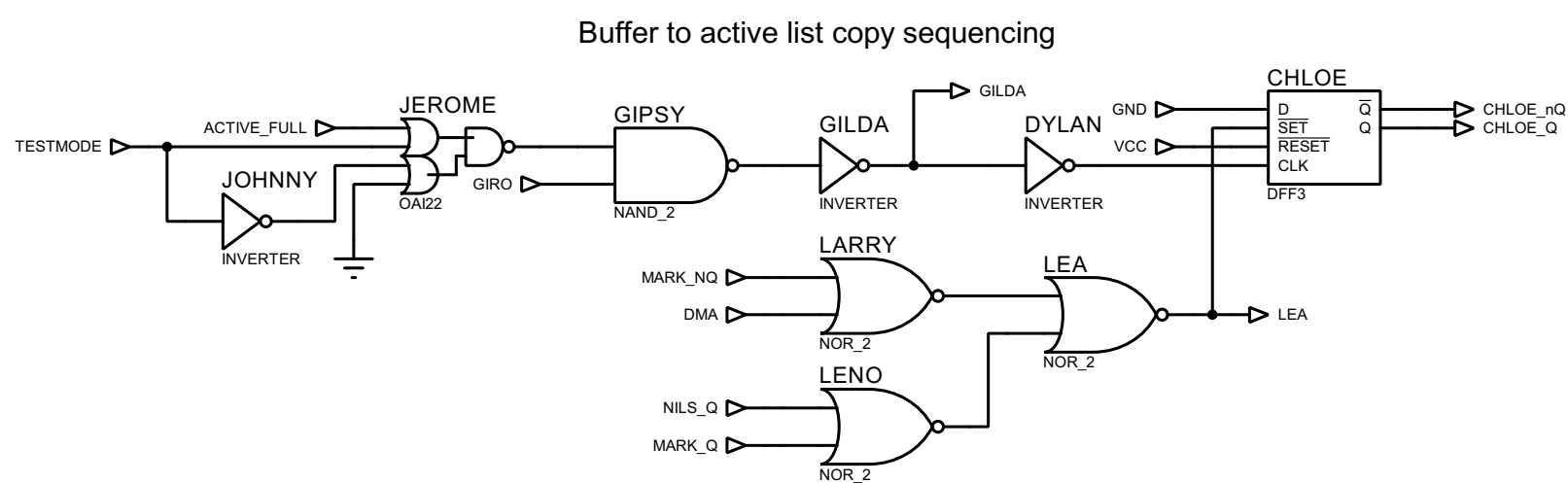
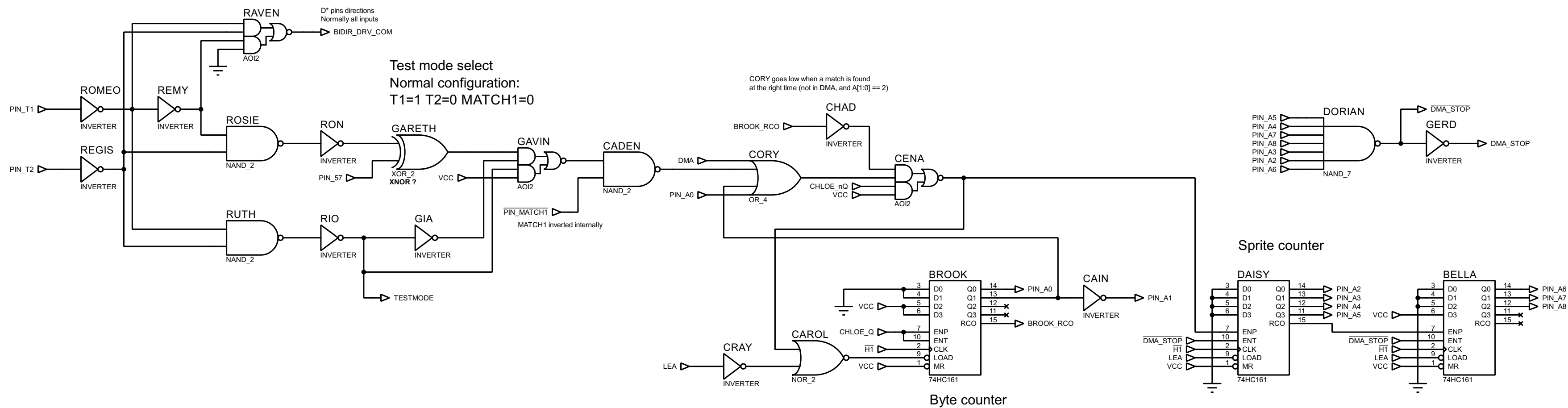
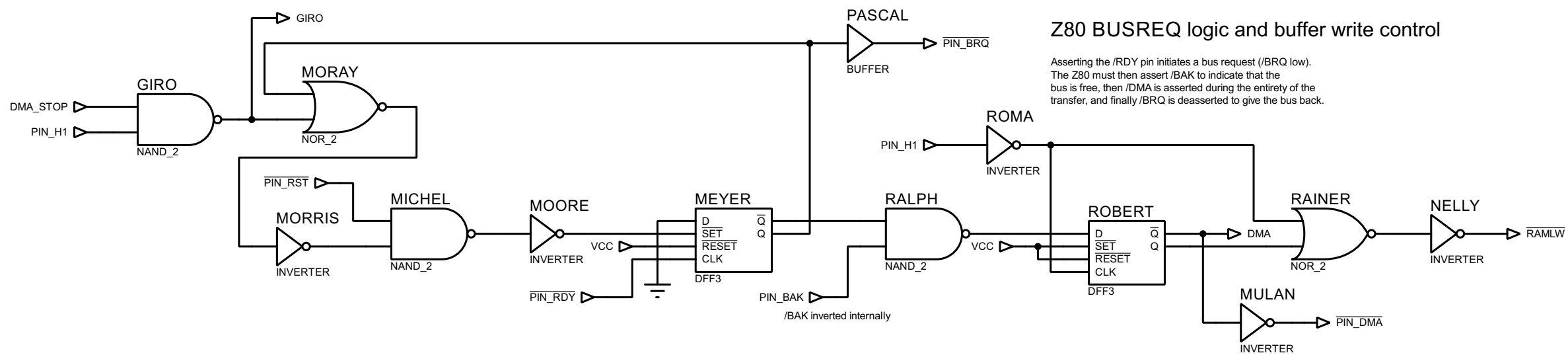
- [0] is tile #
- [1] is attributes (flags, palette...)
- [2] is Y pos
- [3] is X pos

The two smaller RAM blocks are the active sprite lists
When one is used for rendering, the other is filled

This chip DMA's the main work RAM to its internal buffer once per frame, and does Y matching to build active sprite lists each scanline.

During rendering, the tile #, attributes and X pos bytes are output all at the same time (pipelines are used) for the external circuitry to fill the line buffers with the right pixels.





The diagram illustrates the internal wiring of a system. On the left, two 4-to-1 multiplexers (4MUX2) are shown. The top multiplexer, labeled 'LYNN', has four data inputs (1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B) and one select input (\bar{A}/B). The bottom multiplexer, labeled 'KEVIN', has four data inputs (1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B) and one select input (\bar{A}/B). The select input for both is connected to a common line labeled 'KEITH_NQ'. The outputs of the multiplexers are connected to a series of output buffers. The top multiplexer's outputs (1Y, 2Y, 3Y, 4Y) are connected to the inputs of buffers BERTA, COLIN, ADELE, and ABBY. The bottom multiplexer's outputs (1Y, 2Y, 3Y, 4Y) are connected to the inputs of buffers ANDRE, DIANE, MARTIN, and AHMED. Each buffer has two outputs: 'ACTIVE' and 'PIN_POS'. The inputs to the multiplexers are labeled with RAM module names: RAMTRD3, RAMBRD3, RAMTRD2, RAMBRD2, RAMTRD1, RAMBRD1, RAMTRD0, RAMBRD0 for the top; and RAMTRD4, RAMBRD4, RAMTRD5, RAMBRD5, RAMTRD6, RAMBRD6, RAMTRD7, RAMBRD7 for the bottom.

The diagram illustrates a digital circuit with two 4DFF flip-flops, MARY and NICK, and eight output buffers. The inputs and outputs are as follows:

- Inputs:** FABIO2, ACTIVE_D0, ACTIVE_D1, ACTIVE_D2, ACTIVE_D3, ACTIVE_D4, ACTIVE_D5, ACTIVE_D6, ACTIVE_D7.
- Flip-Flops:**
 - MARY:** CLK (connected to FABIO2 and NICK's CLK), D0-D3 (connected to ACTIVE_D0-ACTIVE_D3), Q0-Q3 (outputs).
 - NICK:** CLK (connected to FABIO2 and MARY's CLK), D0-D3 (connected to ACTIVE_D4-ACTIVE_D7), Q0-Q3 (outputs).
- Outputs:**
 - MARY's Q0-Q3:** Connected to buffers LIAM, MIGUEL, MORGAN, and MOLLY, which output to PIN_ATR0, PIN_ATR1, PIN_ATR2, and PIN_ATR3 respectively.
 - NICK's Q0-Q3:** Connected to buffers NORA, PETER, PAUL, and ROGER, which output to PIN_ATR4, PIN_ATR5, PIN_ATR6, and PIN_ATR7 respectively.

The diagram illustrates the internal structure of the 4DFF module, which consists of four 4-bit D-type flip-flops (DFFs) arranged in a 2x2 grid. The top row contains the HOGAN and HARDY DFFs, and the bottom row contains the KASPER and KEPLER DFFs. Each DFF has four data inputs (D0, D1, D2, D3) and four data outputs (Q0, Q1, Q2, Q3). The clock inputs (CLK) for all DFFs are connected to the FABIO1 and FABIO2 signals. The outputs of the DFFs are connected to the output pins (PIN_CHR0 to PIN_CHR7) through buffers. The output pins are labeled as PIN_CHR0, PIN_CHR1, PIN_CHR2, PIN_CHR3, PIN_CHR4, PIN_CHR5, PIN_CHR6, and PIN_CHR7. The buffers are labeled as DUKE, ELWOOD, ETAN, FALCON, GARAN, JEFF, KOSSI, and KYLE. The diagram also shows the internal connections between the DFFs and the output pins.