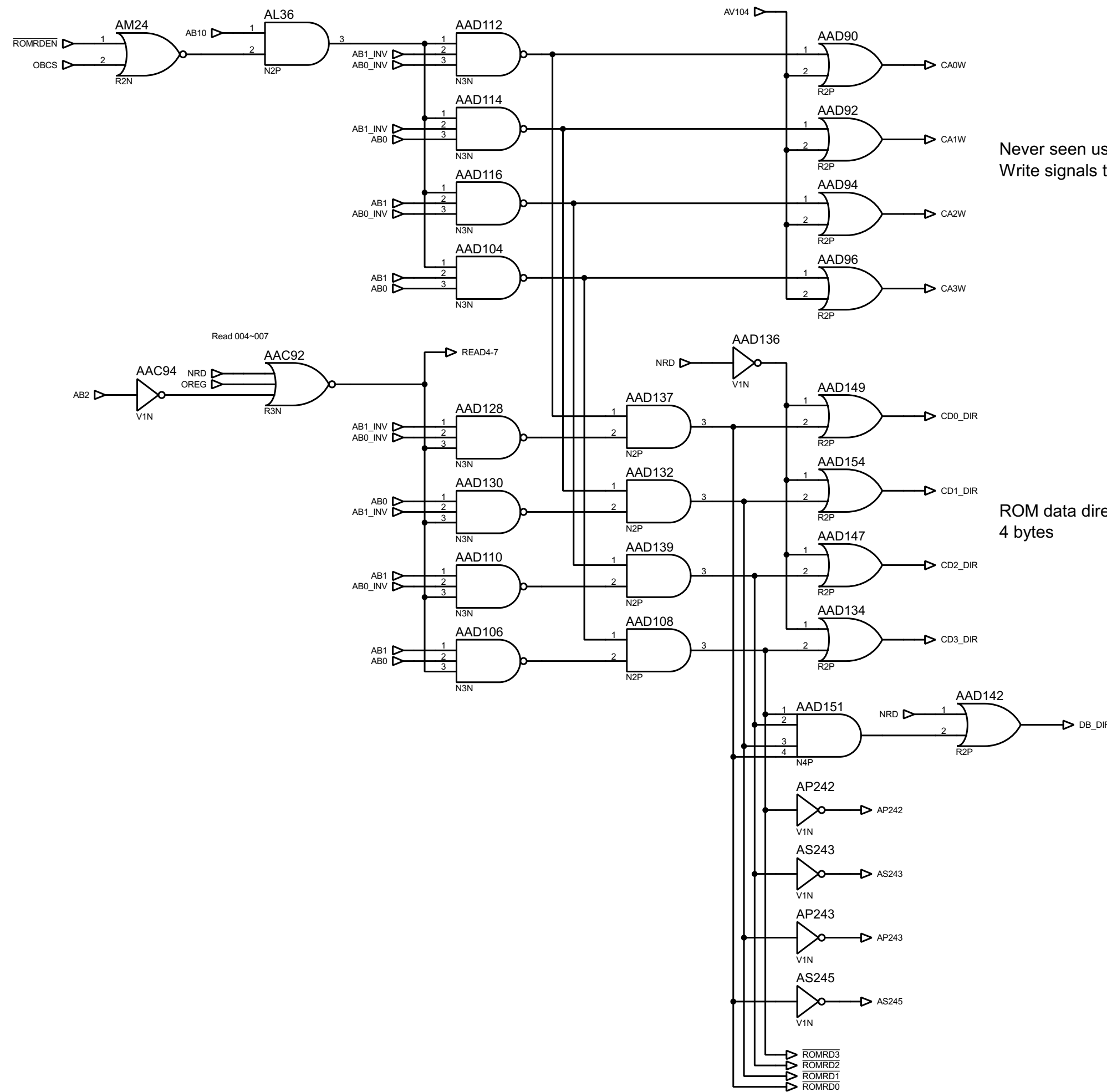
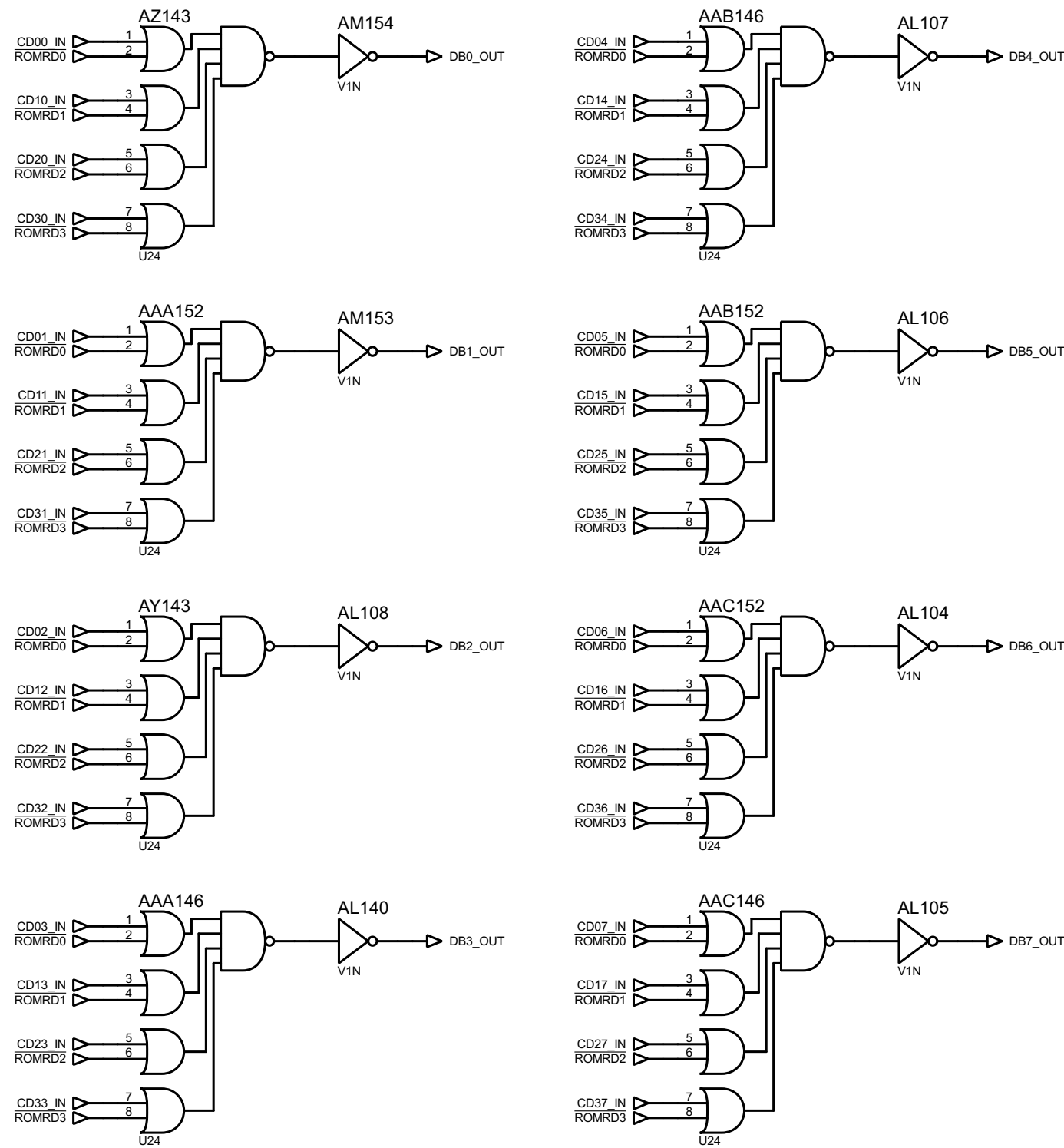


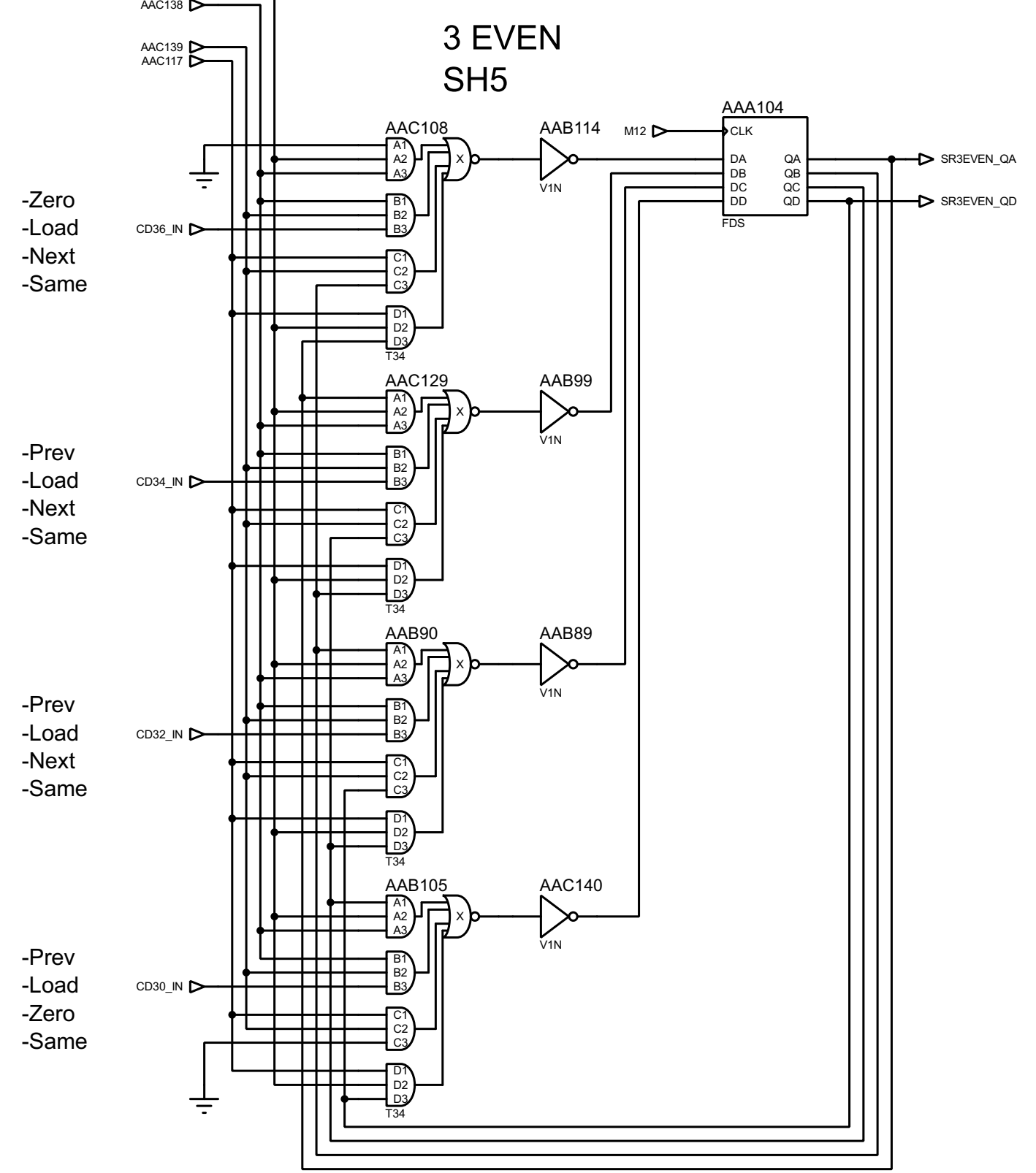
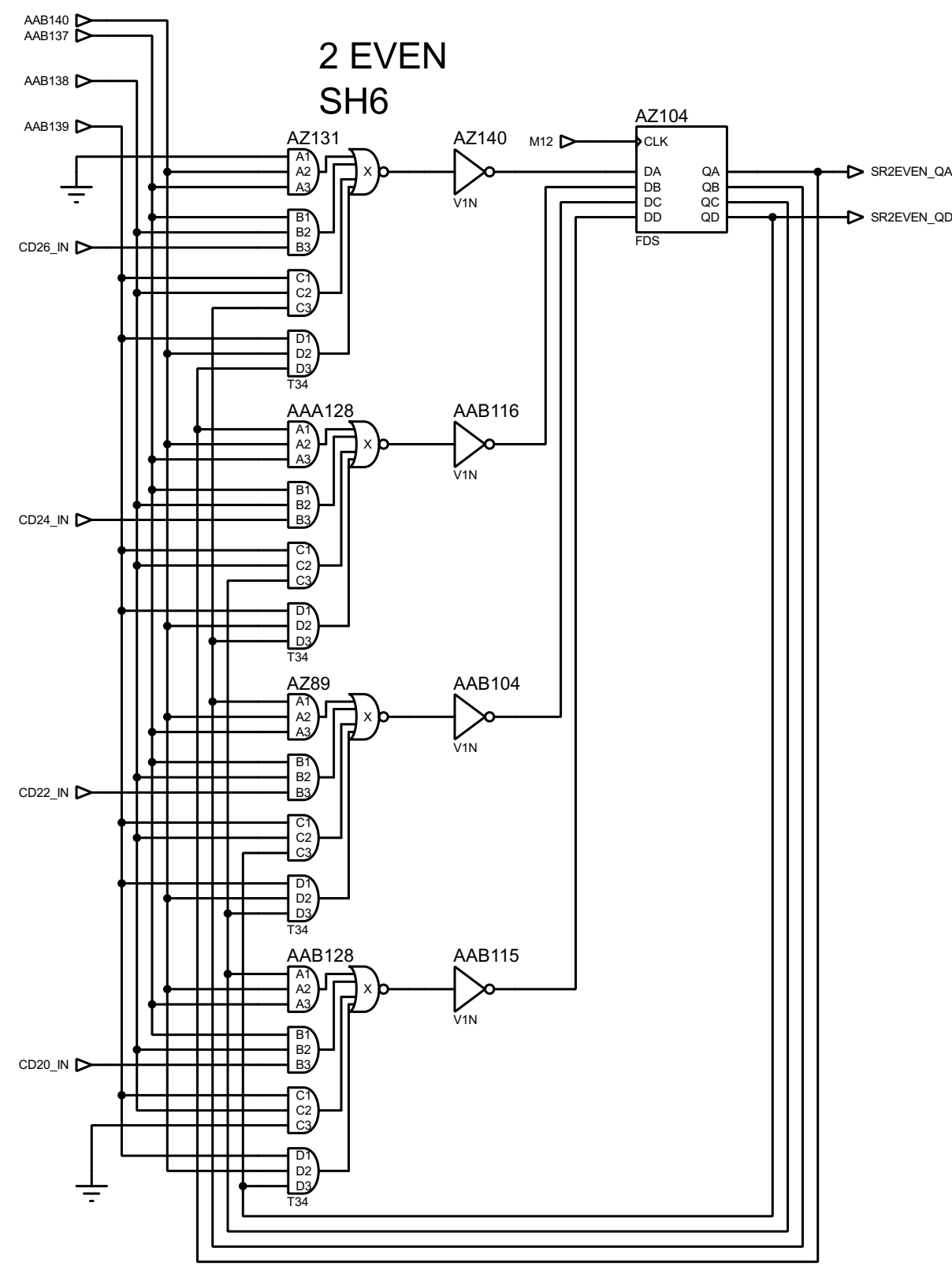
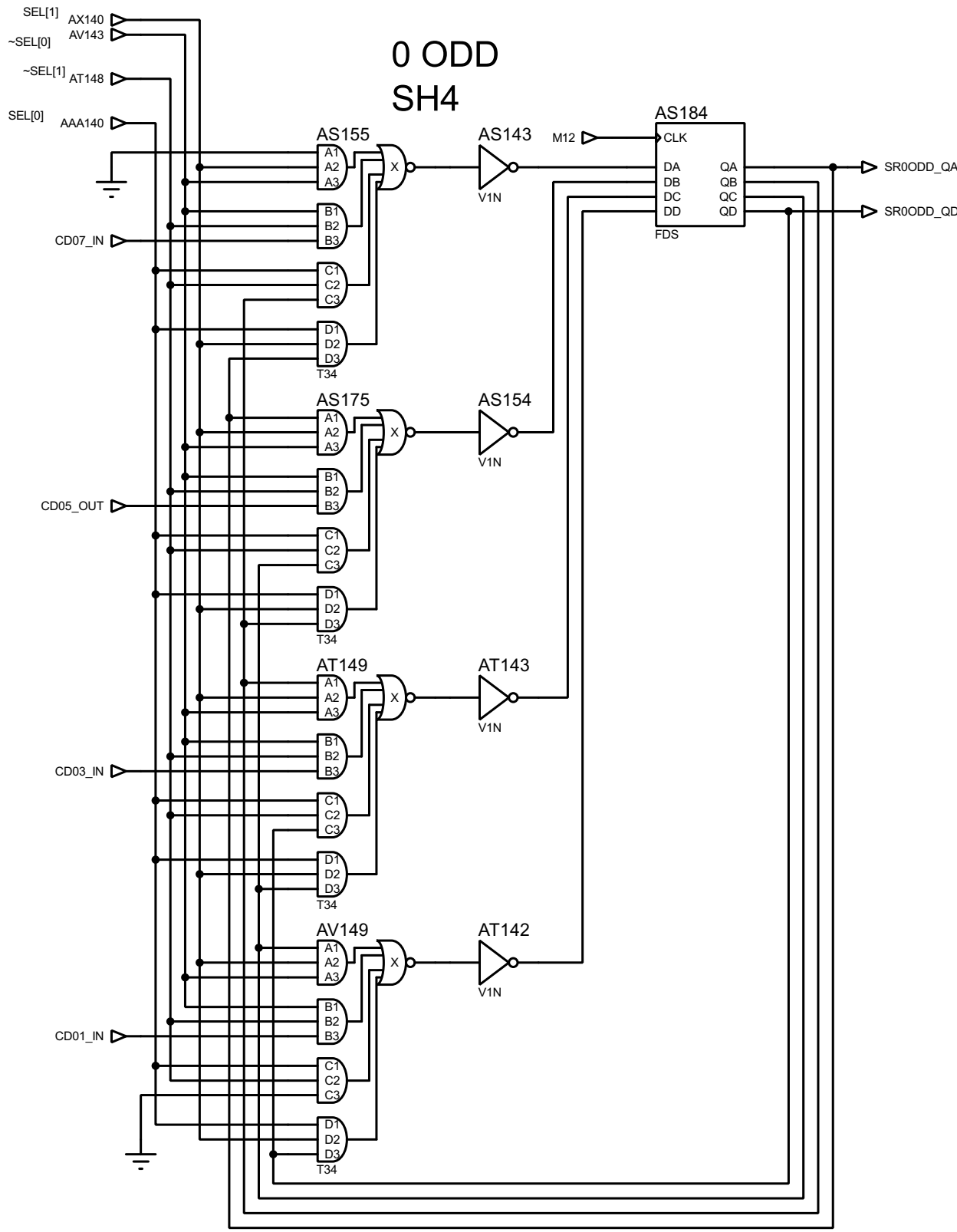
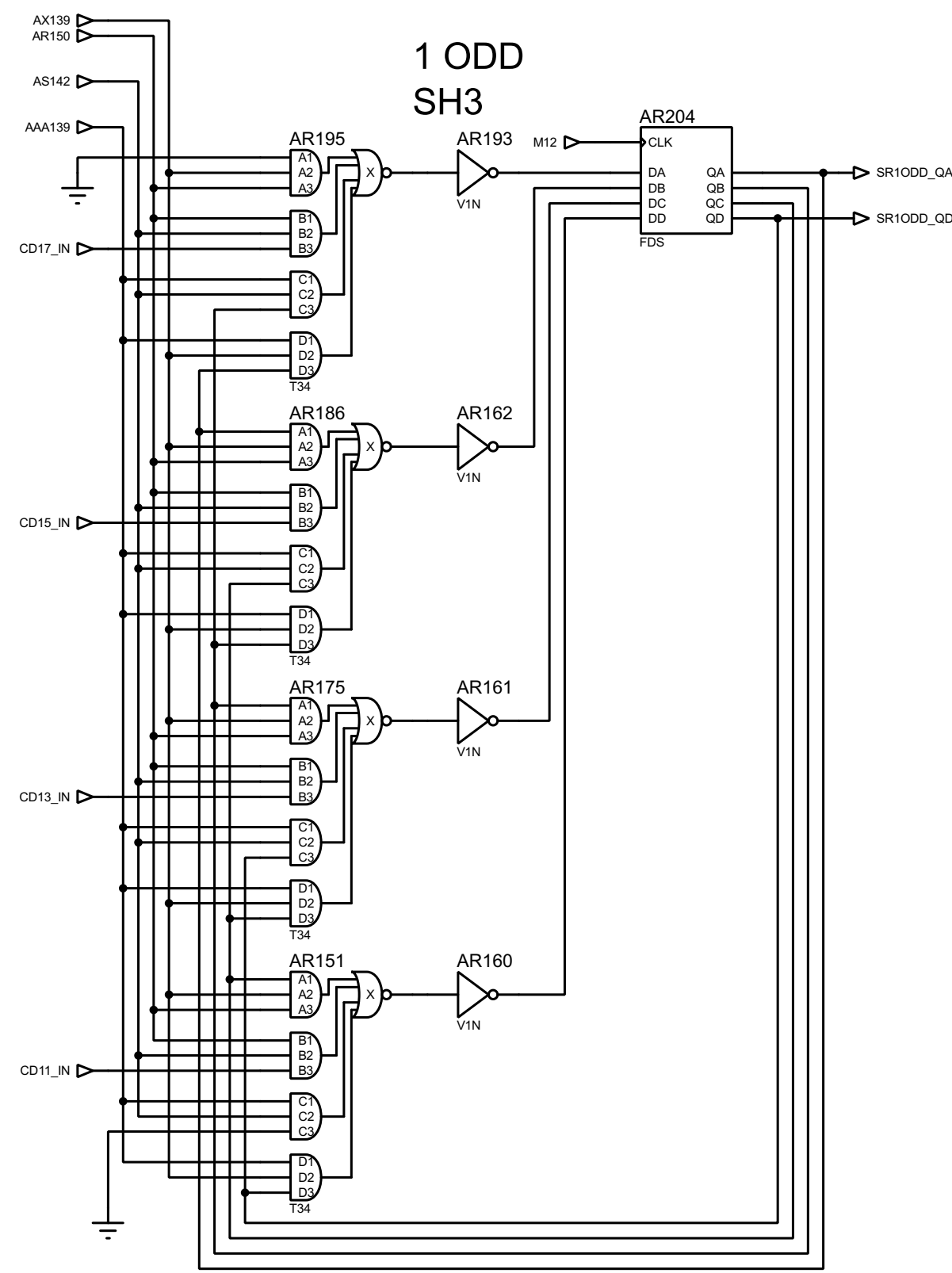
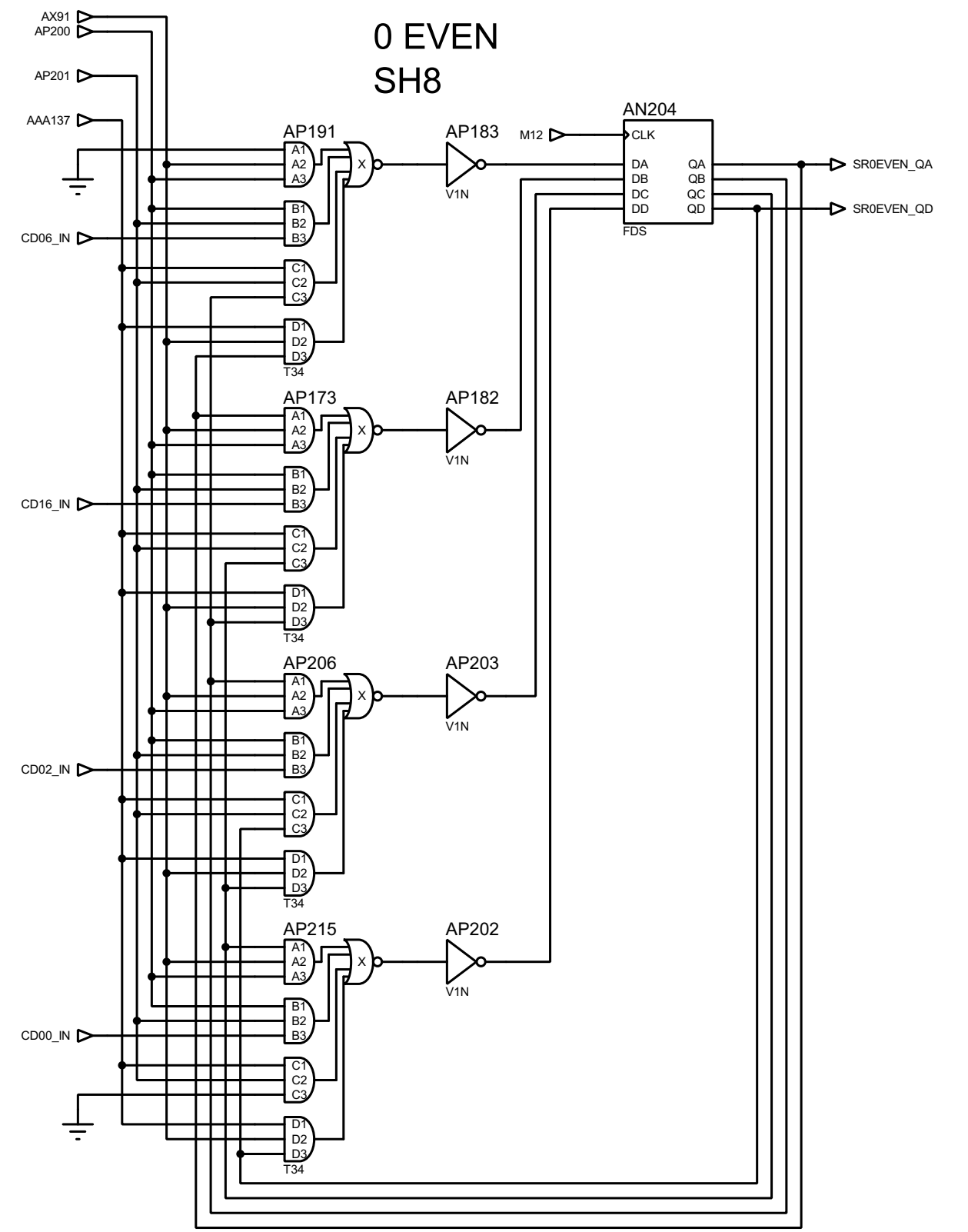
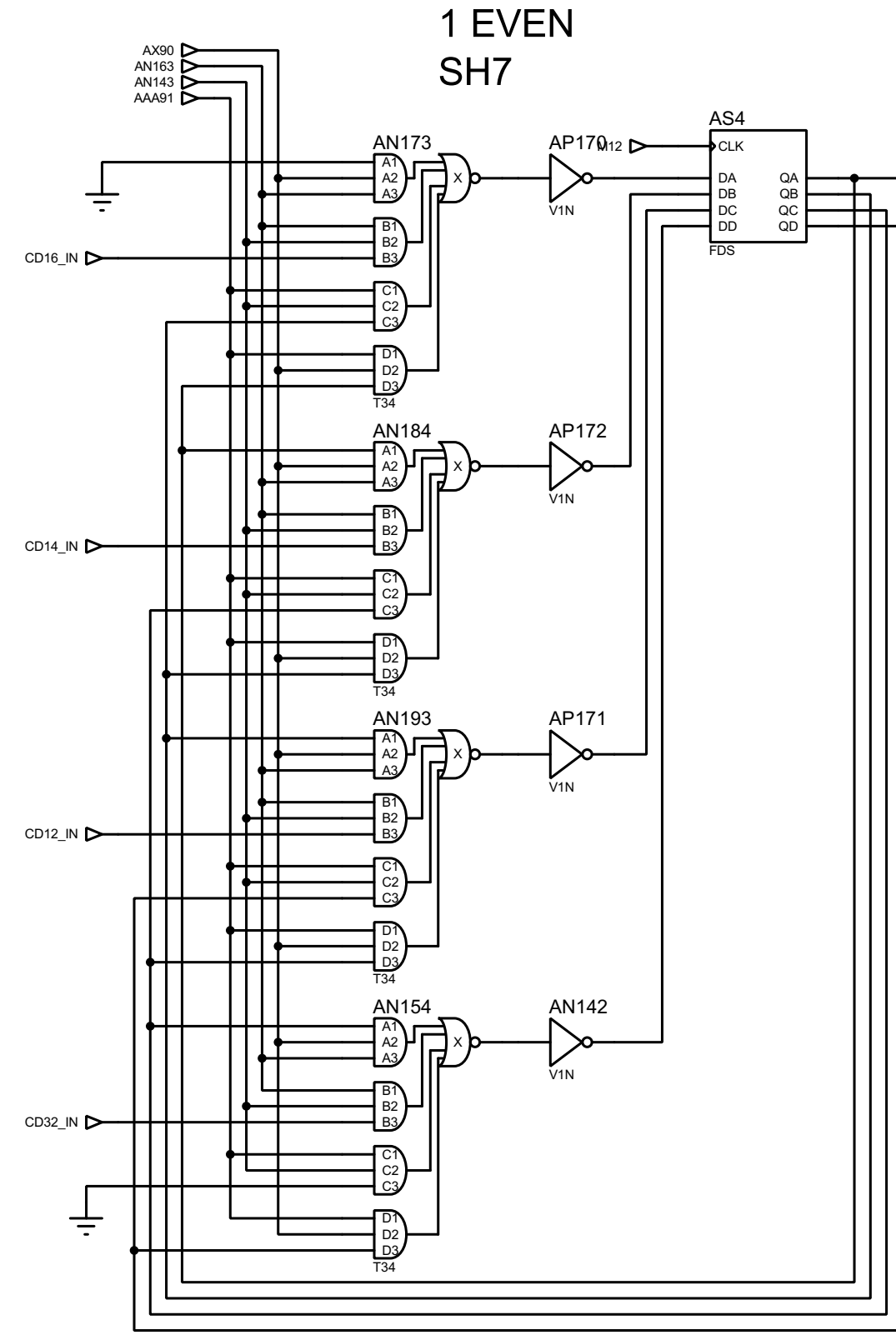
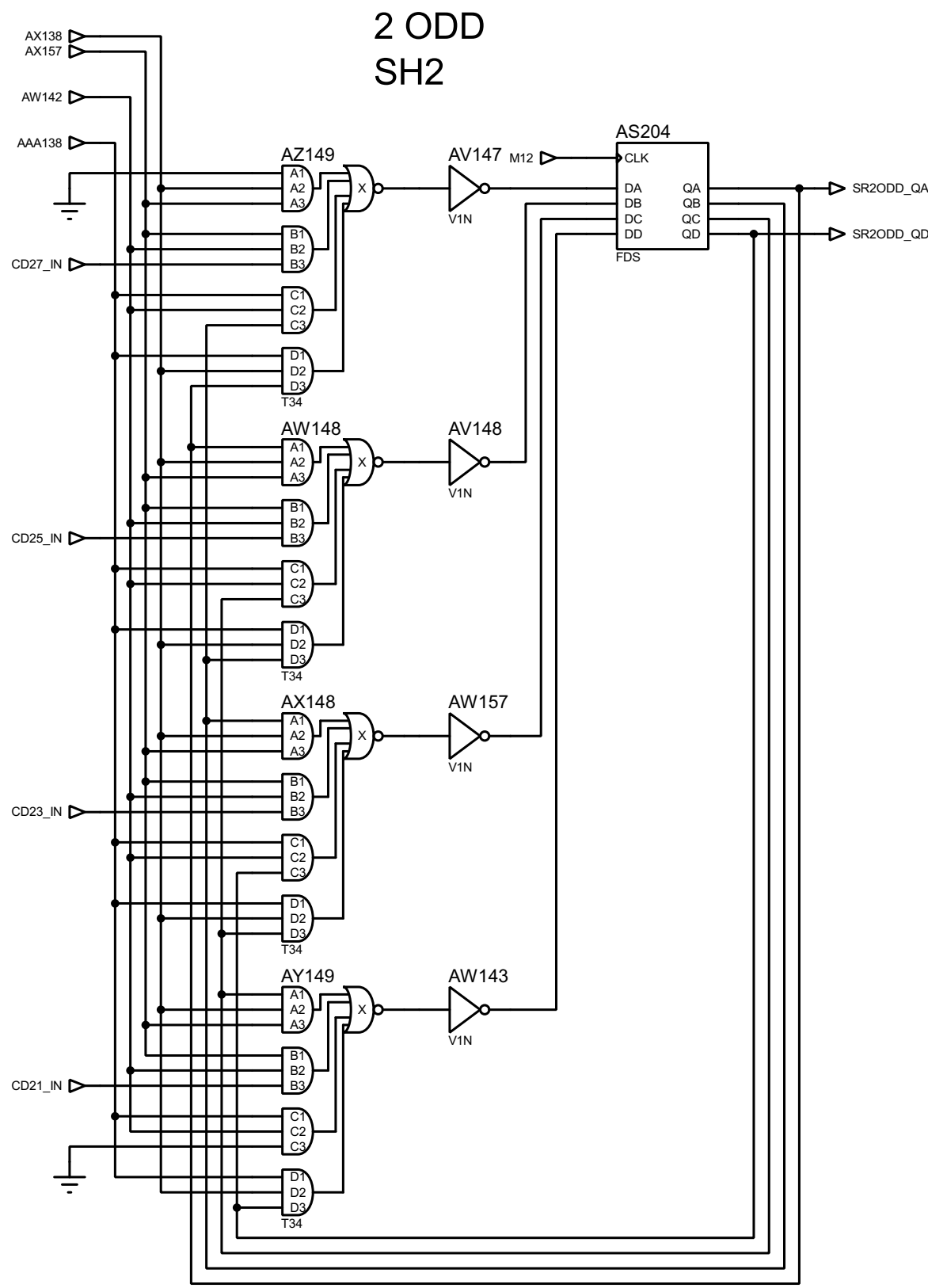
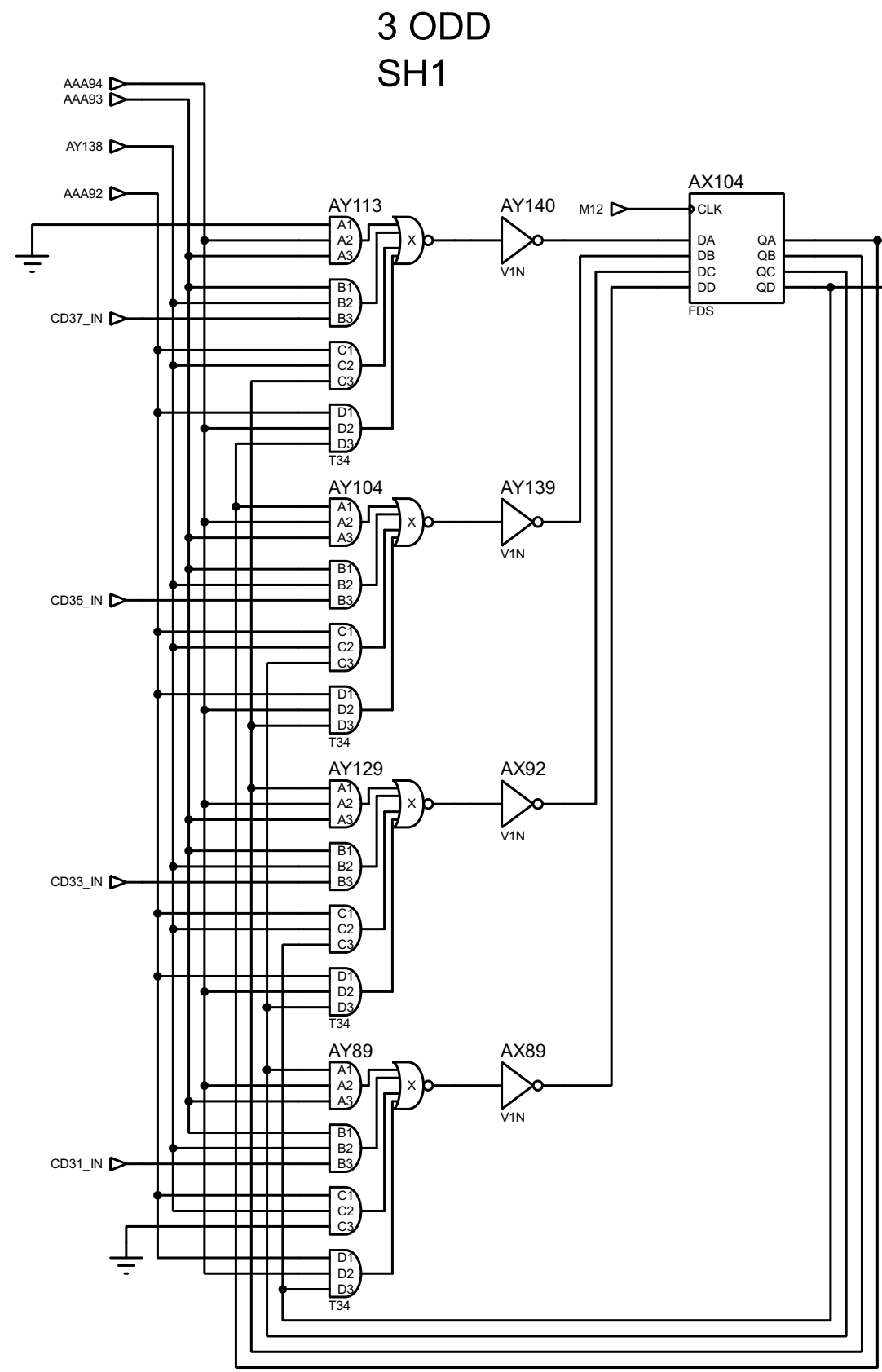
32 to 8 mux for ROM CPU readback



Never seen used on schematics
Write signals to possible GFX RAM ?

ROM data direction
4 bytes

Eight 4bpp pixels in

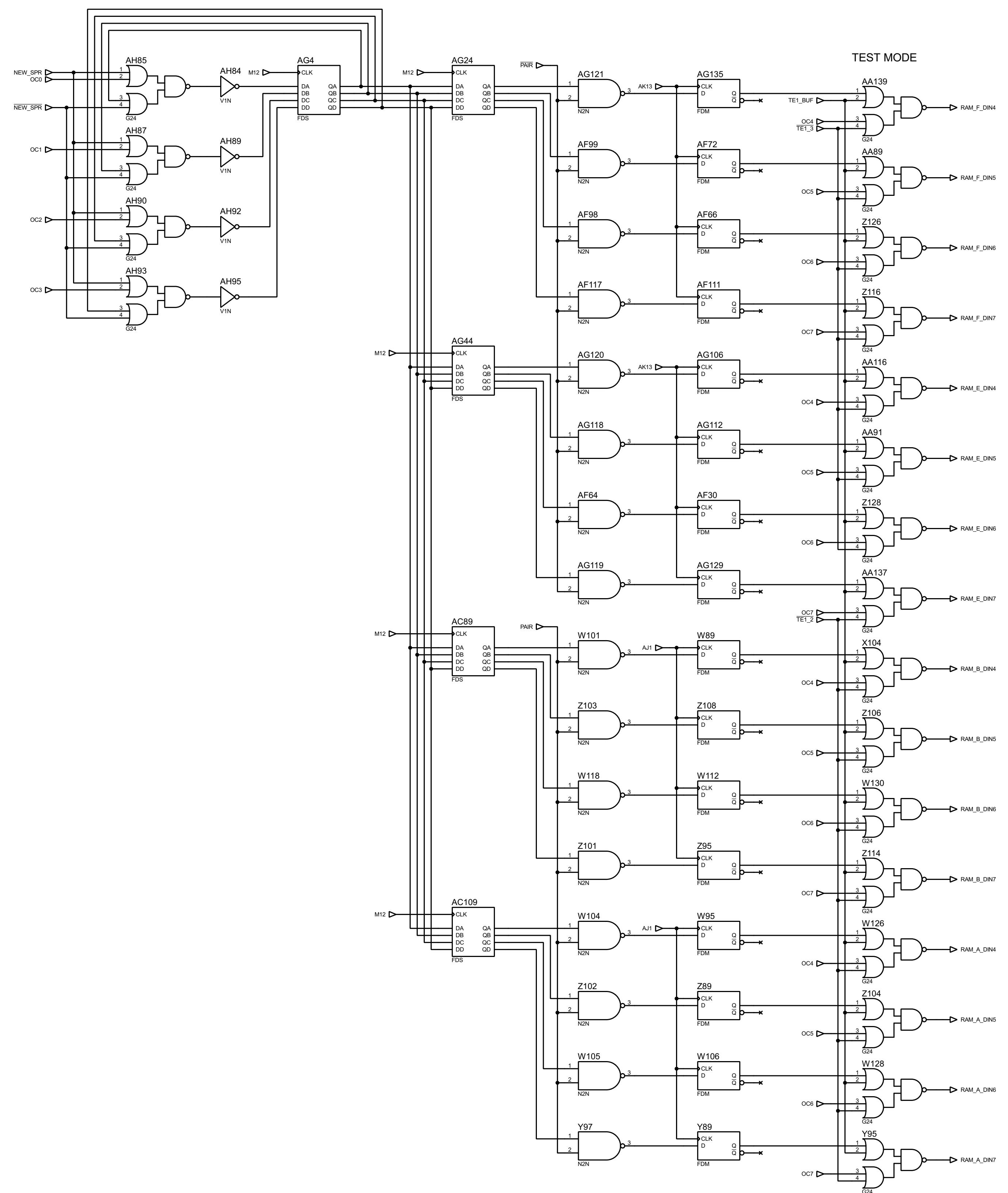
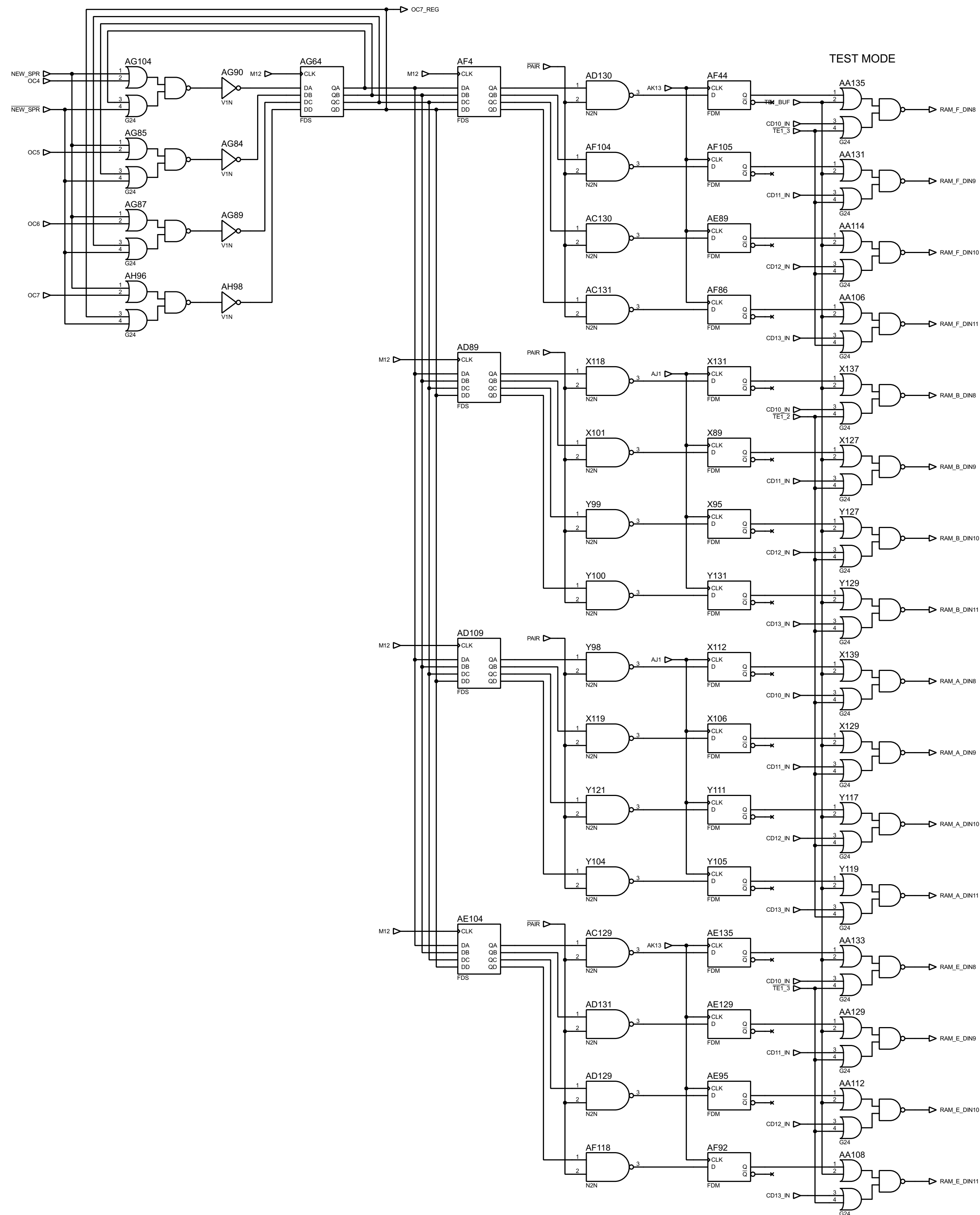


-Zero
-Load
-Next
-Same

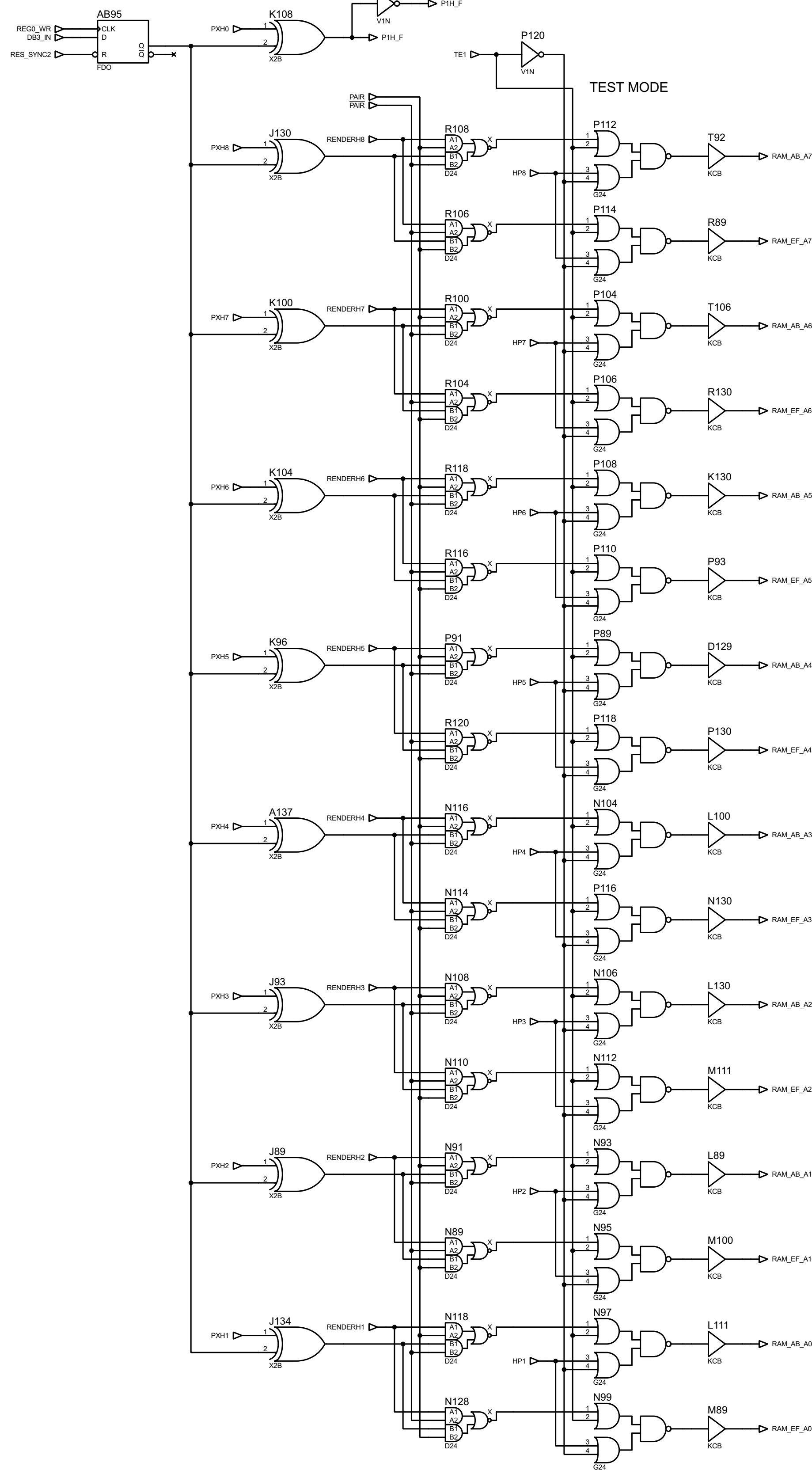
-Prev
-Load
-Next
-Same

-Prev
-Load
-Next
-Same

-Prev
-Load
-Zero
-Same

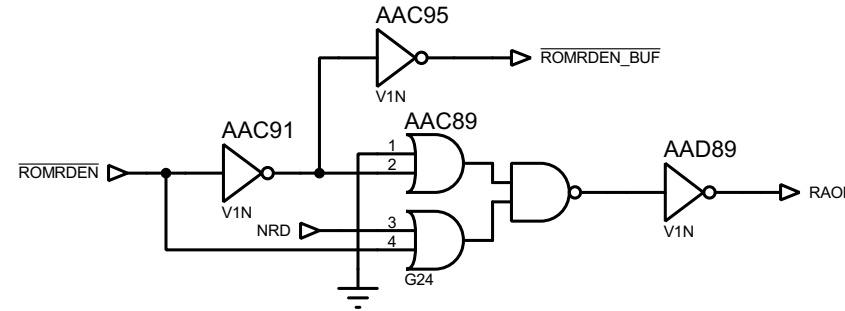


Reg 0 bit 3: Flip screen

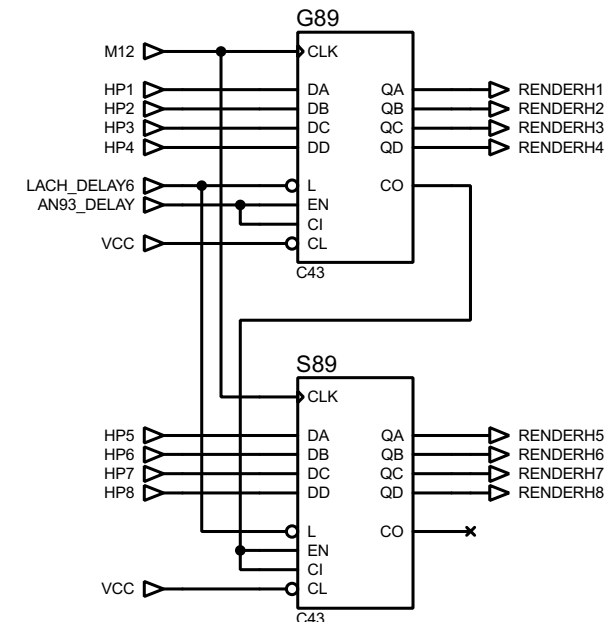


Select between rendering apos
and output scan counters

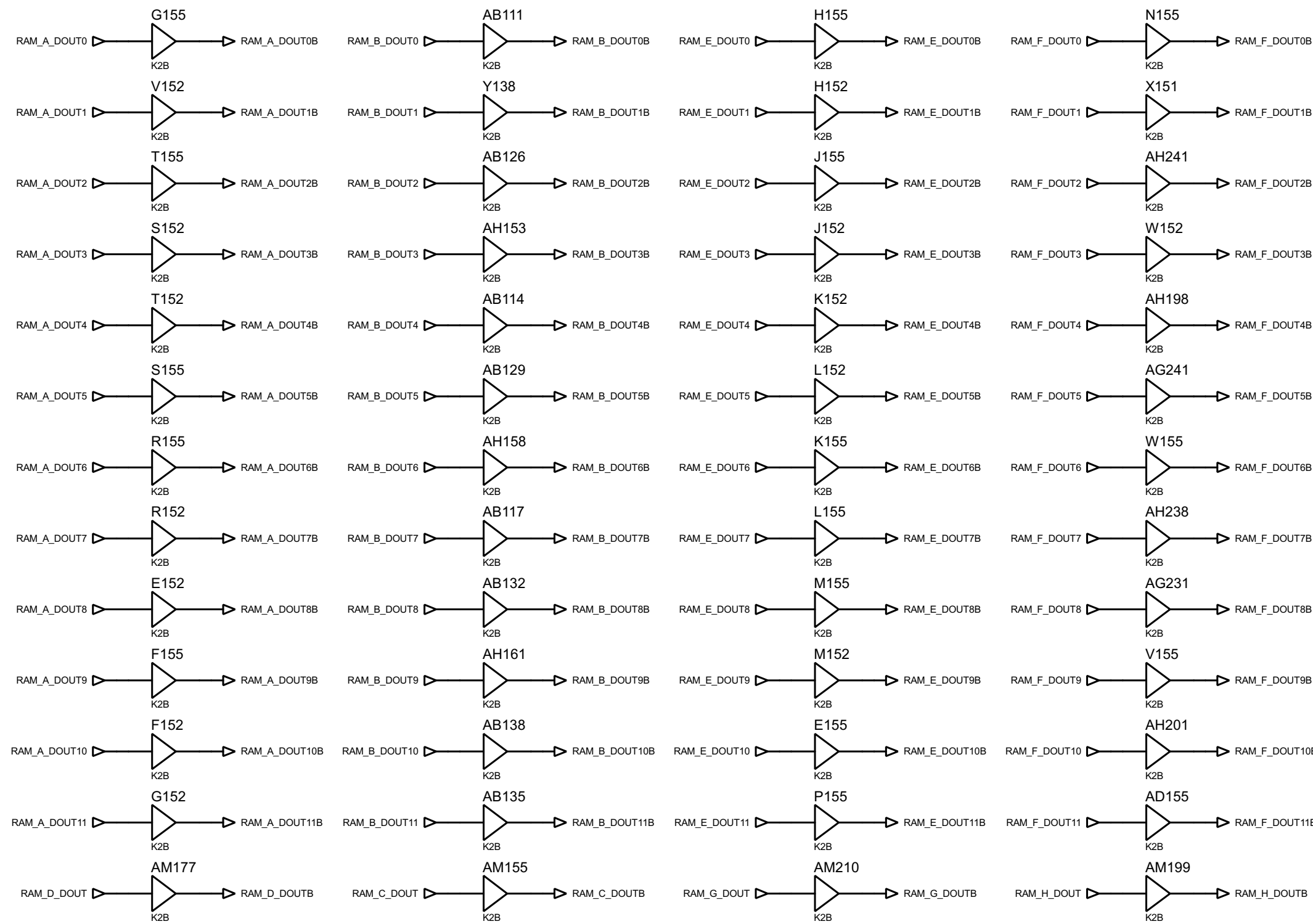
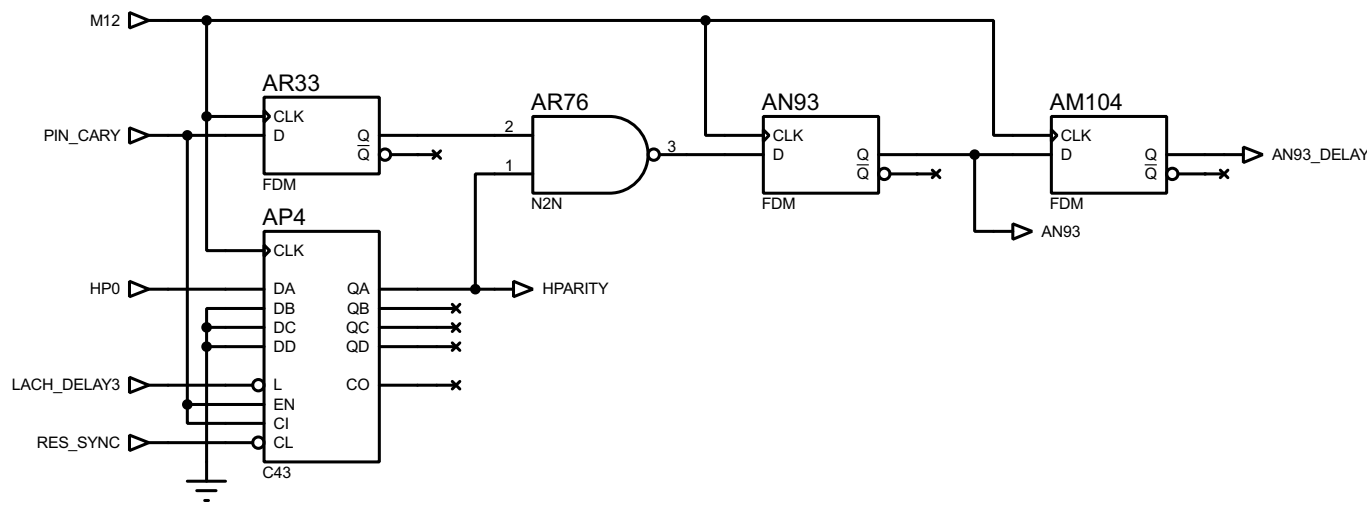
TEST MODE

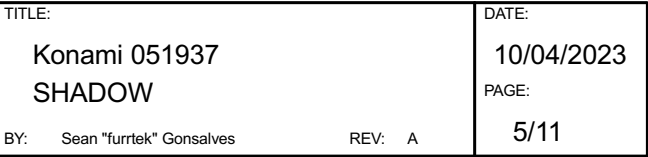


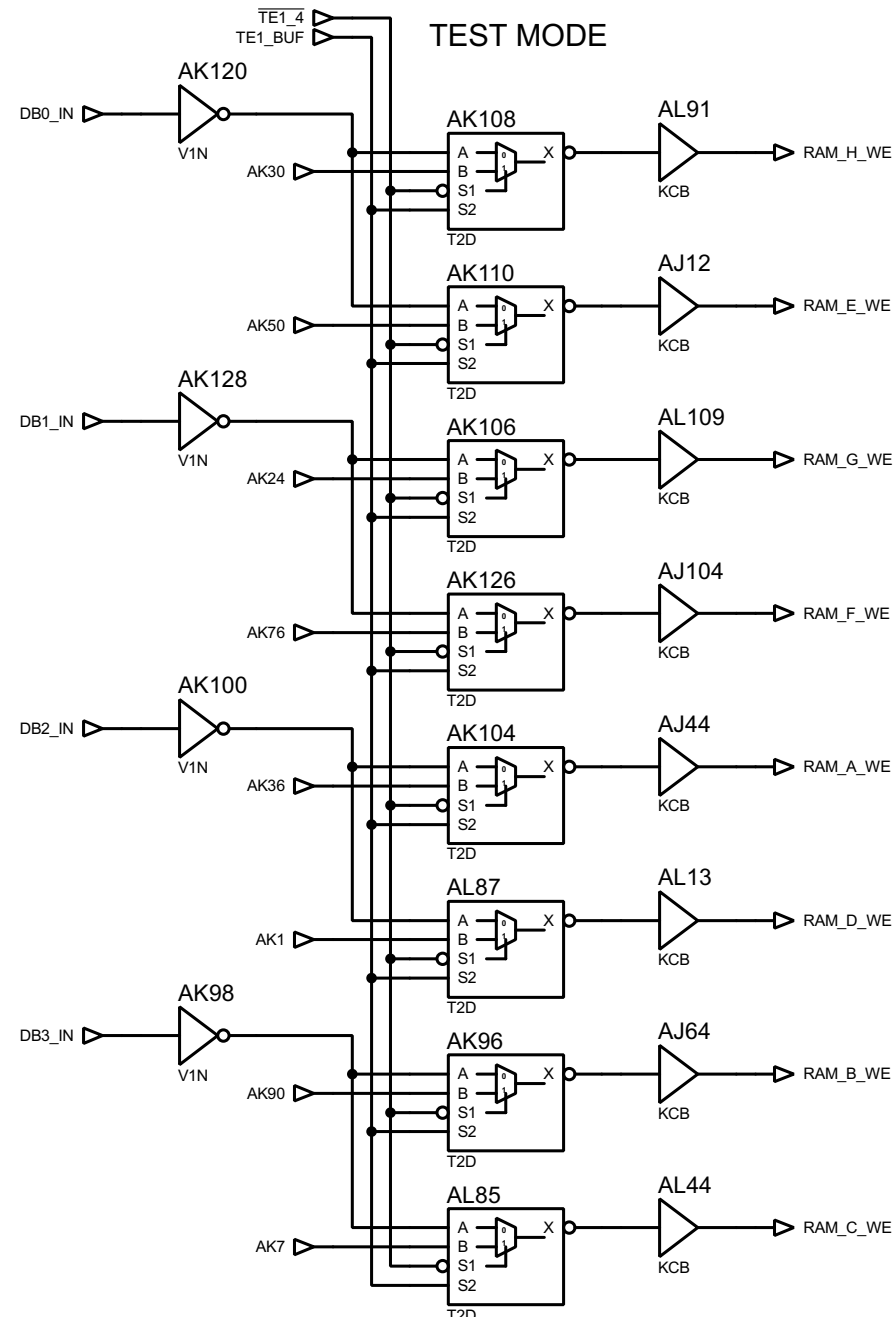
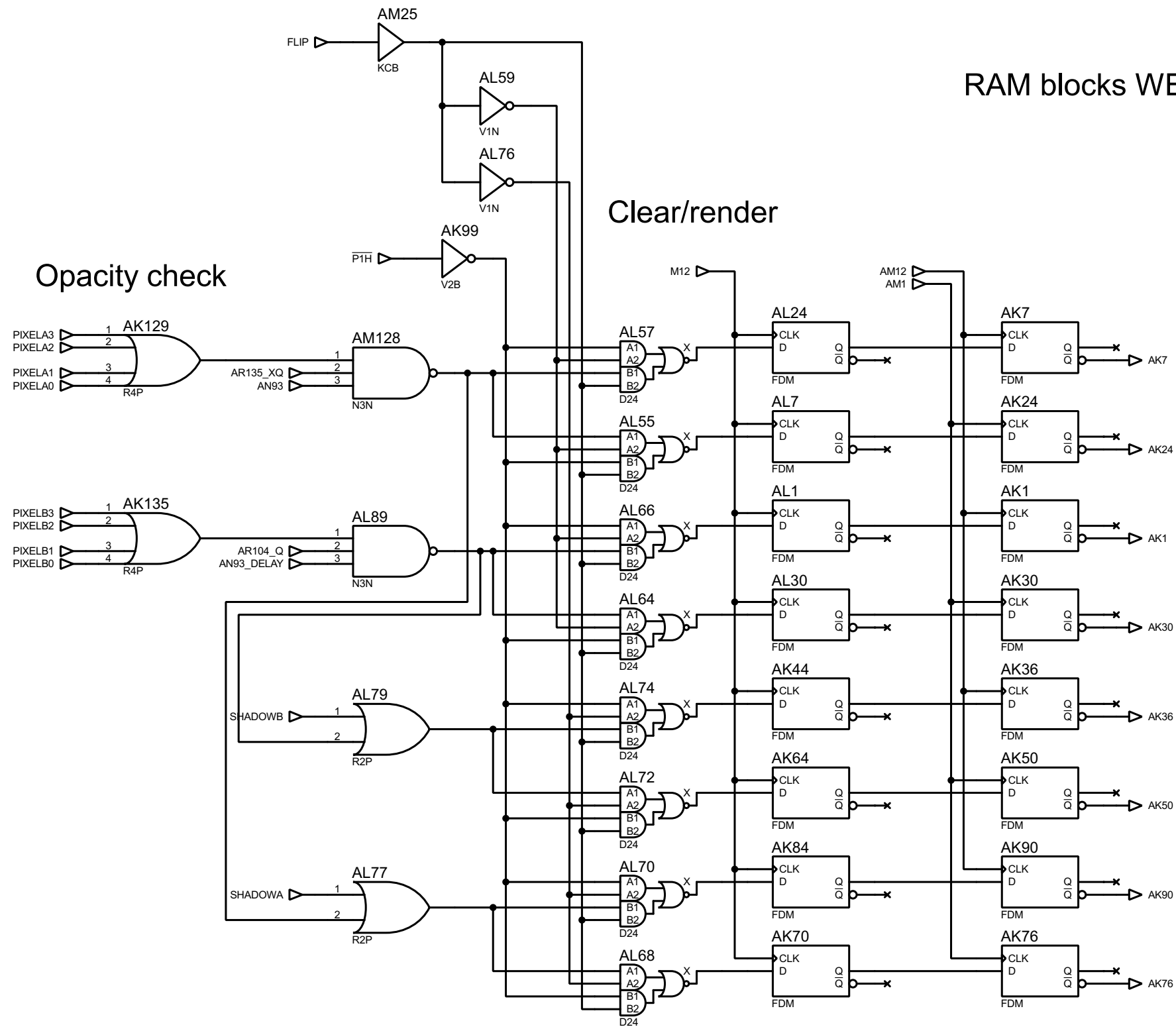
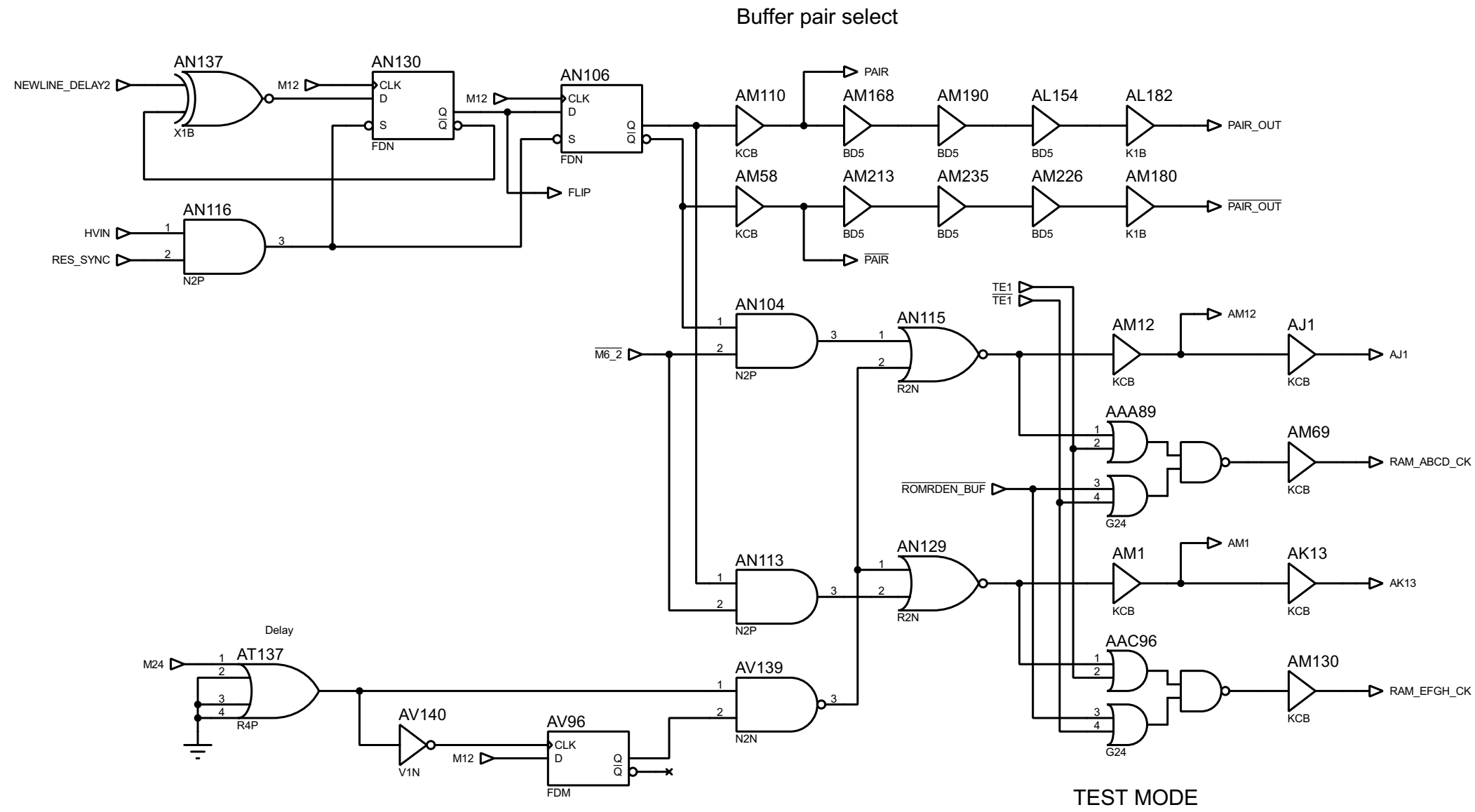
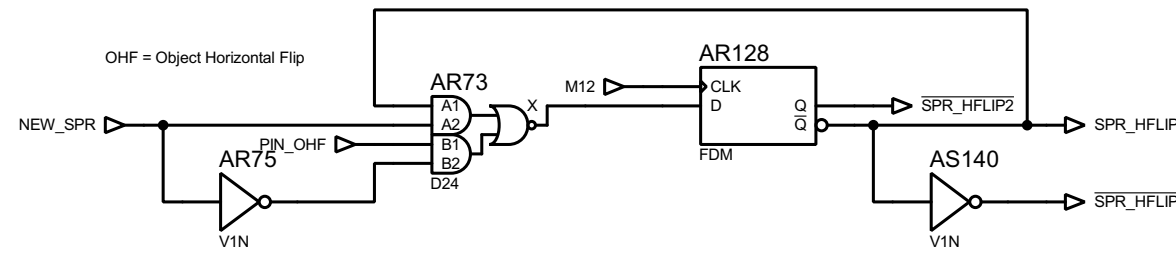
Render counters

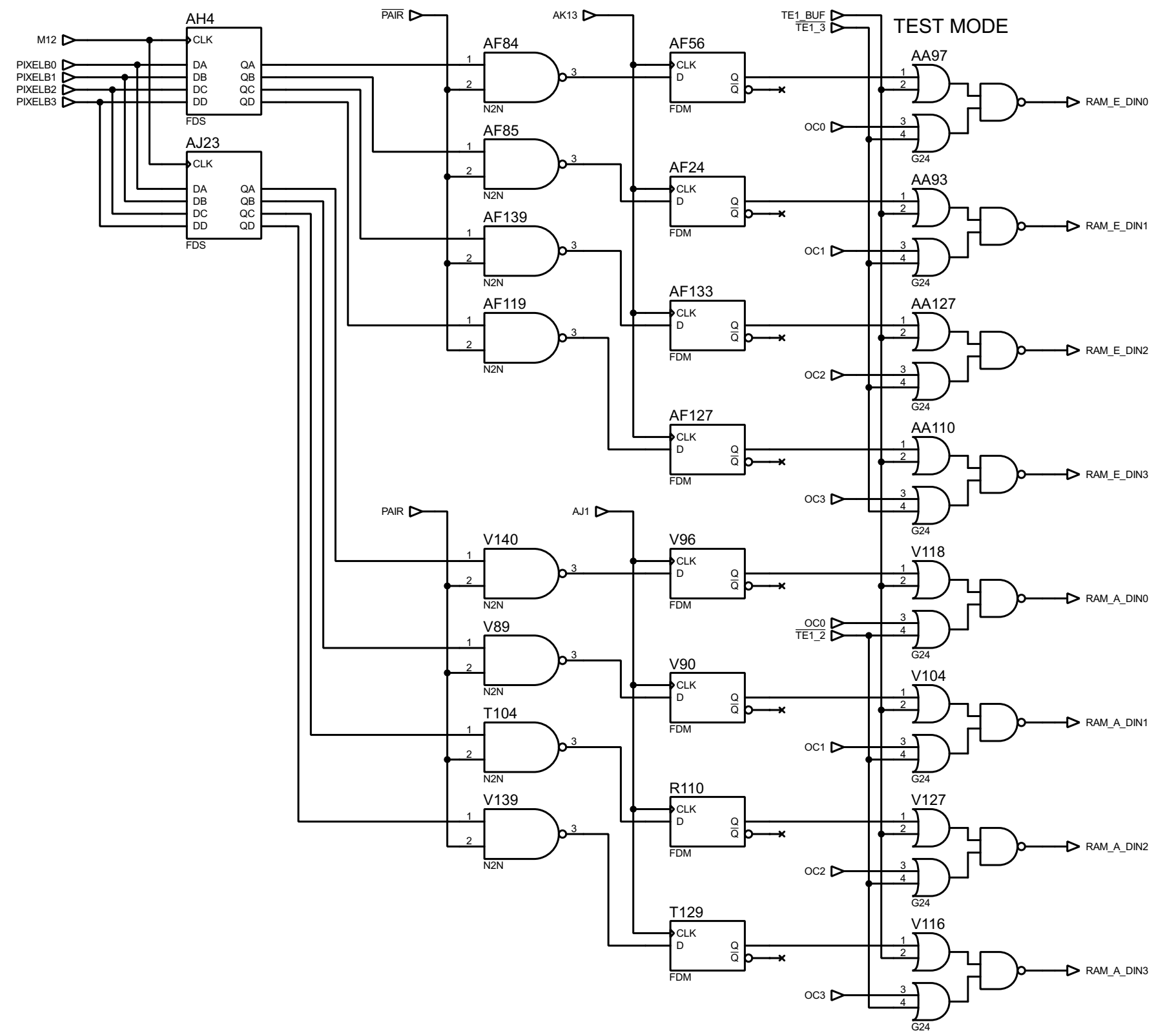
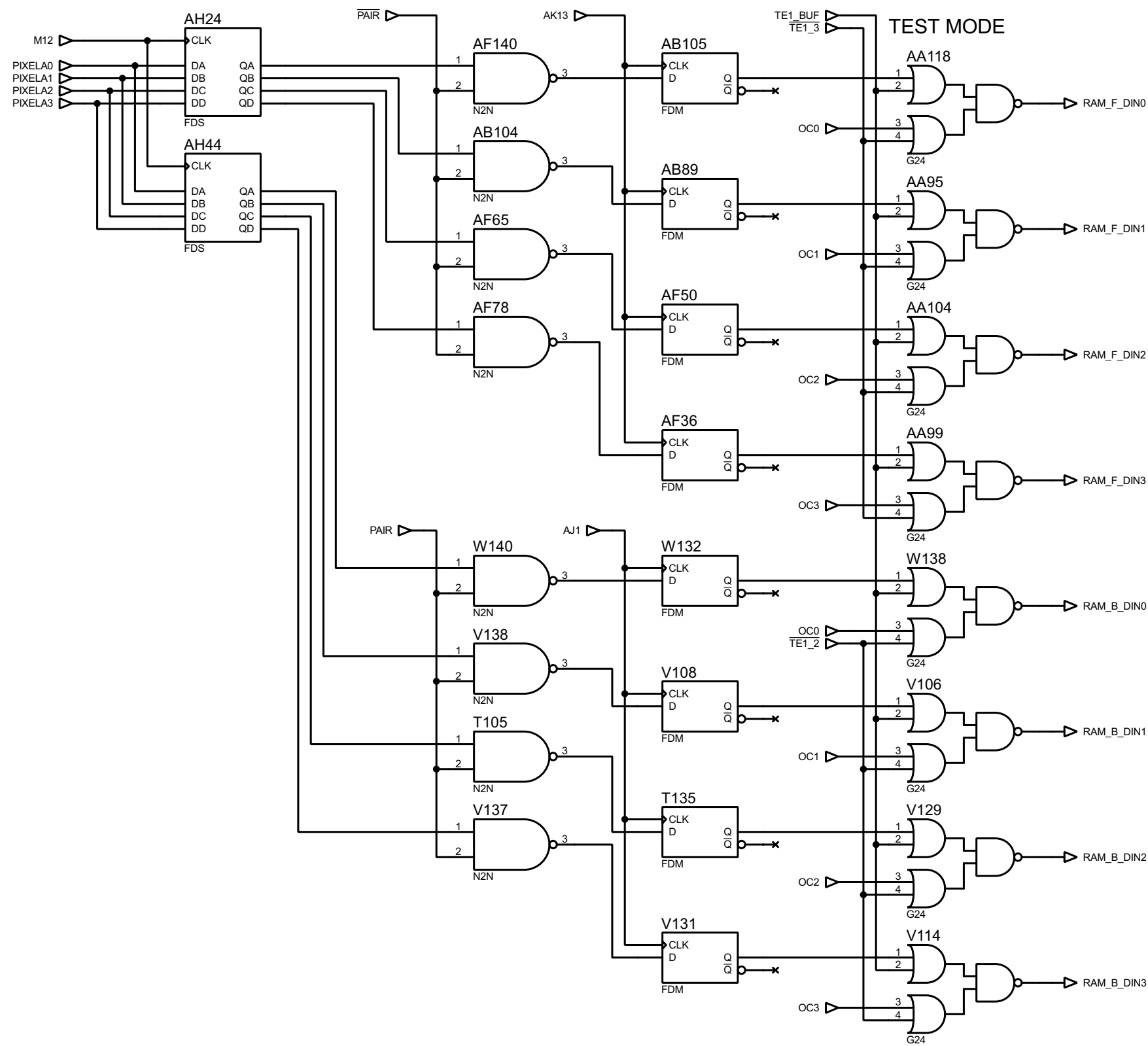


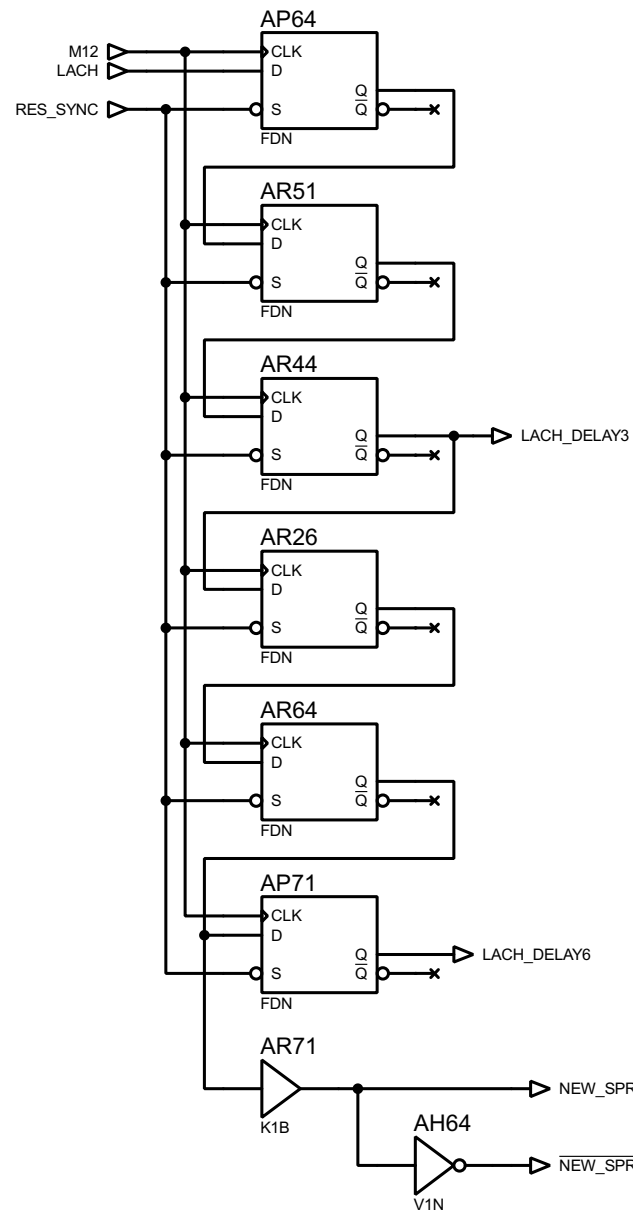
Overwrite pixel in LB if CARY changes CHECKED



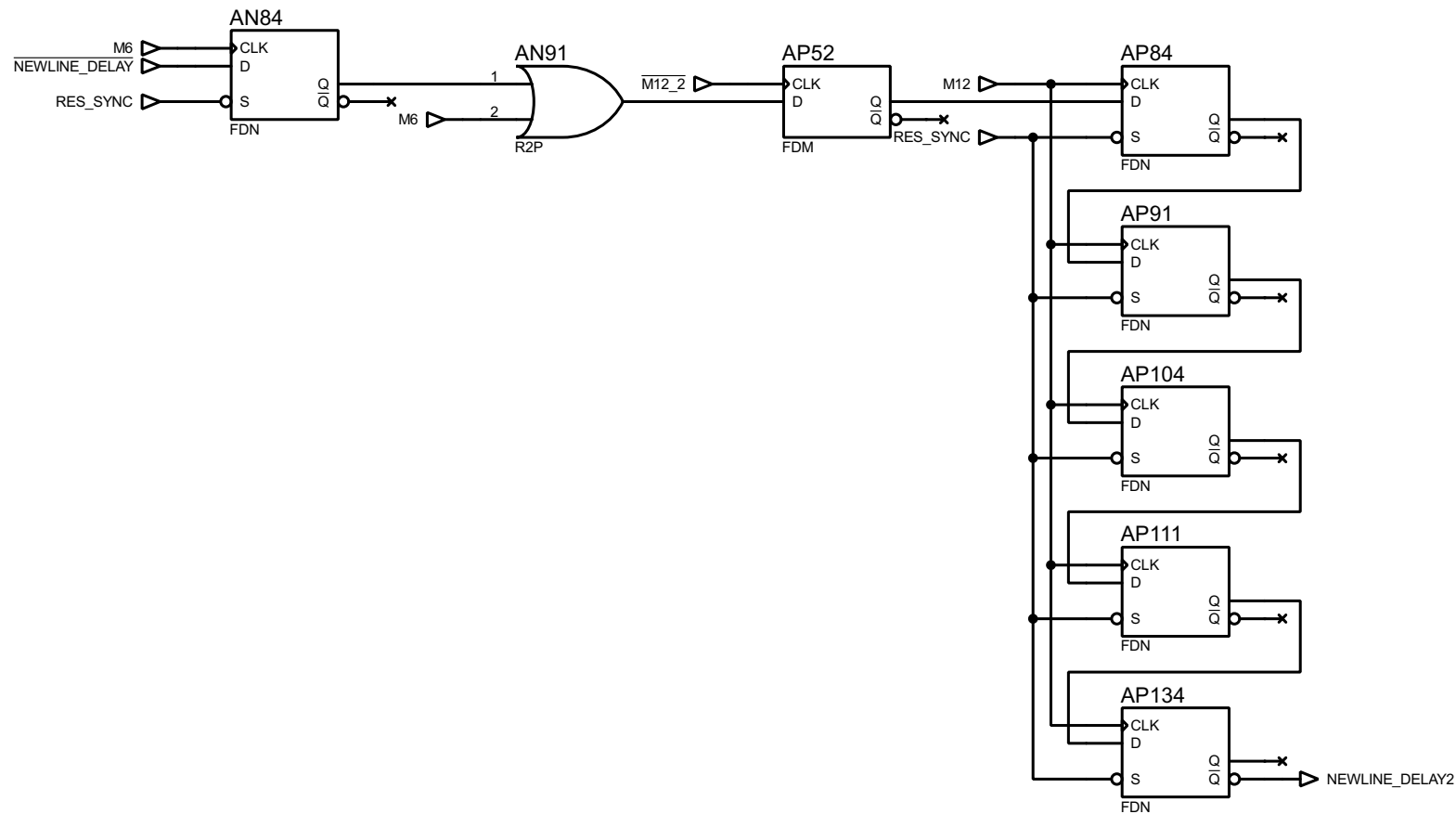
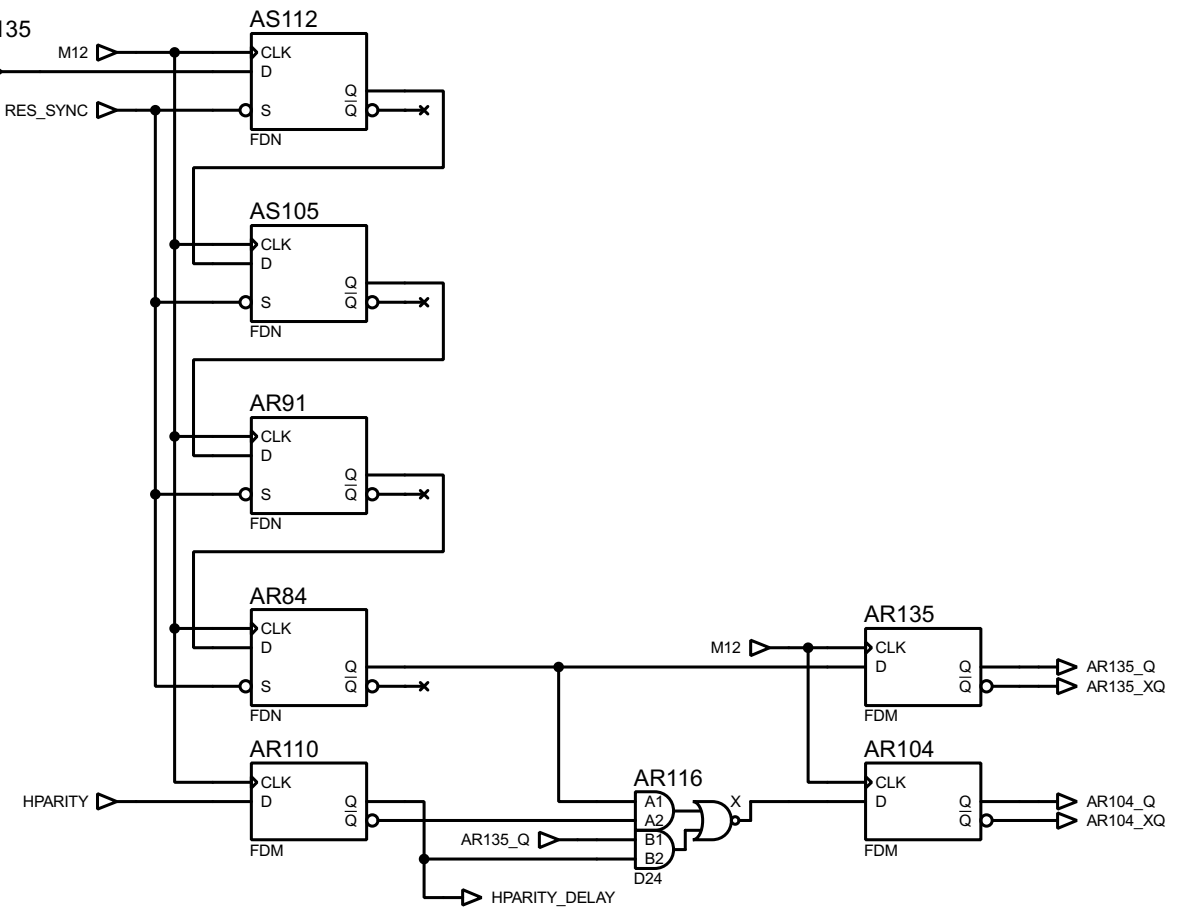
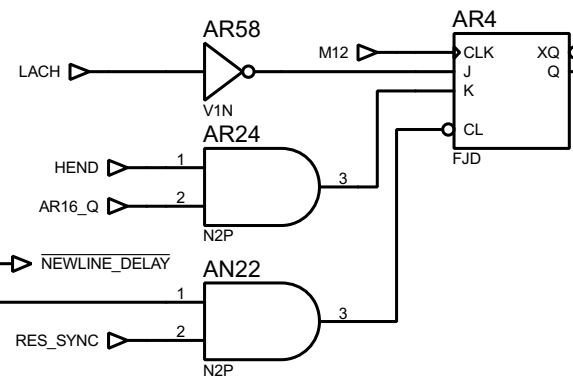
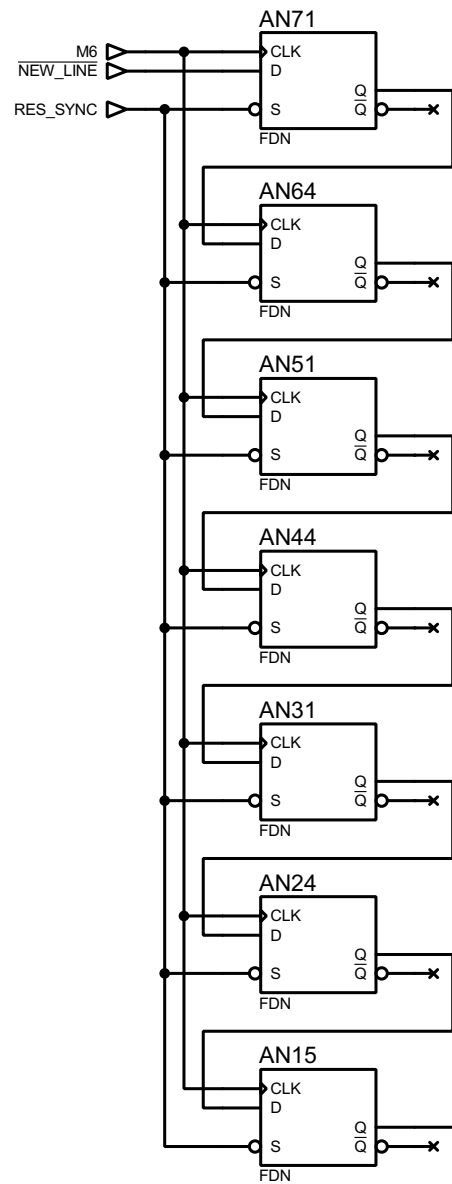
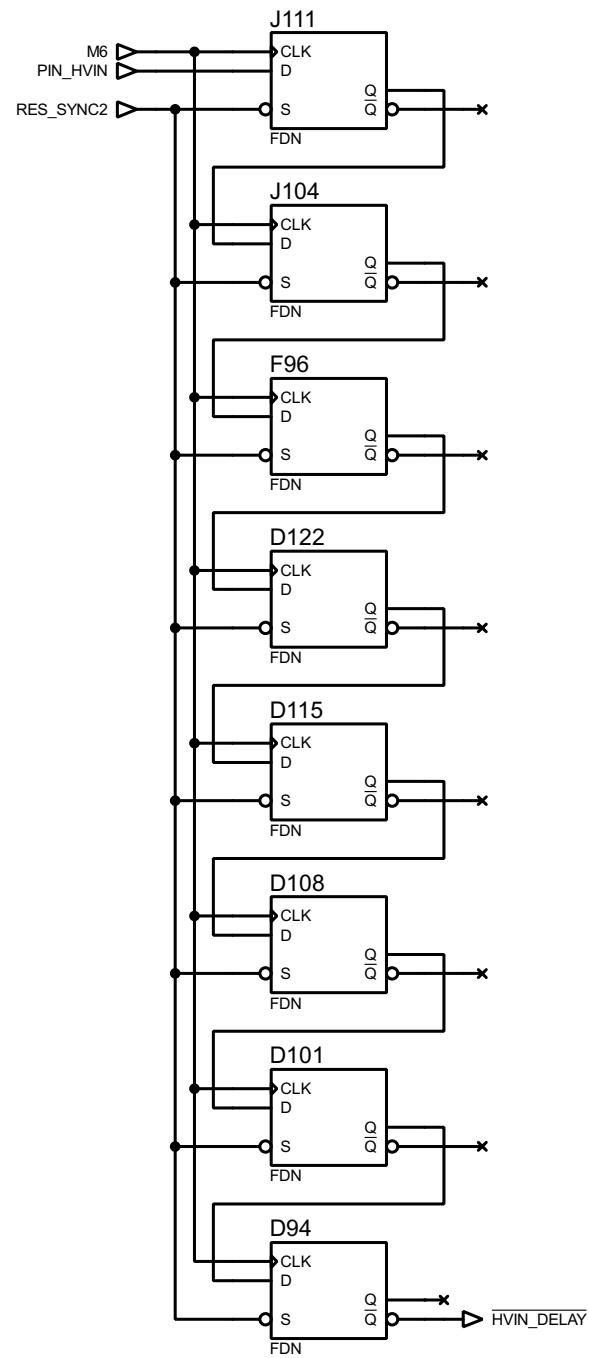


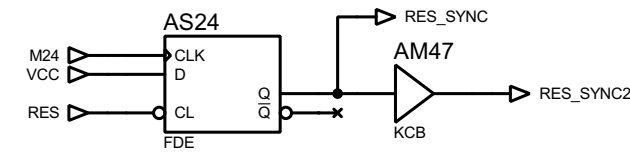






Catch palette # from OC*
Load sprite xpos
Load OHF hflip bit



[illegible]