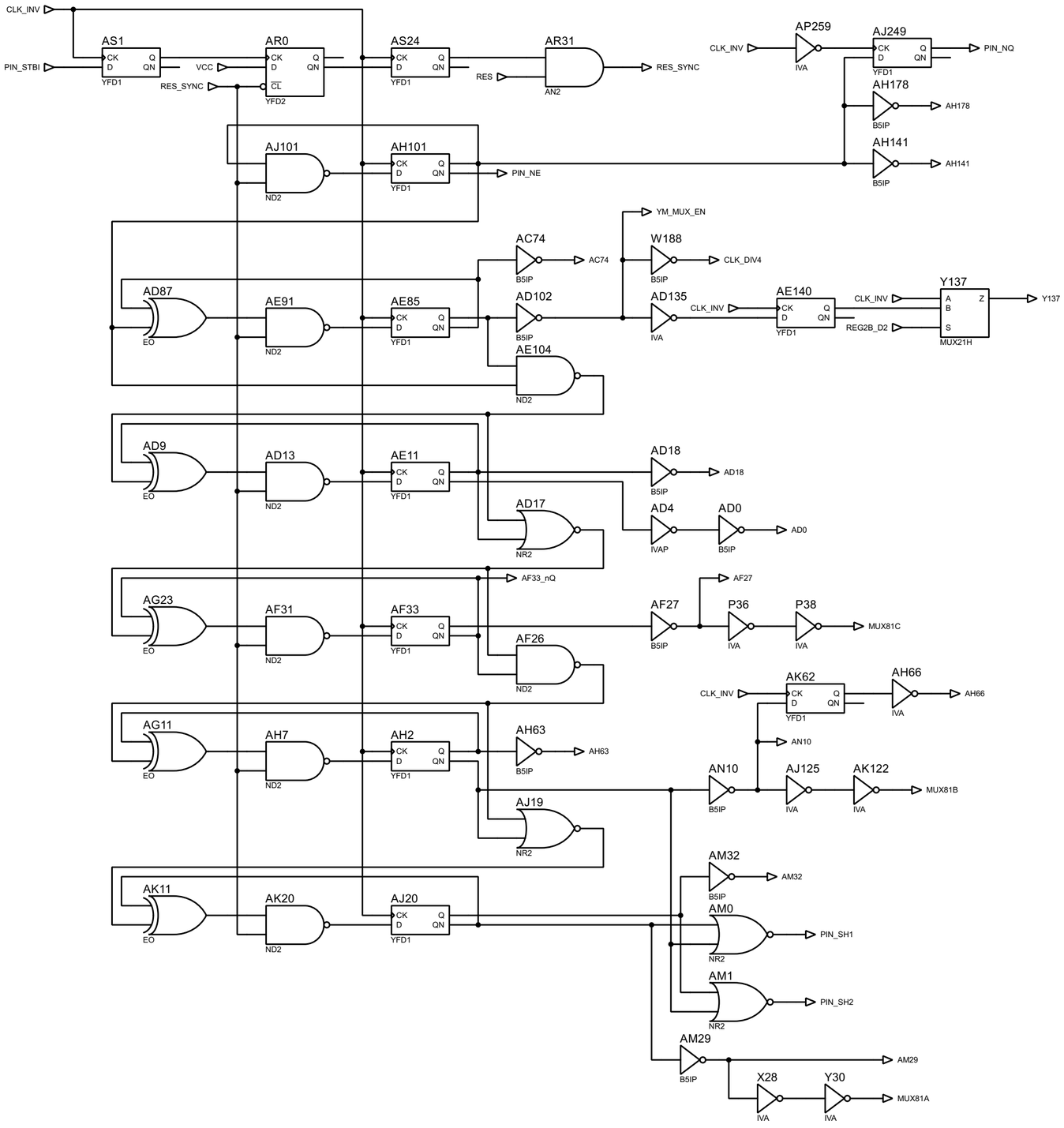
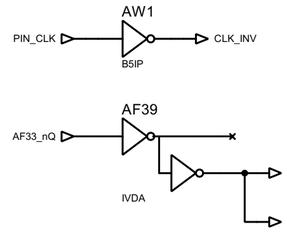
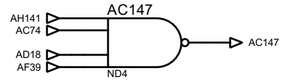
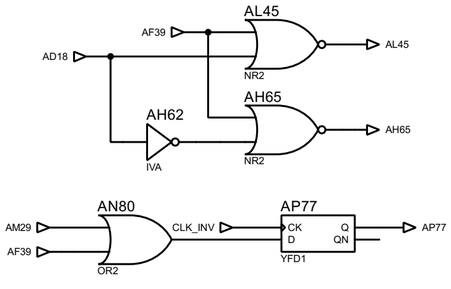
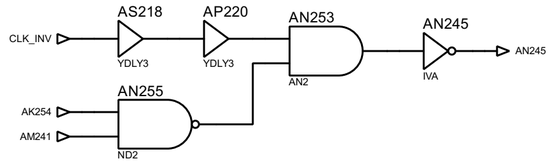
```
Clock distribution:
AH141      /2 invert
AC74       /4
AD18 AD0   /8
AF27       /16 invert
AN10       /32
AH63       /32 invert
AM29 AM32  /64 invert
```











TITLE: Konami 053260 CLOCKS	DATE: 9/19/2025
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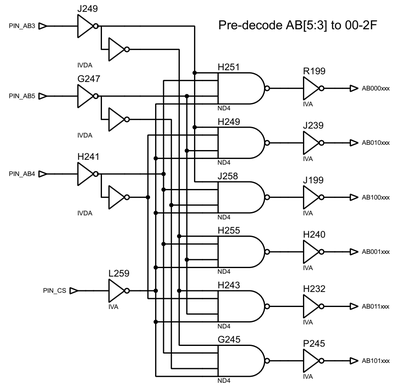
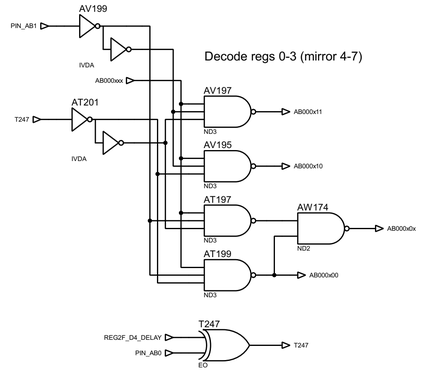


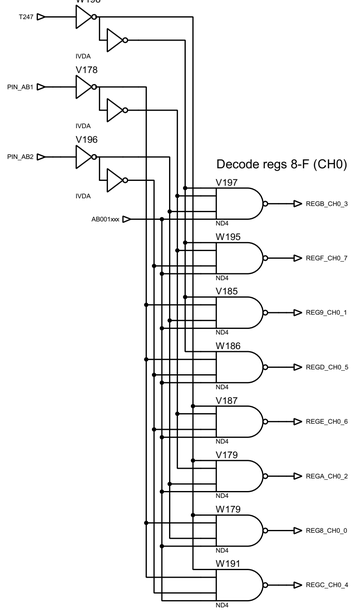
W198

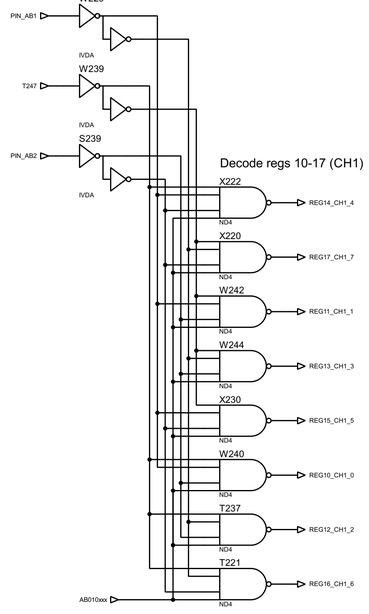


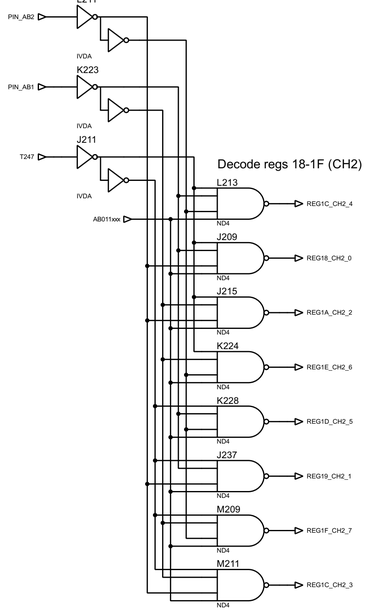
L211

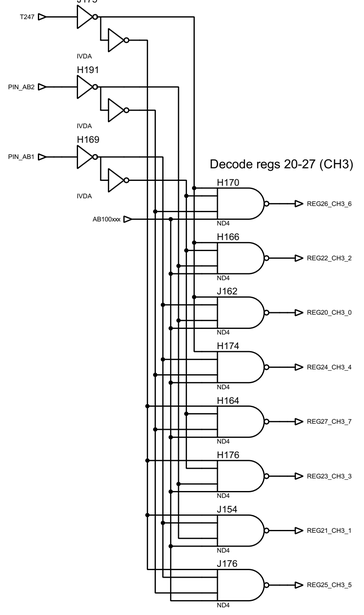
J175

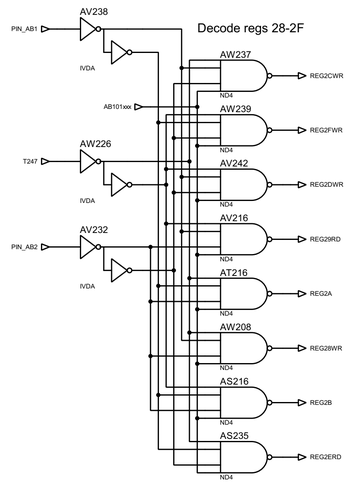
```
Reg
00: Sub-to-main A     WR
01: Sub-to-main B     WR
02: Main-to-sub A     RD
03: Main-to-sub B     RD
04: Mirror of 0 ?
05: Mirror of 1 ?
06: Mirror of 2 ?
07: Mirror of 3 ?

4x the following group (08-27)
08: Pitch low         WR
09: [3:0] Pitch high  WR
0A: Length low        WR
0B: Length high       WR
0C: Start low         WR
0D: Start middle      WR
0E: [4:0] Start high  WR
0F: [6:0] Volume      WR

28: [3:0] key on      WR
    [7:4] ?
29: [3:0] Ch status   RD
2A: [7:4] sample format, [3:0] loop en
2B: Test modes
2C: [7:4] CH1 pan, [3:0] CH0 pan
2D: [7:4] CH3 pan, [3:0] CH2 pan
2E: ROM data
2F: 0: ROM read en
    1: Enable sound output
    2: Enable aux input ?
    3: ?
```











TITLE: Konami 053260 ADDR DECODE	DATE: 9/19/2025
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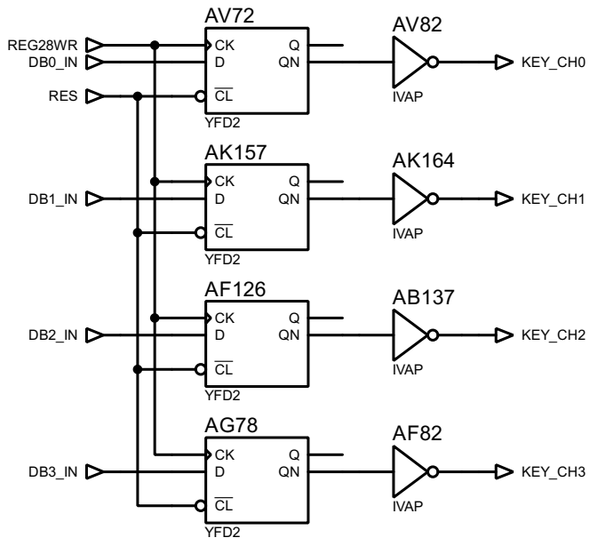
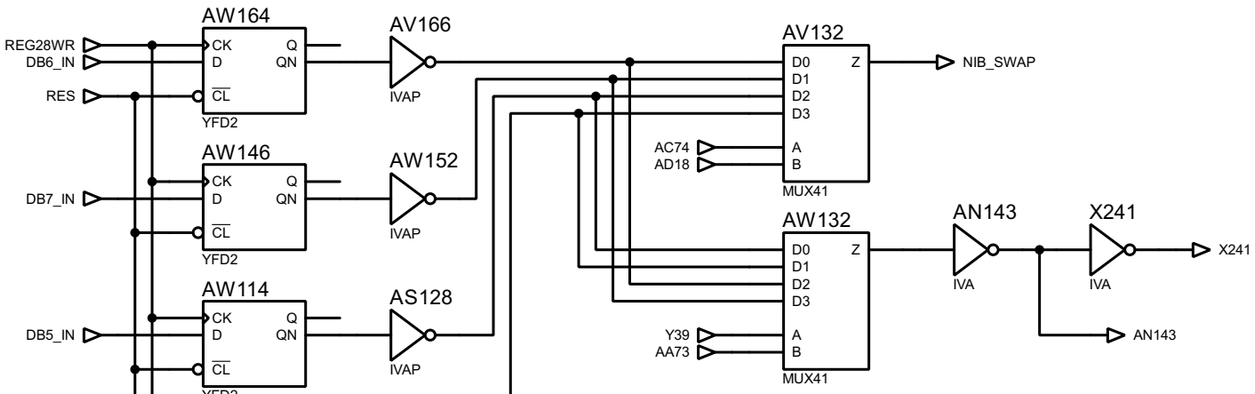
Reg key on/off



Play channel backwards ?



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Konami 053260 REG 28	9/19/2025
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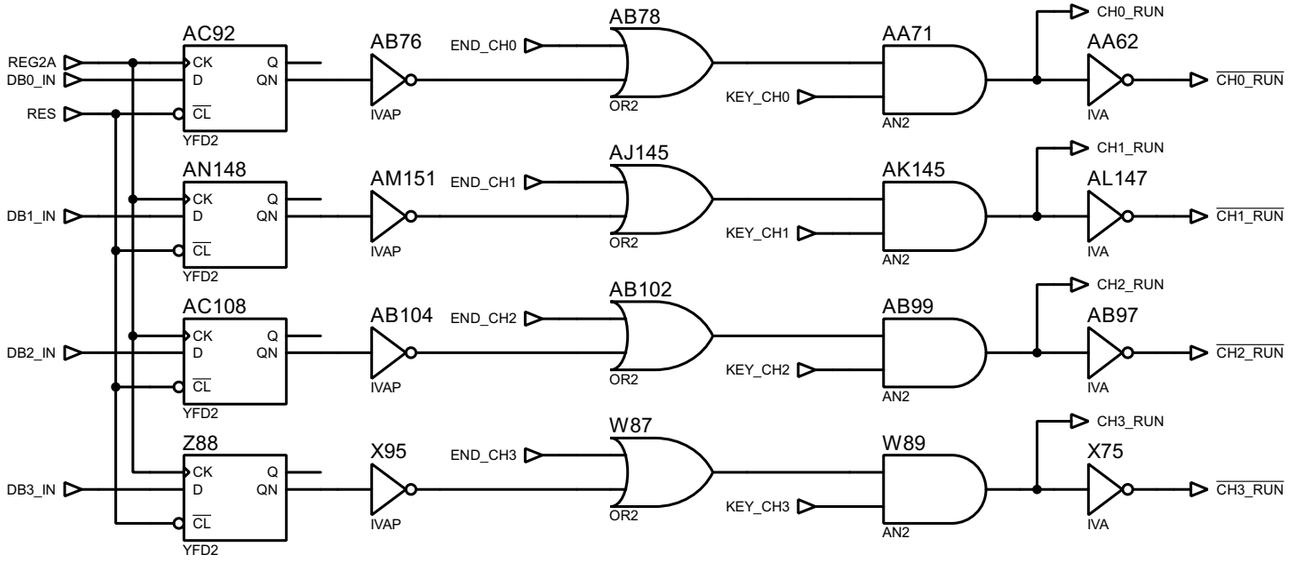
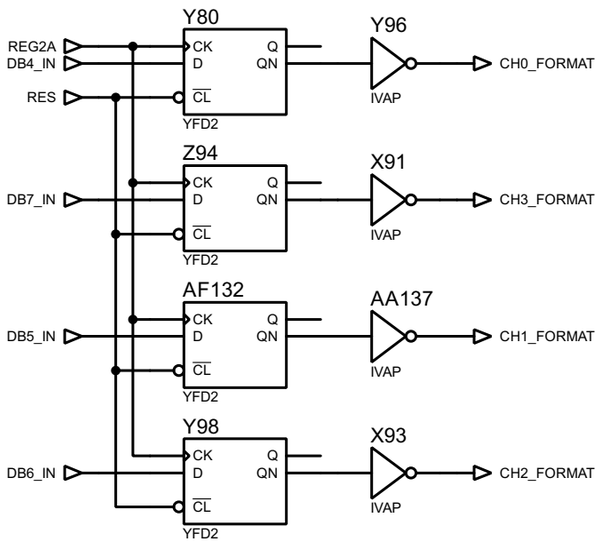
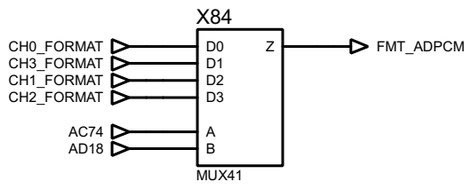
Loop flags

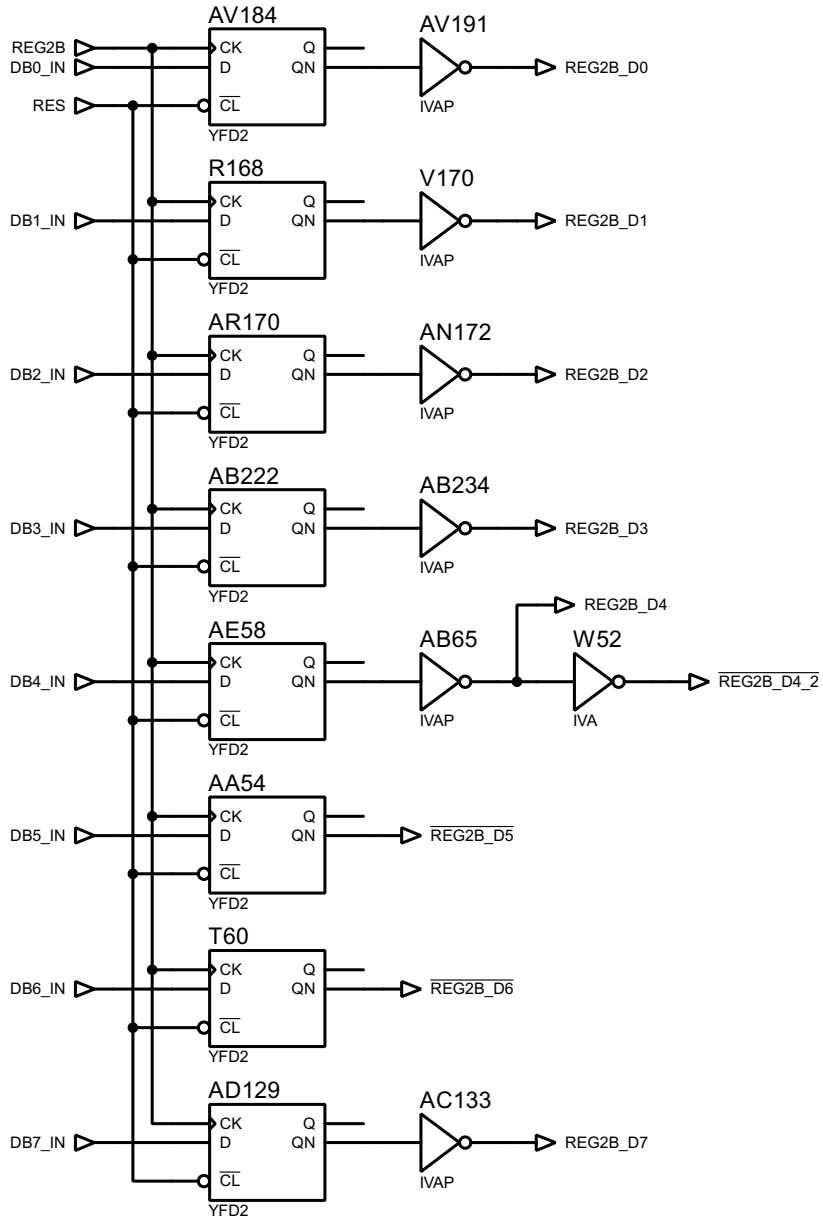


Format flags





TITLE: Konami 053260 REG 2A	DATE: 9/19/2025
BY: Sean Gonsalves REV: A	PAGE: 4/34



Test stuff. Setting this register to anything other than zero may cause irreversible damage.

0: Bypass counters
1: ROM address mux select
2: Multiplier input select
3: Clock related
4: Enable channel selection
5: Channel select A
6: Channel select B
7: Clock for some ROM addr

TITLE:	DATE:
Konami 053260 REG 2B	9/19/2025
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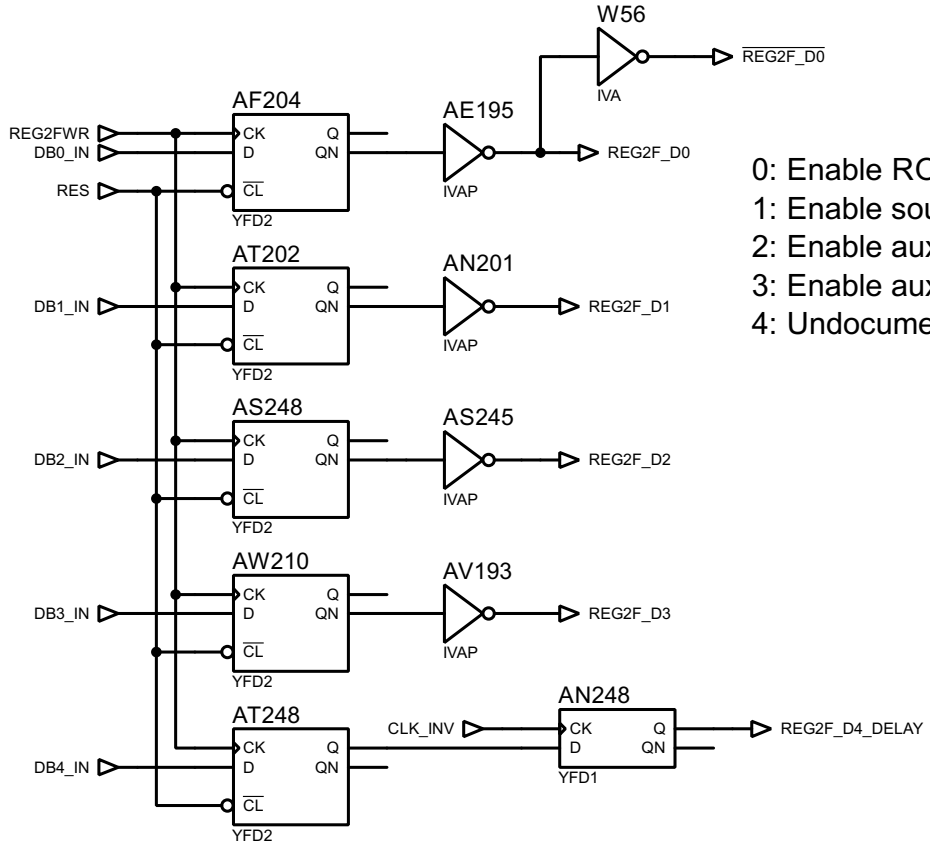

0: Enable ROM read from 2E
1: Enable sound output
2: Enable aux input 1
3: Enable aux input 2
4: Undocumented, flip AB0 input ?

TITLE:	DATE:
Konami 053260 REG 2F	9/19/2025
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Sample ROM to sub CPU readback

Main-to-sub registers

Sub-to-main registers

Voice status register 0x29

Deez nuts

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Konami 053260 CPU DATA	9/19/2025
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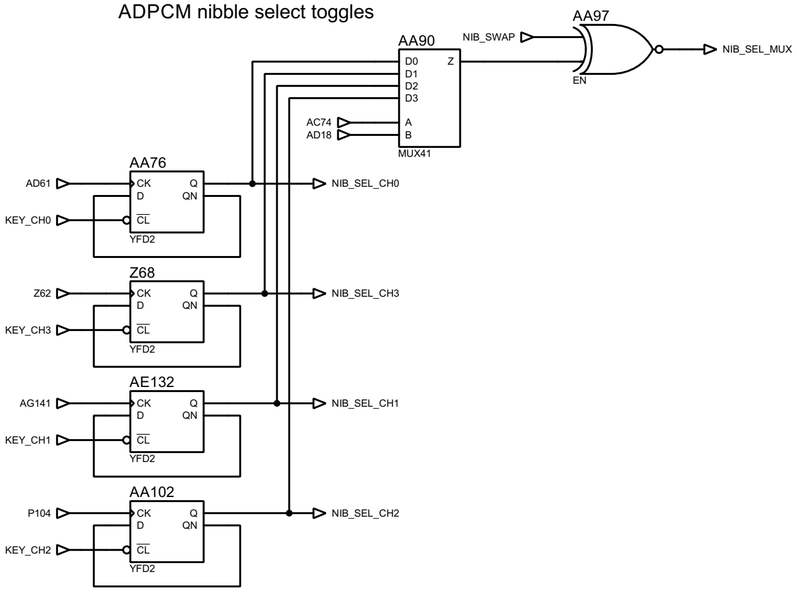
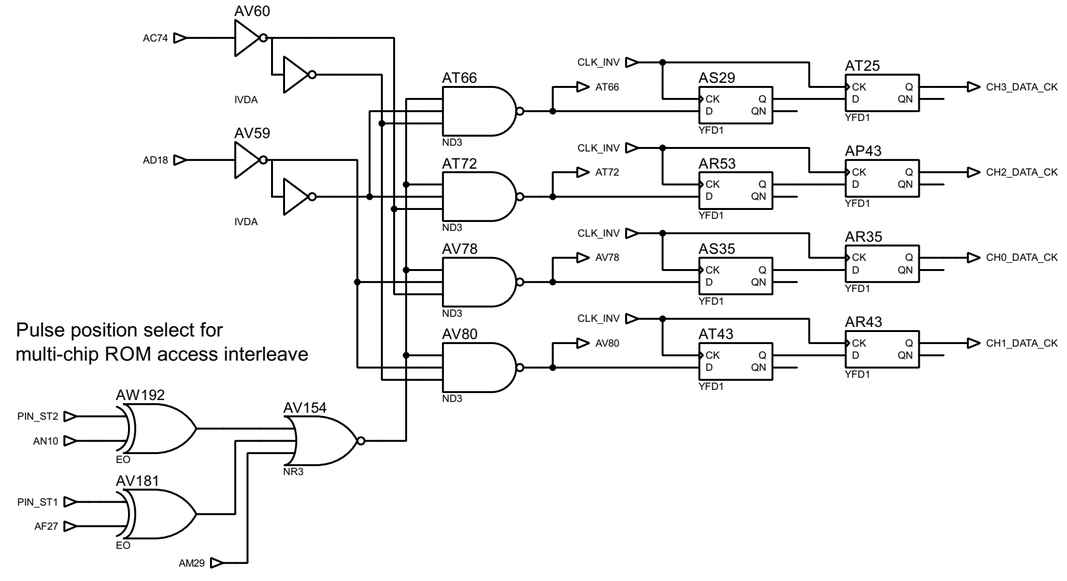
ADPCM nibble select toggles



ROM read pulse generator

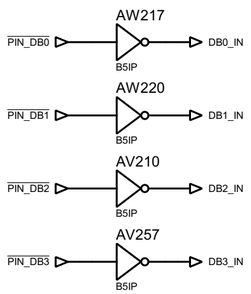


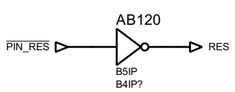
ROM data registration delay

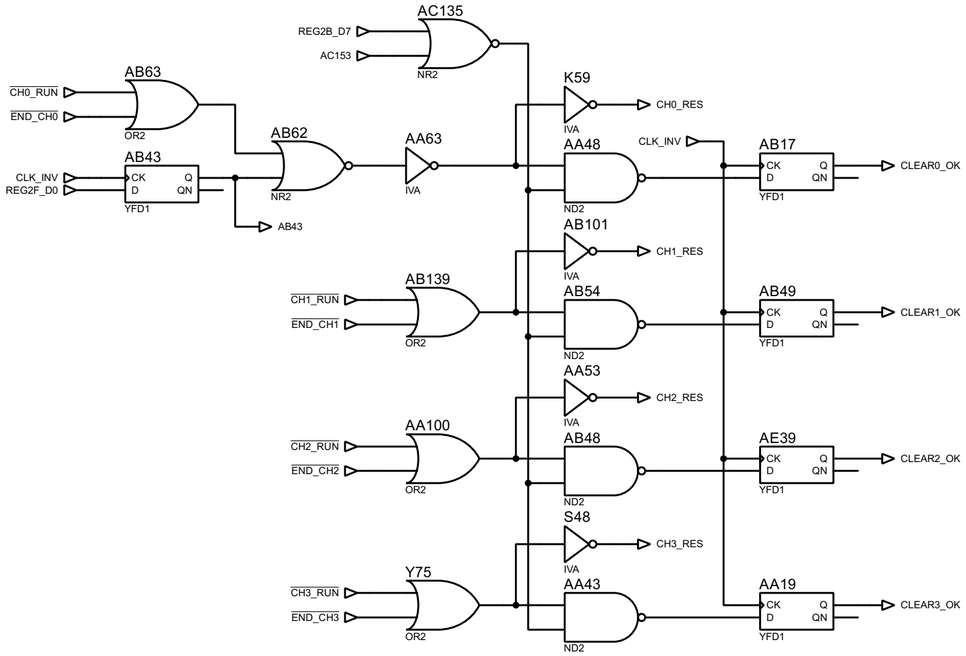

```
AN10  AF27  AV154
0     0     1
0     1     0
1     0     0
1     1     0

ST1:
AN10  AF27  AV154
0     1     0
0     0     1
1     1     0
1     0     0

ST2:
AN10  AF27  AV154
1     0     0
1     1     0
0     0     1
0     1     0

ST ST2:
AN10  AF27  AV154
1     1     0
1     0     0
0     1     0
0     0     1
```

Pulse position select for
multi-chip ROM access interleave

Input signals for pins DB4 to DB7
are direct from the IO blocks







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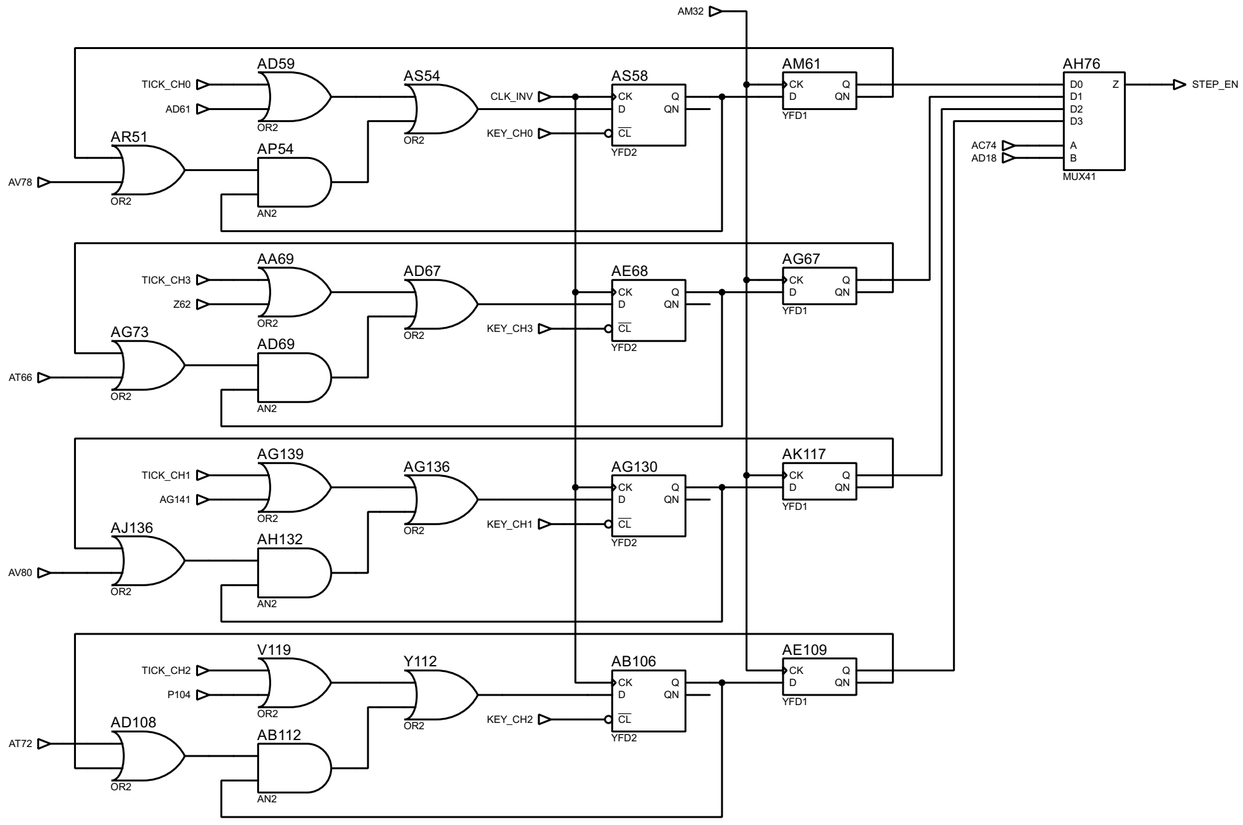

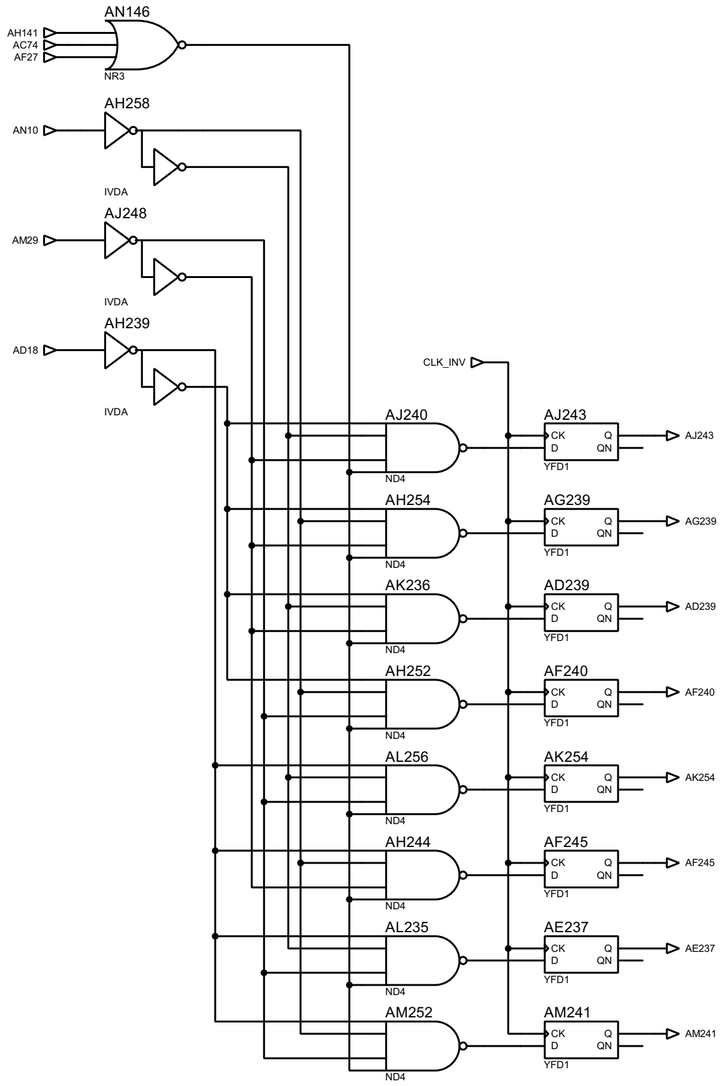

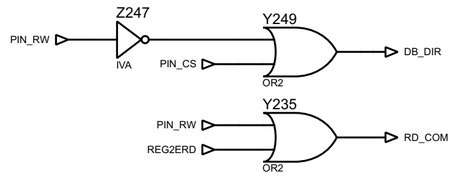

TITLE:	DATE:
Konami 053260 MISC 2	9/19/2025
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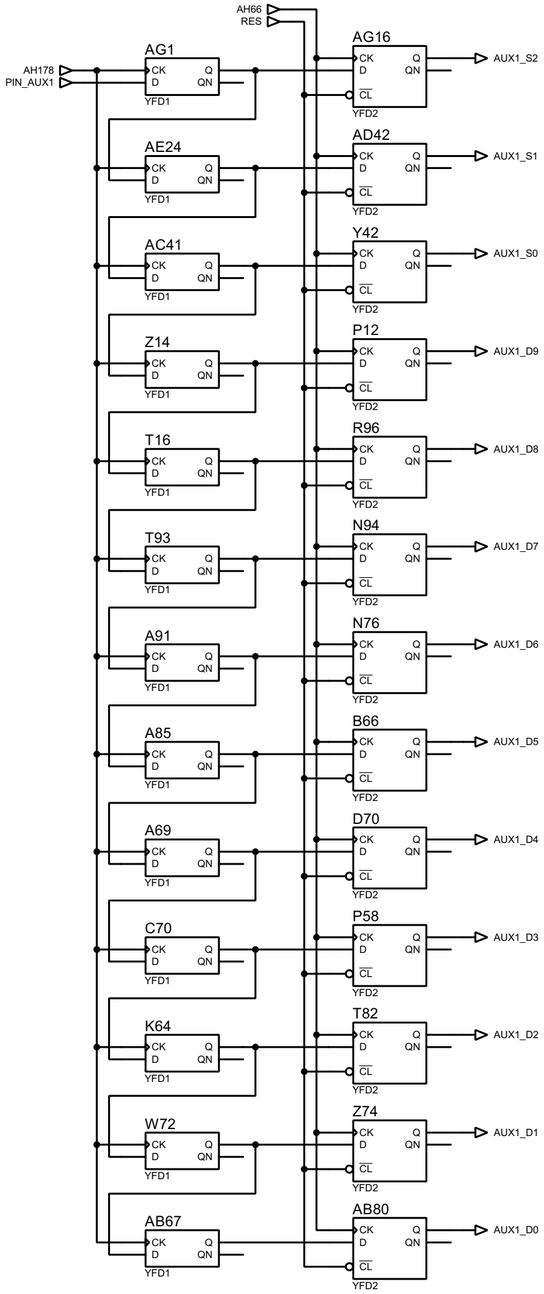

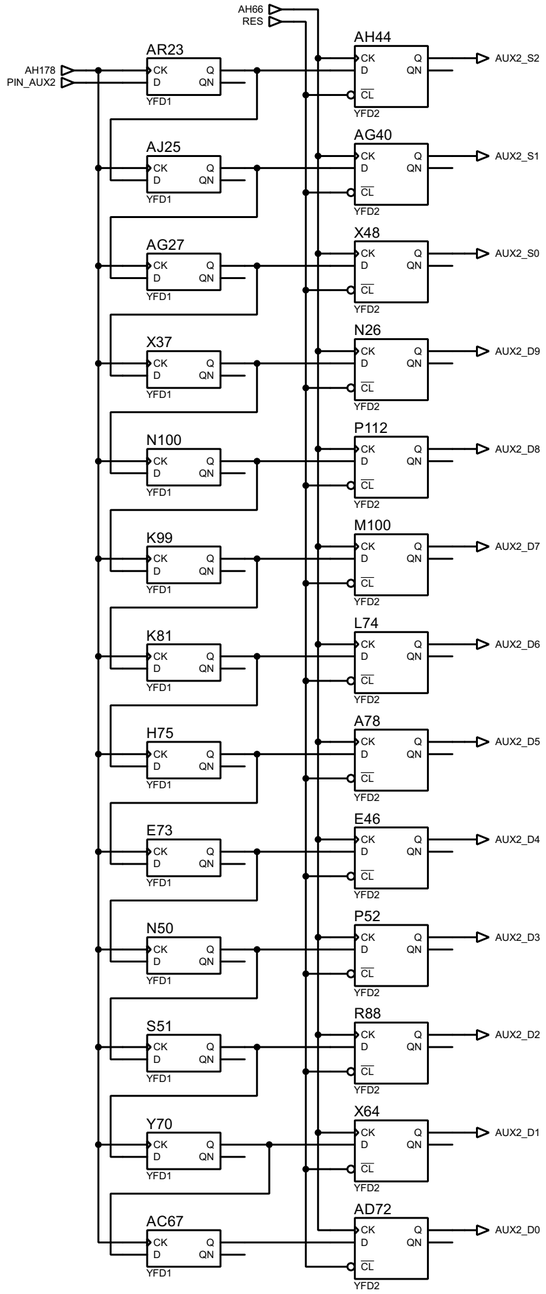

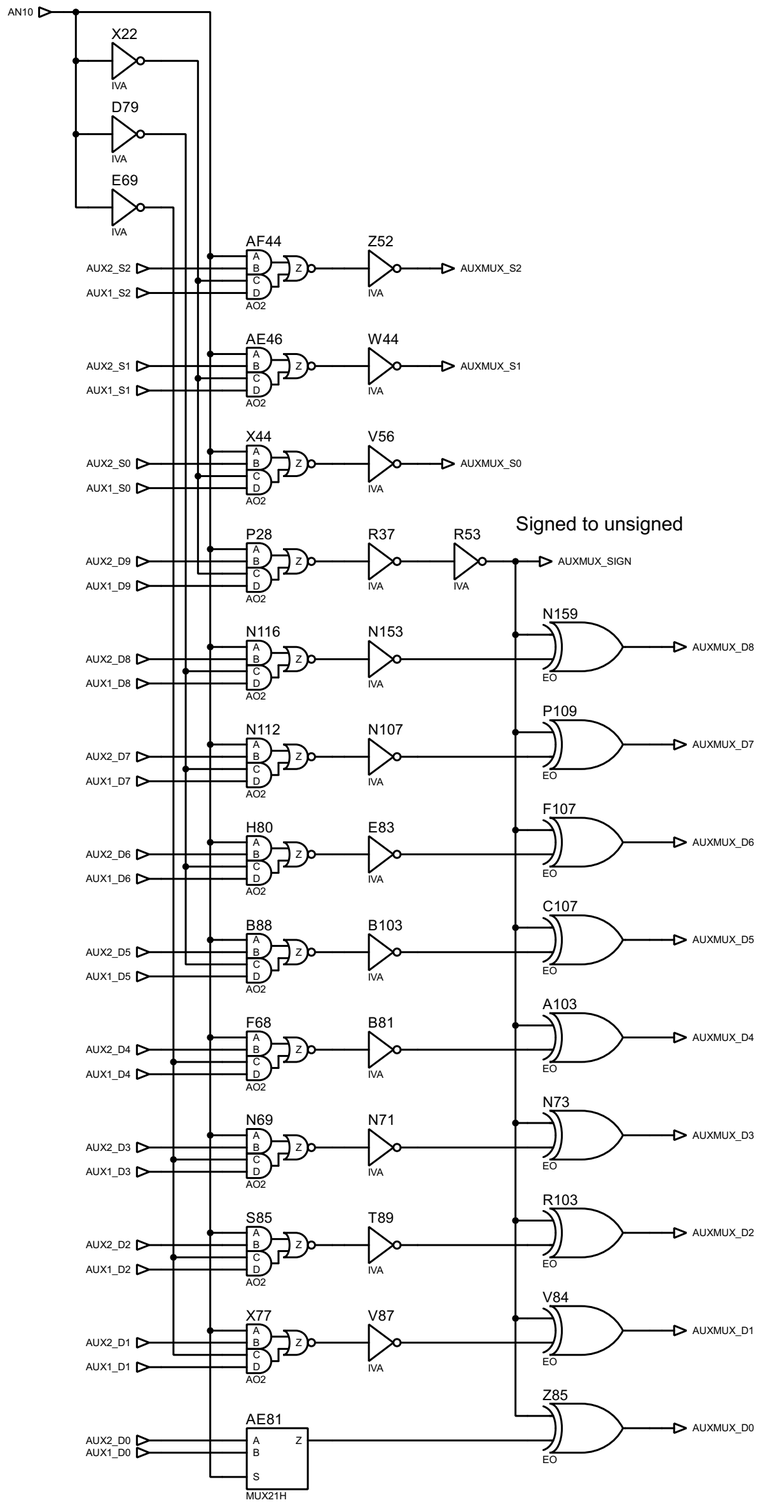

TITLE:	DATE:
Konami 053260 YM IN	9/19/2025
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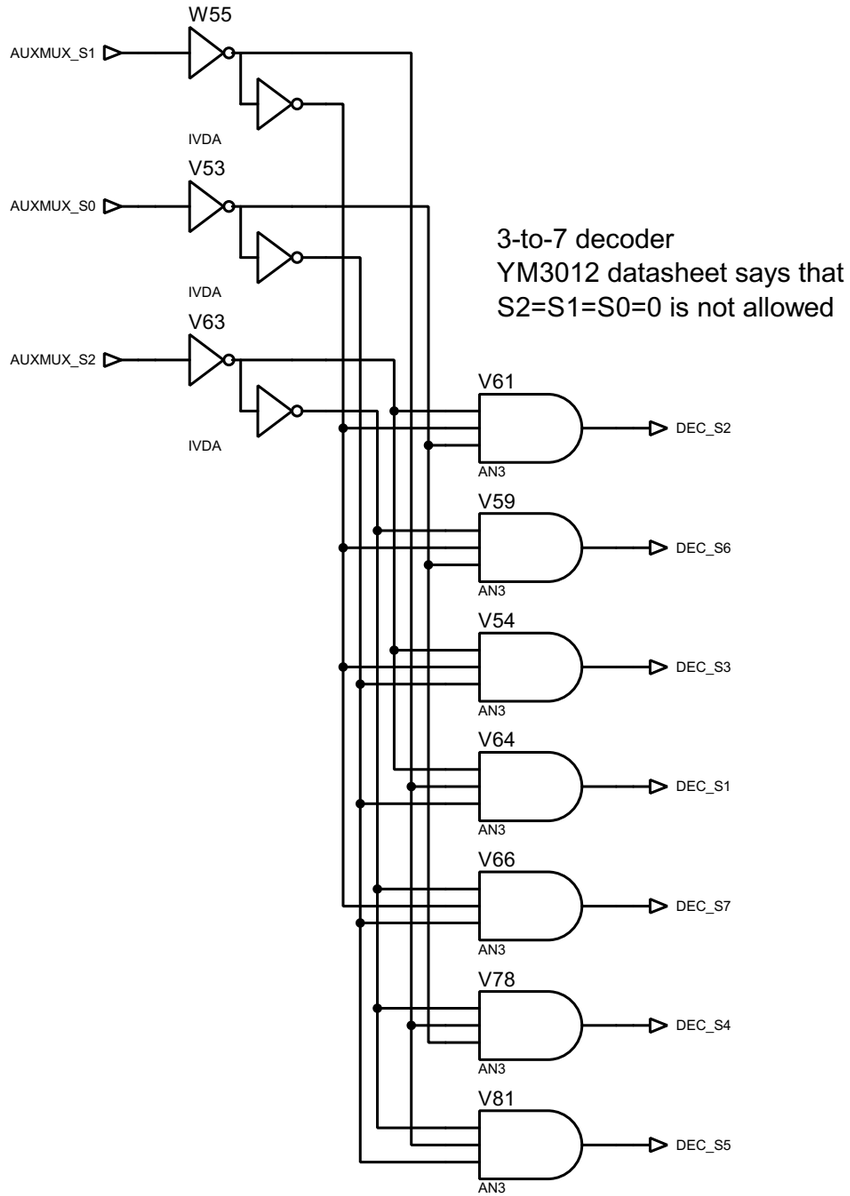

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Konami 053260 YM EXP DECODE	9/19/2025
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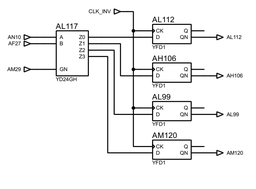
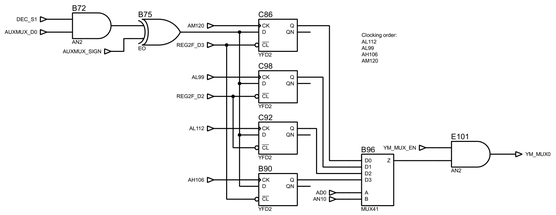
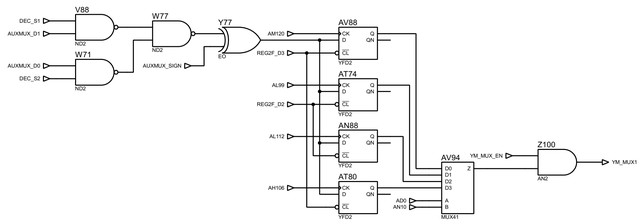
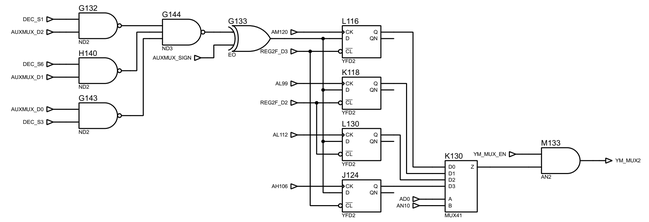
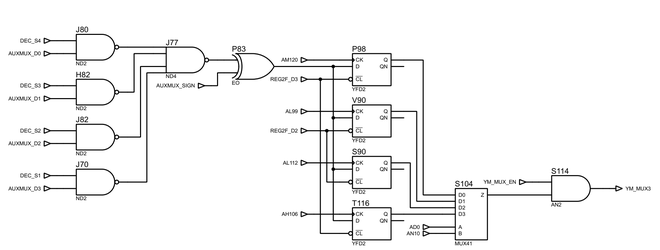
Muxes used to select AUX1/AUX2 and L/R channels ?

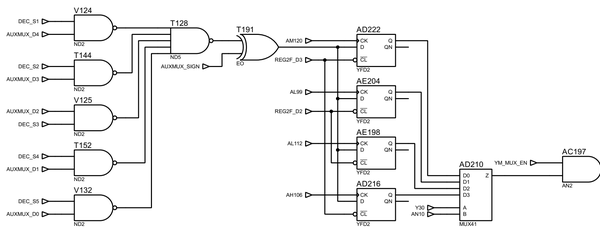


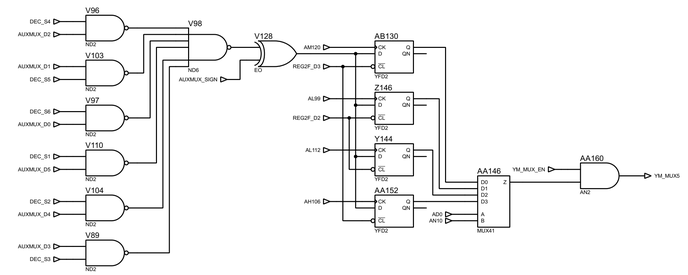


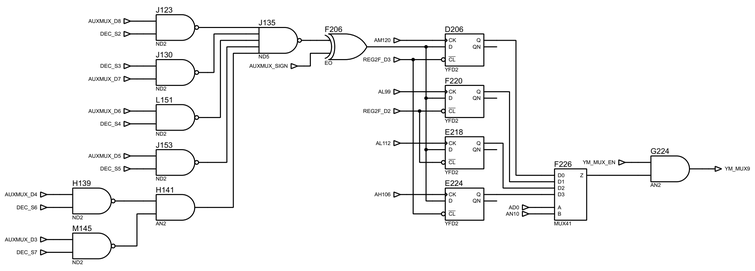


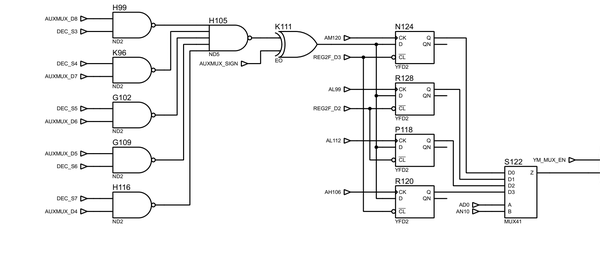


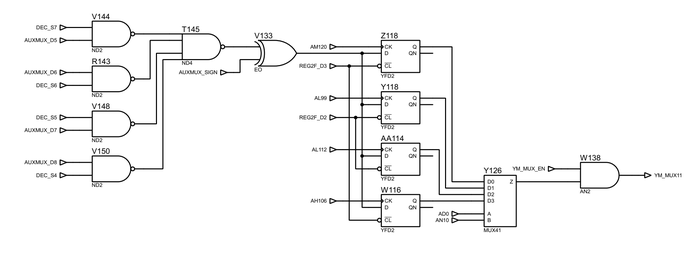












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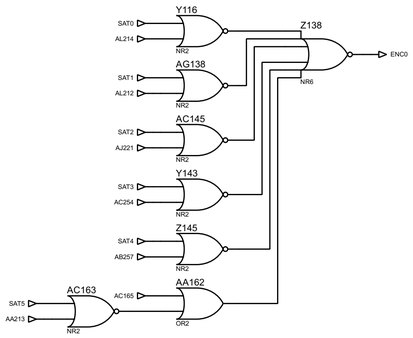

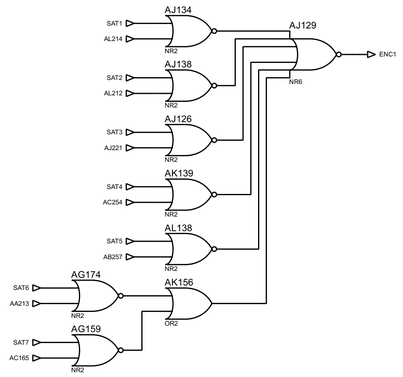

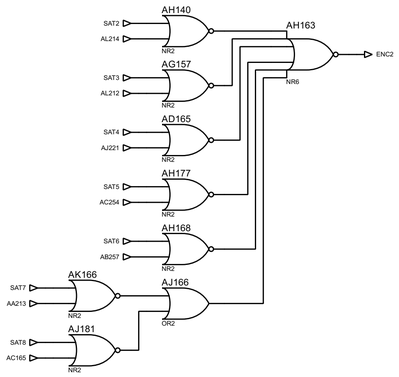

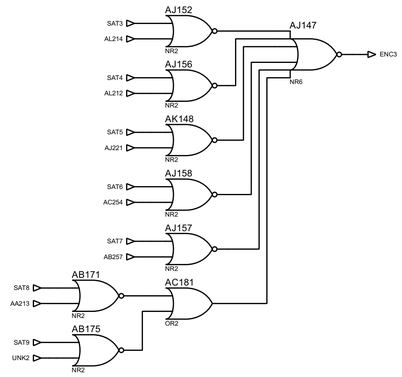

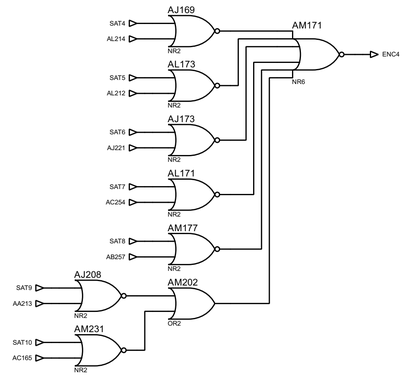

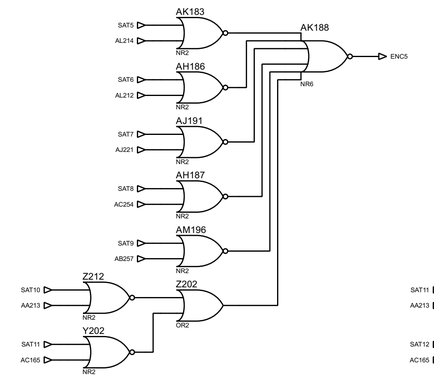

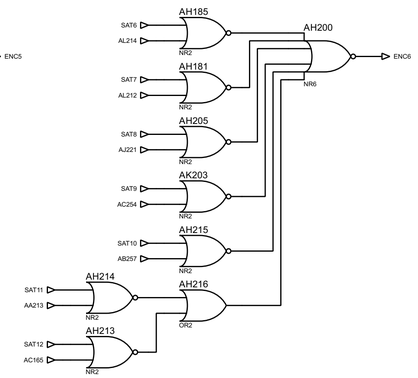

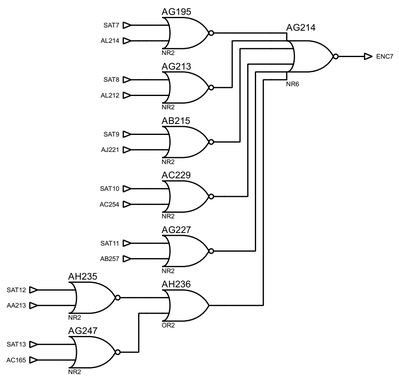

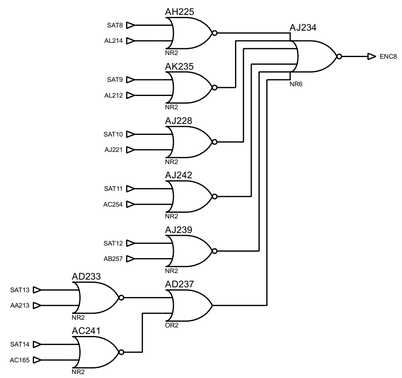

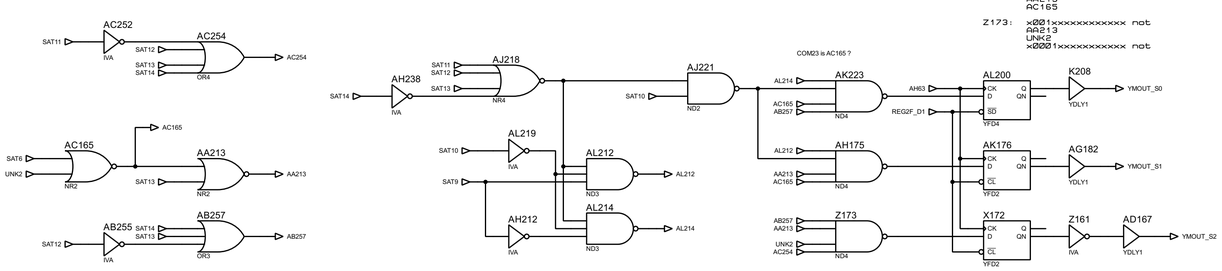


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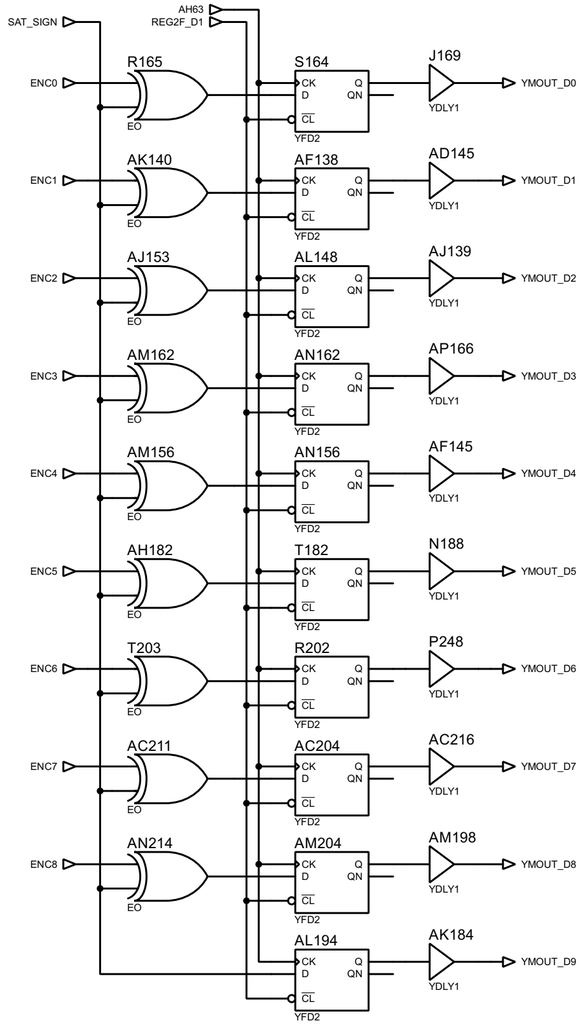

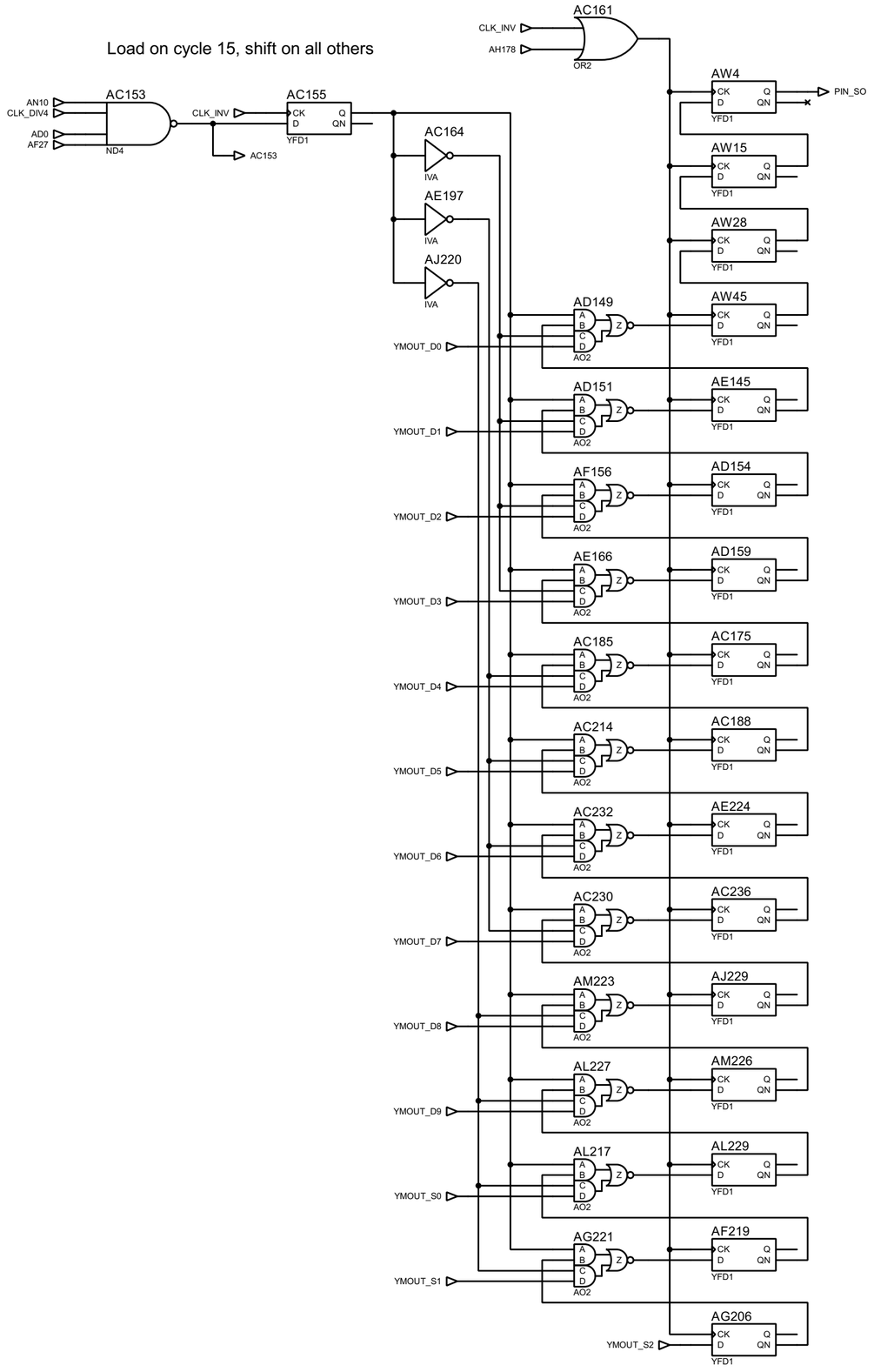

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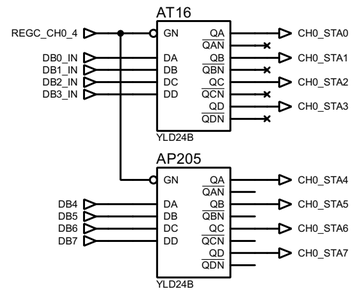

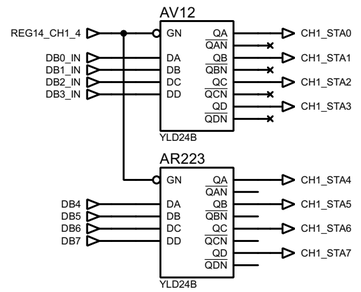

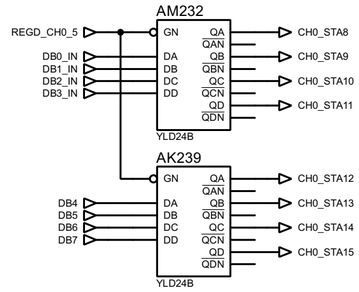

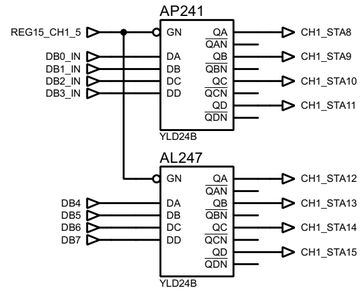

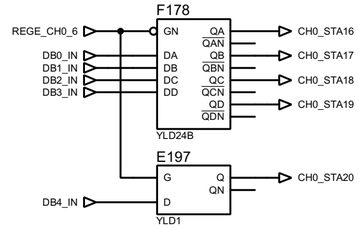

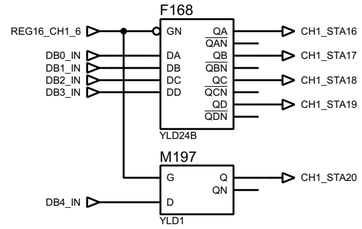

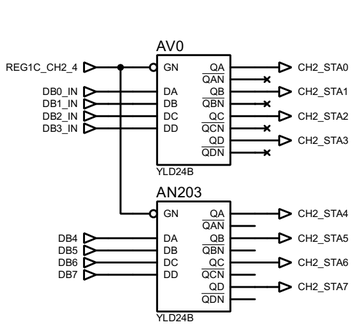

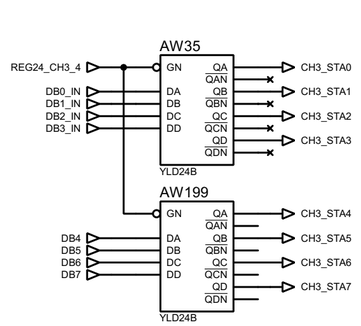

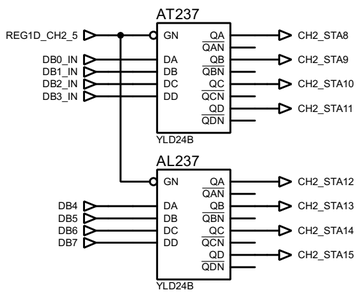

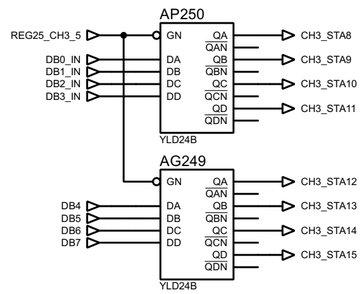

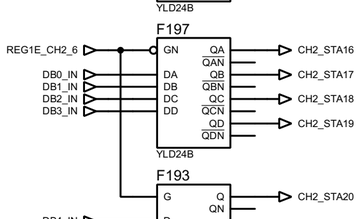

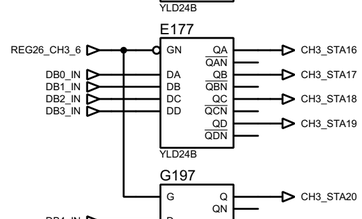

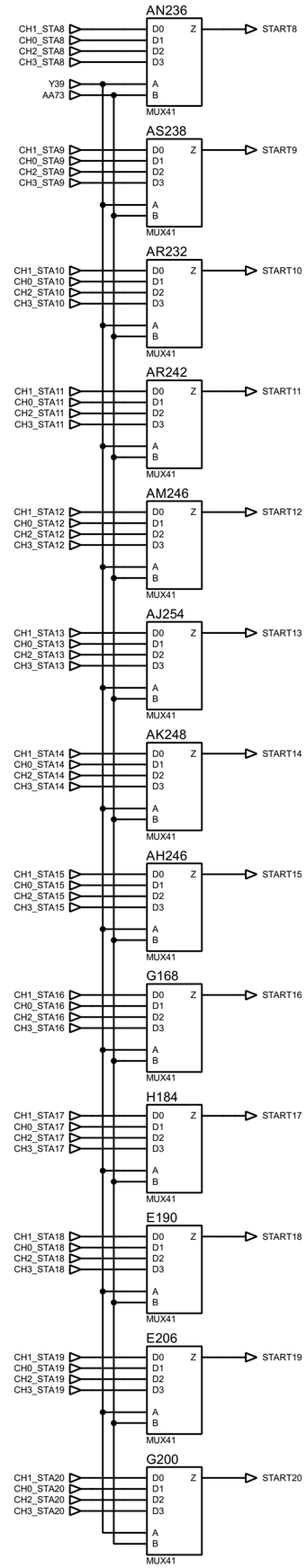

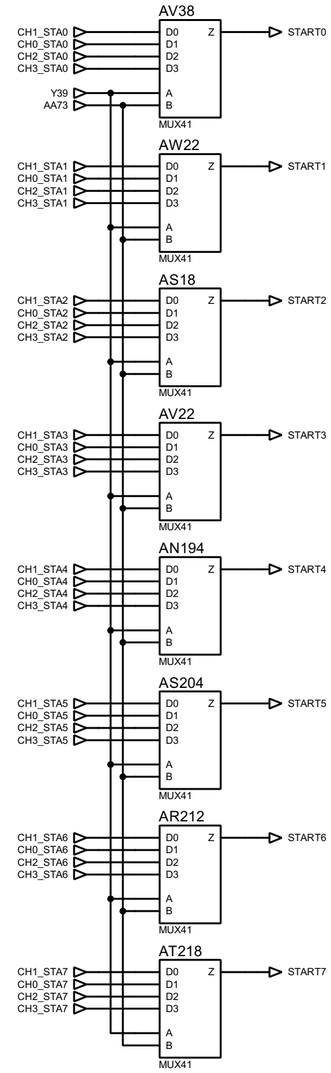

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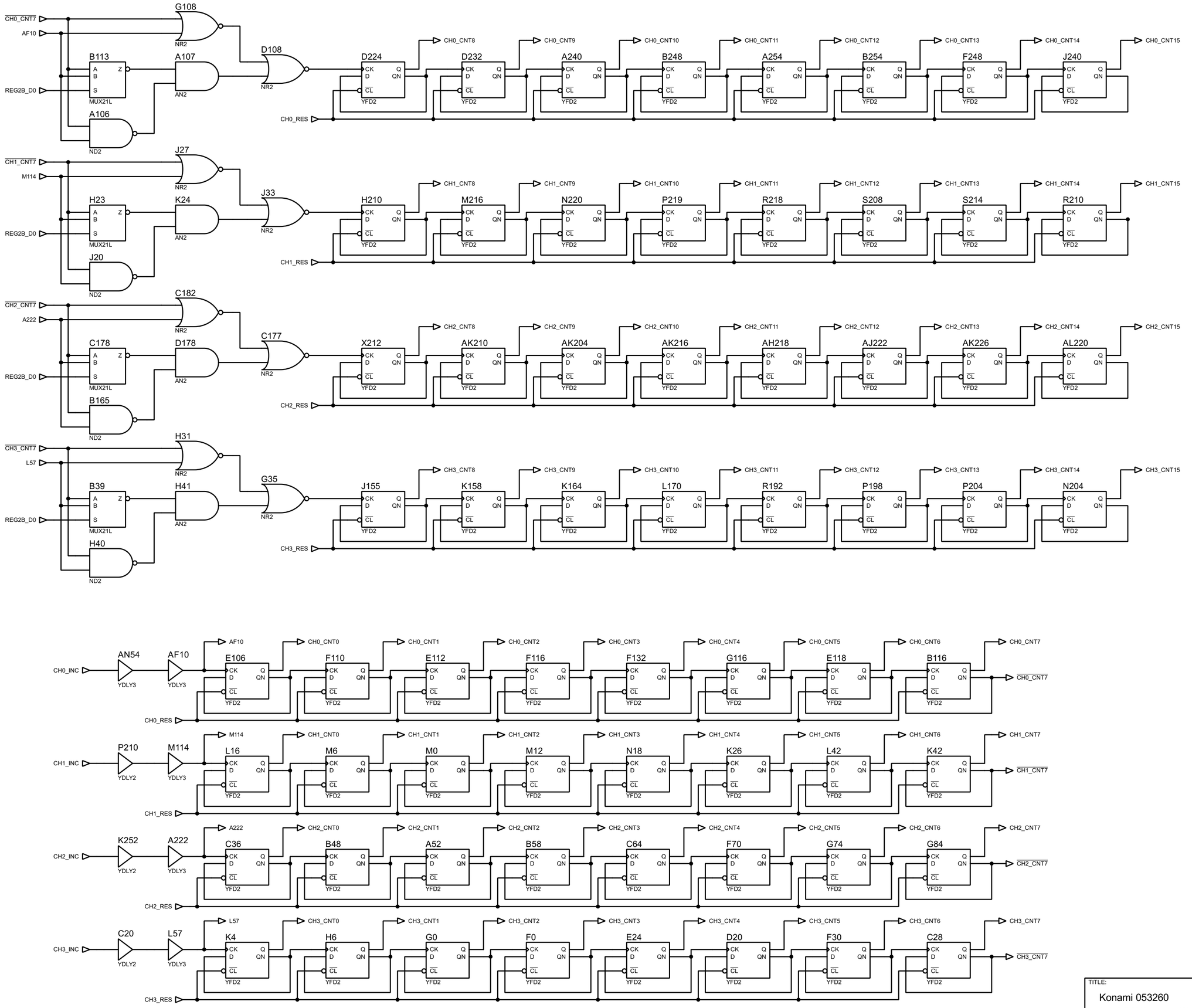

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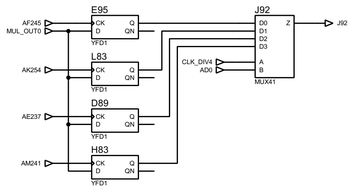

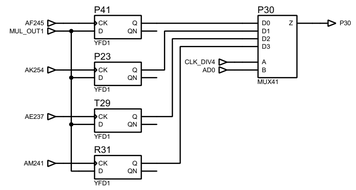

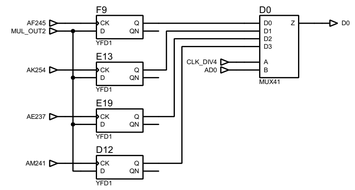

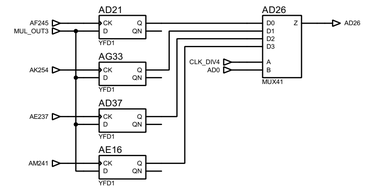

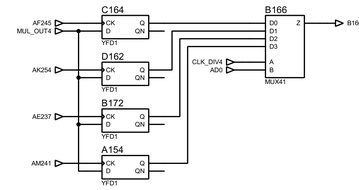

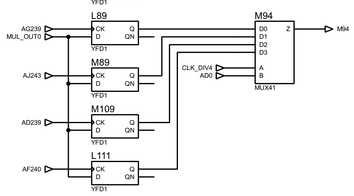

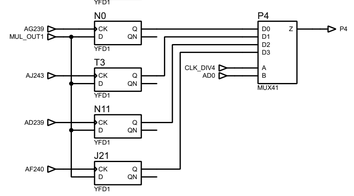

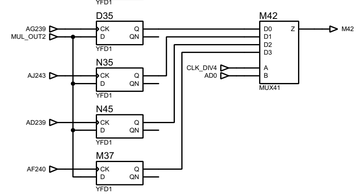

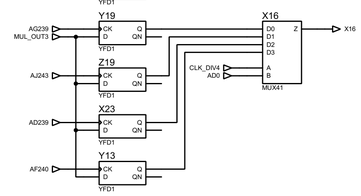

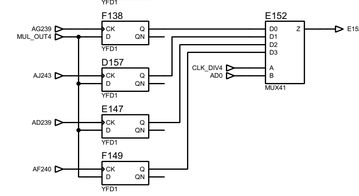

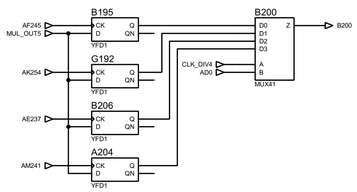

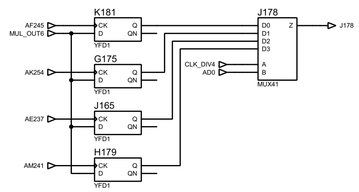

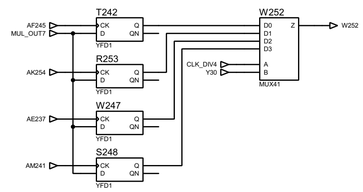

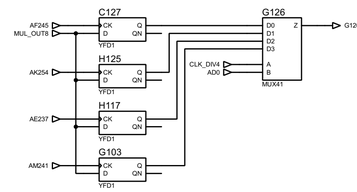

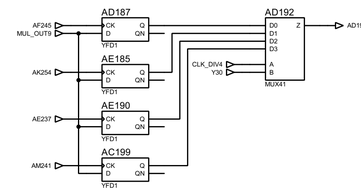

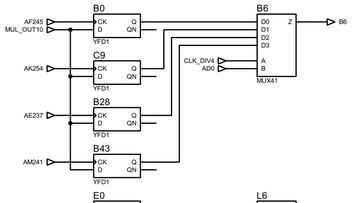

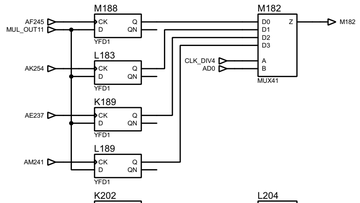

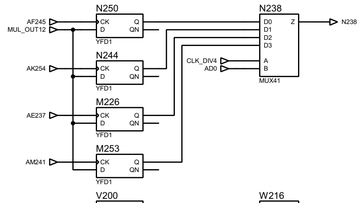

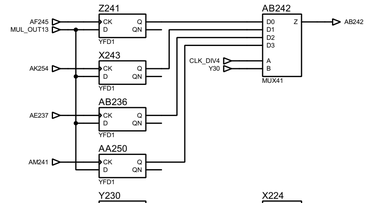

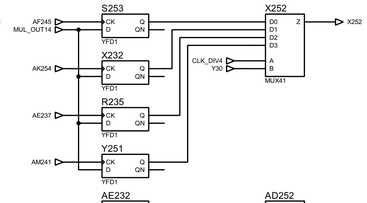

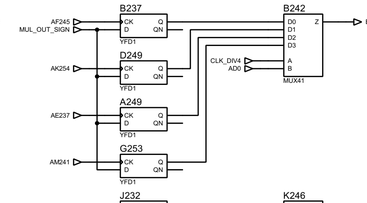

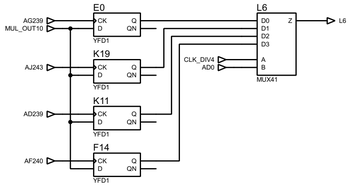

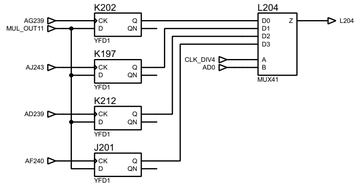

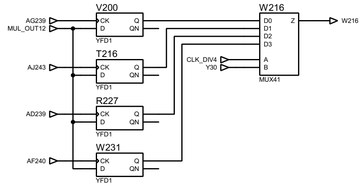

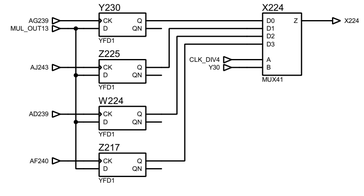

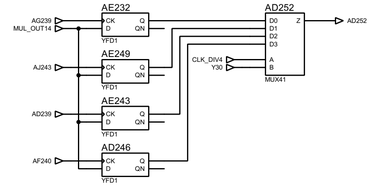

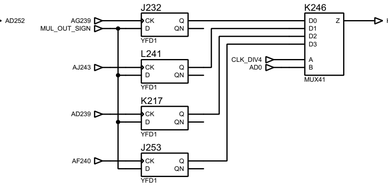

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TITLE: Konami 053260 MUL REGS		DATE: 9/19/2025	
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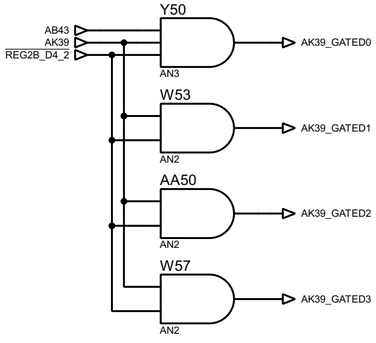
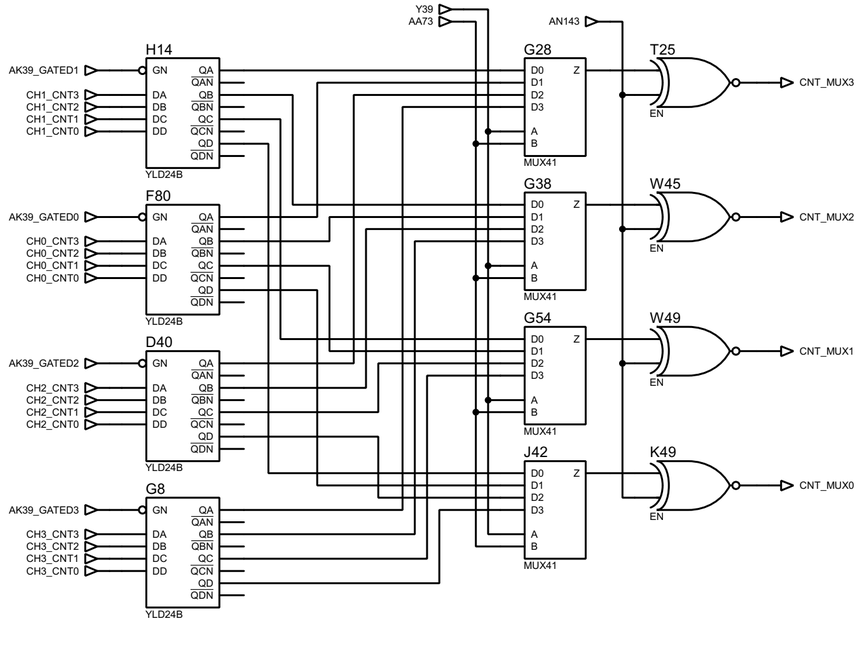
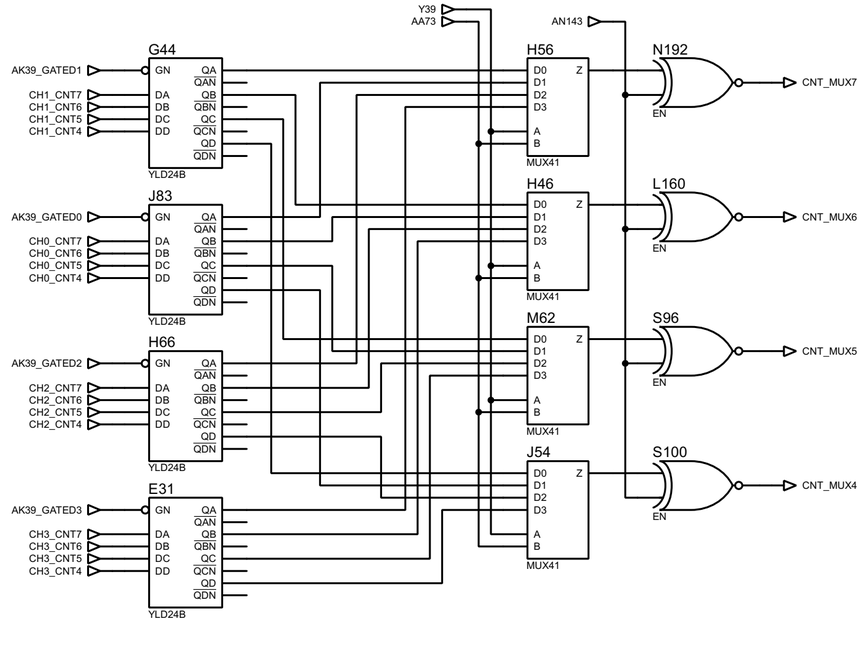
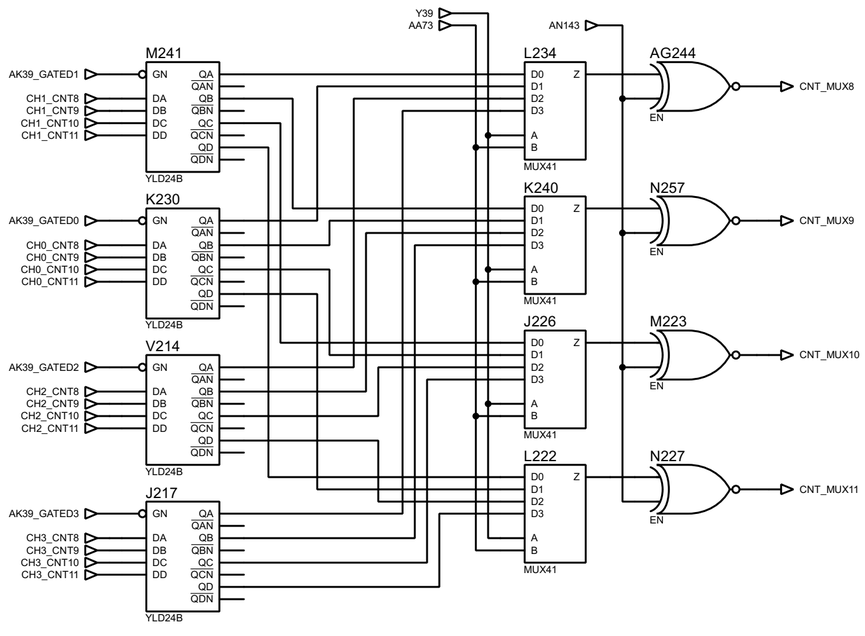
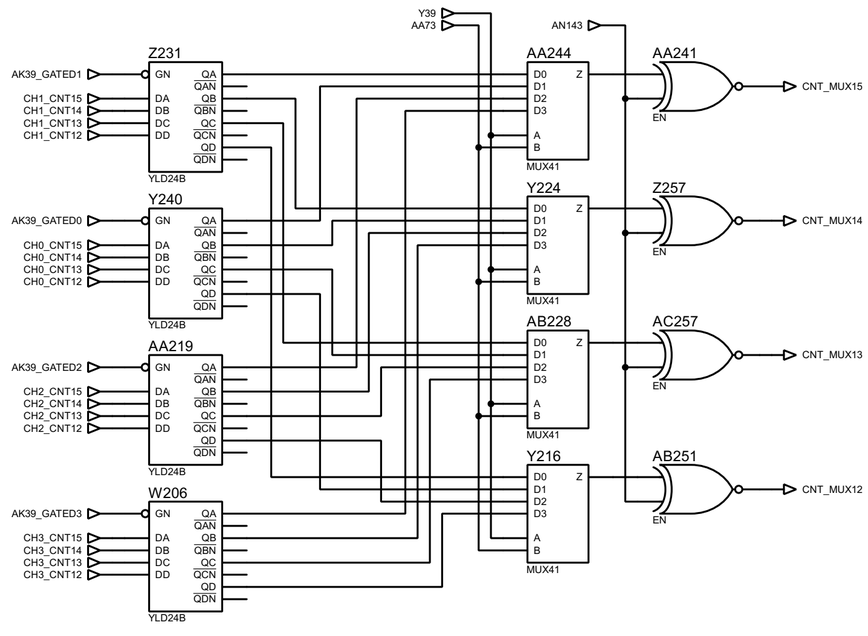


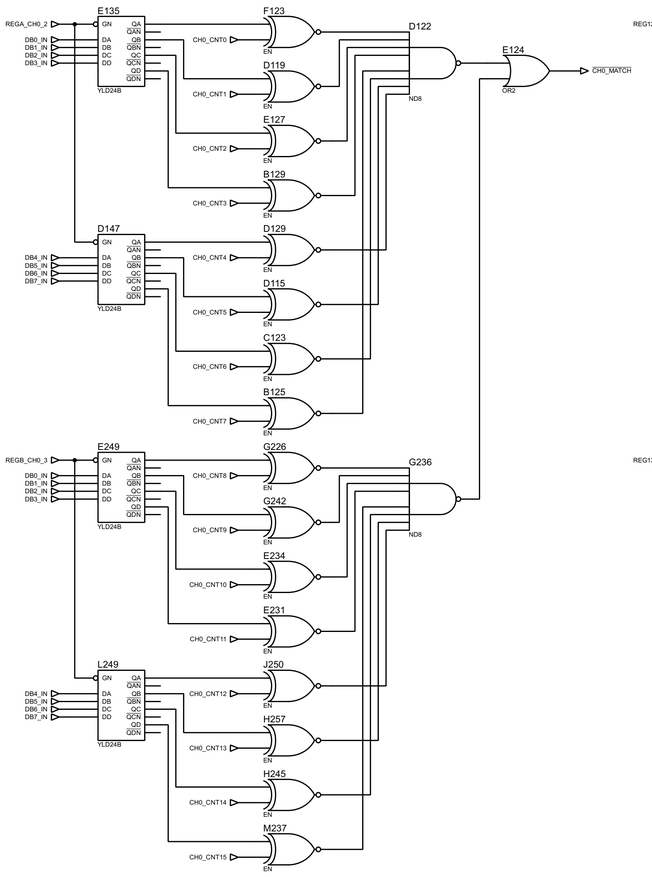


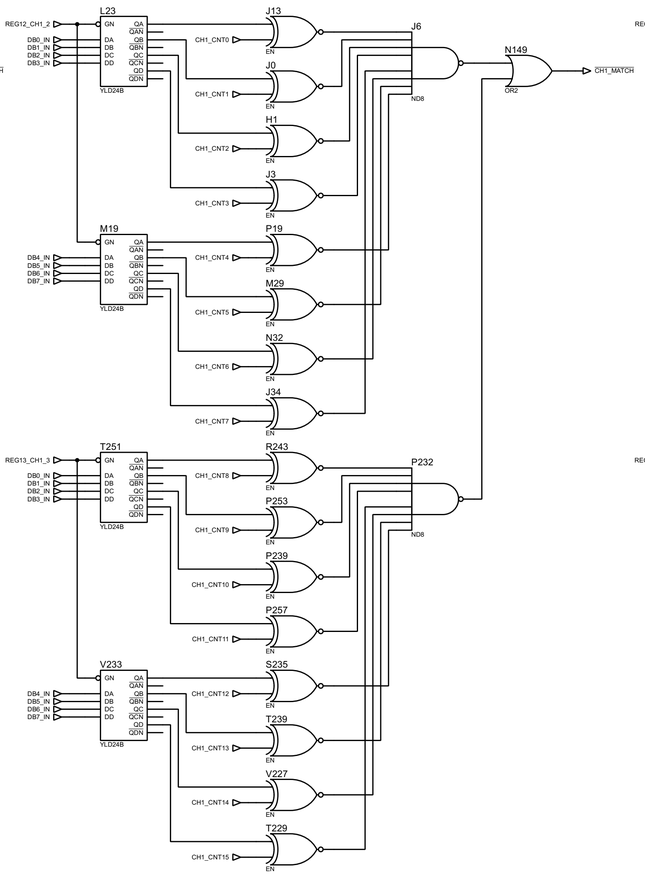


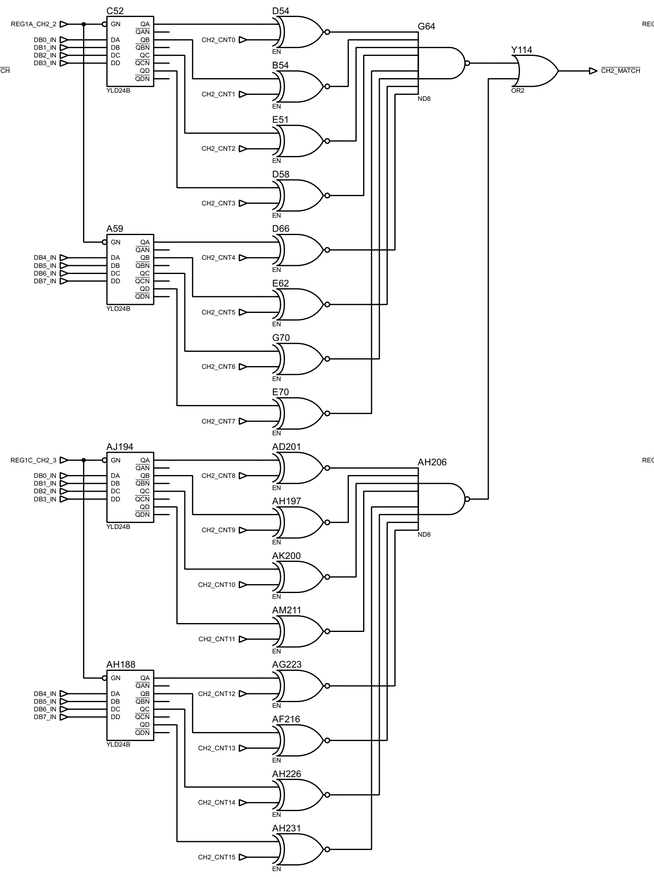


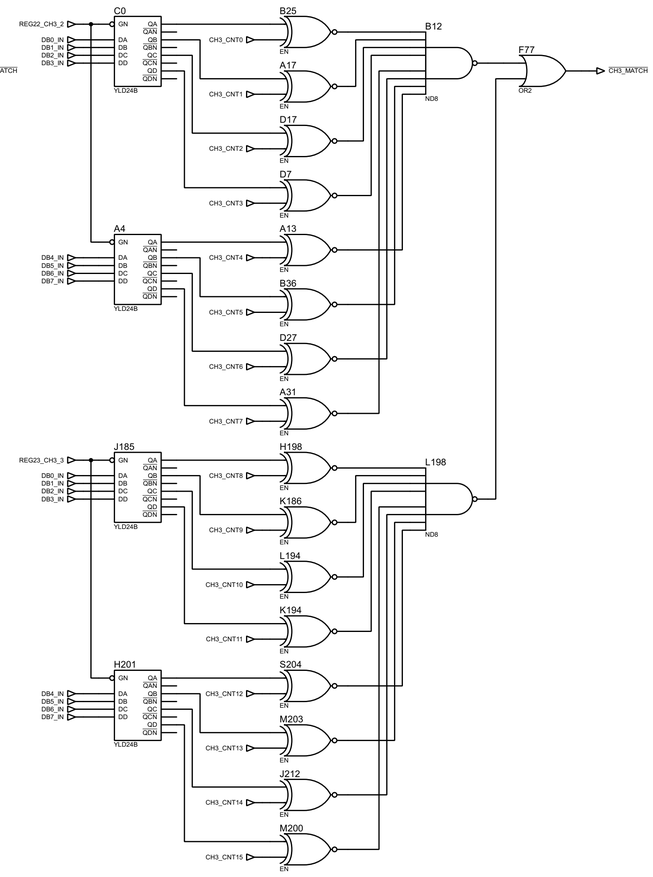


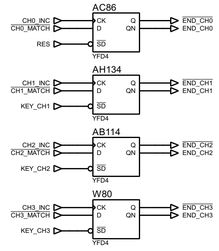
TITLE: Konami 053260 ADDR COUNTER MUX	DATE: 9/19/2025
BY: Sean Gonsalves REV: A	PAGE: 18/34





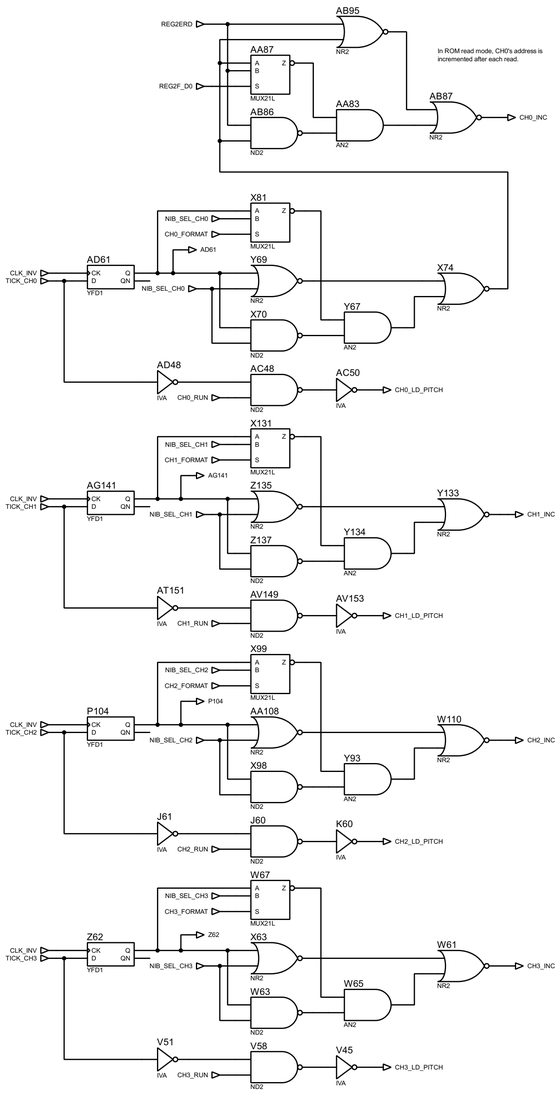




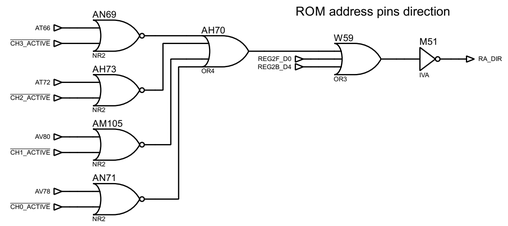


TITLE: Konami 053260 END CHECKS	DATE: 9/19/2025
BY: Sean Gonsalves REV: A	PAGE: 19/34

CH0 has additional logic used
for ROM readout by CPU, ticked
by reading REG 2E
See AE195



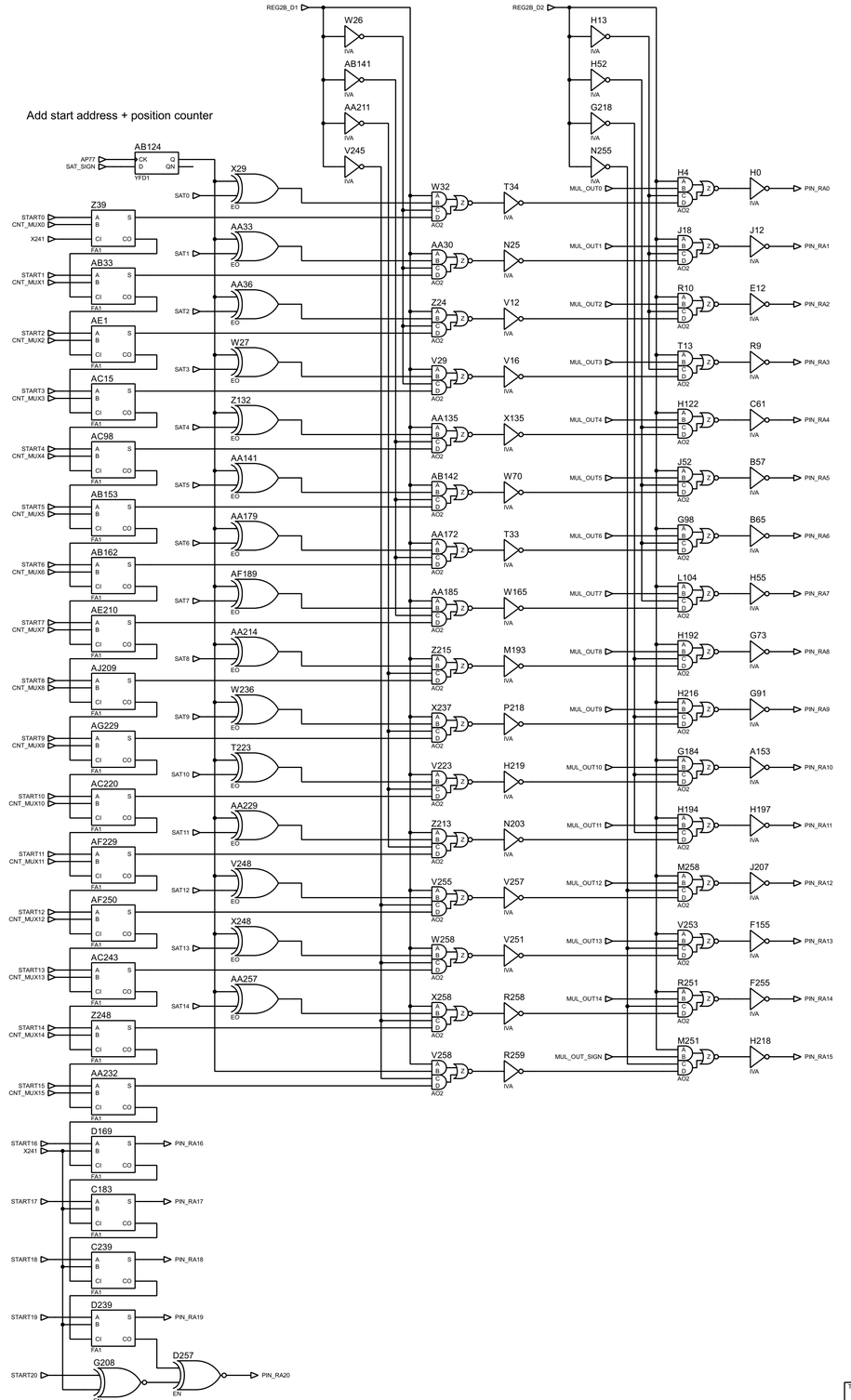
ROM address pins direction



Test mode: Select between
normal ROM address and
final mixed sample value

Test mode: Select between
normal ROM address and
multiplier output

Add start address + position counter

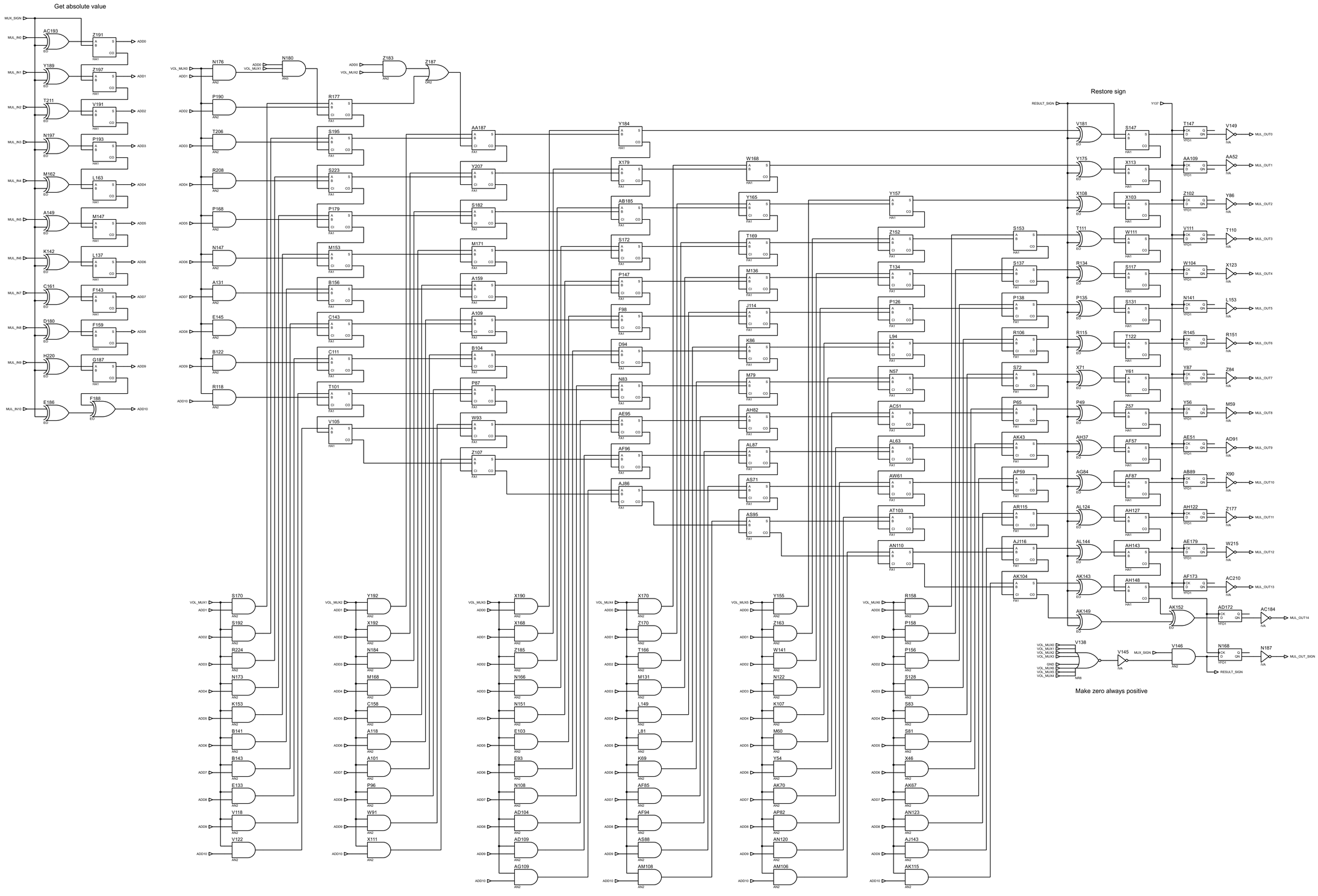


TITLE: Konami 053260 ROM ADDRESS	DATE: 9/19/2025
BY: Sean Gonsalves REV: A	PAGE: 20/34

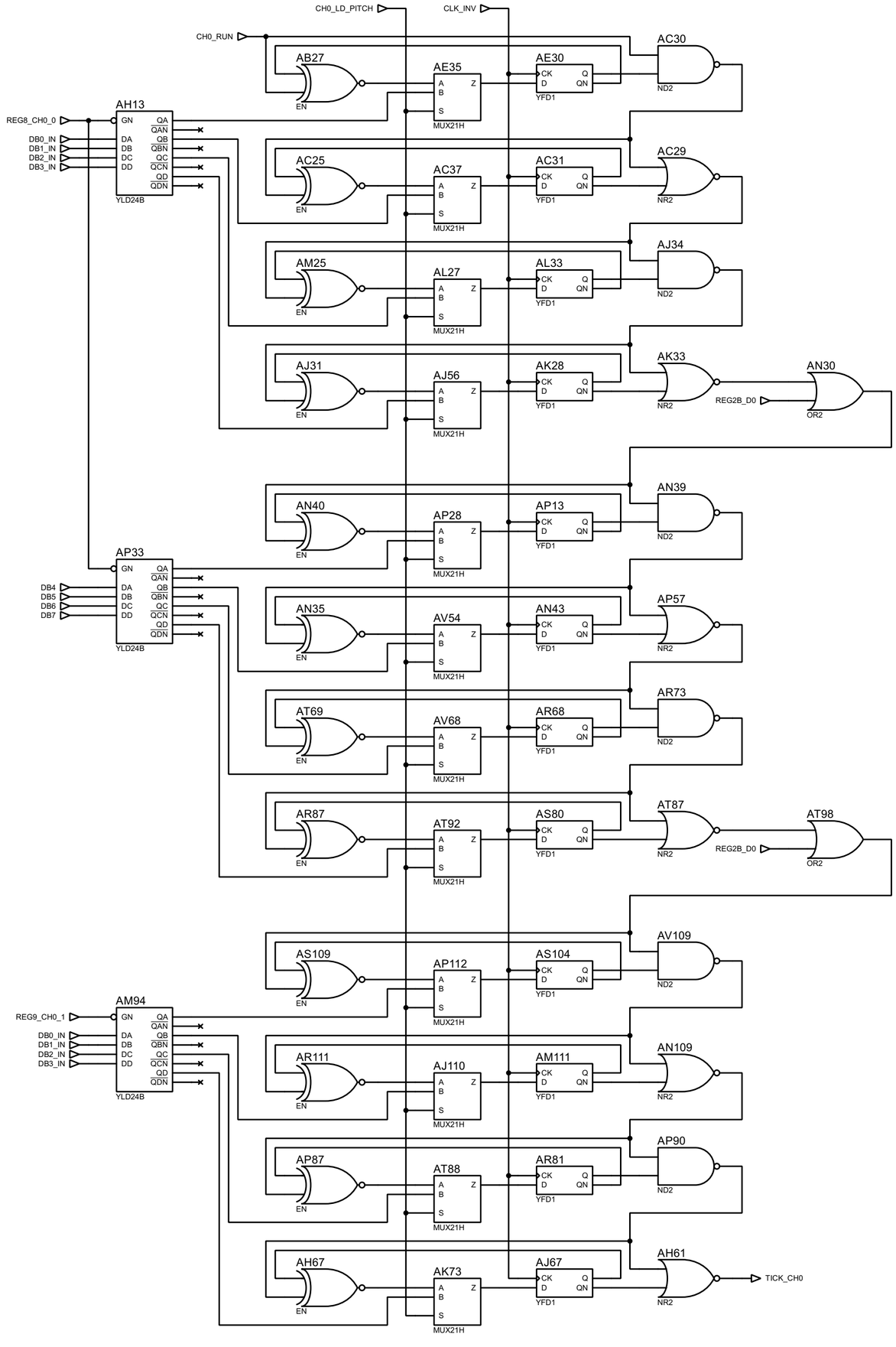
4 PCM channels L/R sample value mux to feed volume multiplier ?
Sign extend 8 to 12 bits

What are these used for ?
They allow feeding back the result of a multiplication back into the multiplier.
Only connected to 12 bits instead of 16.
Is it panning related ?

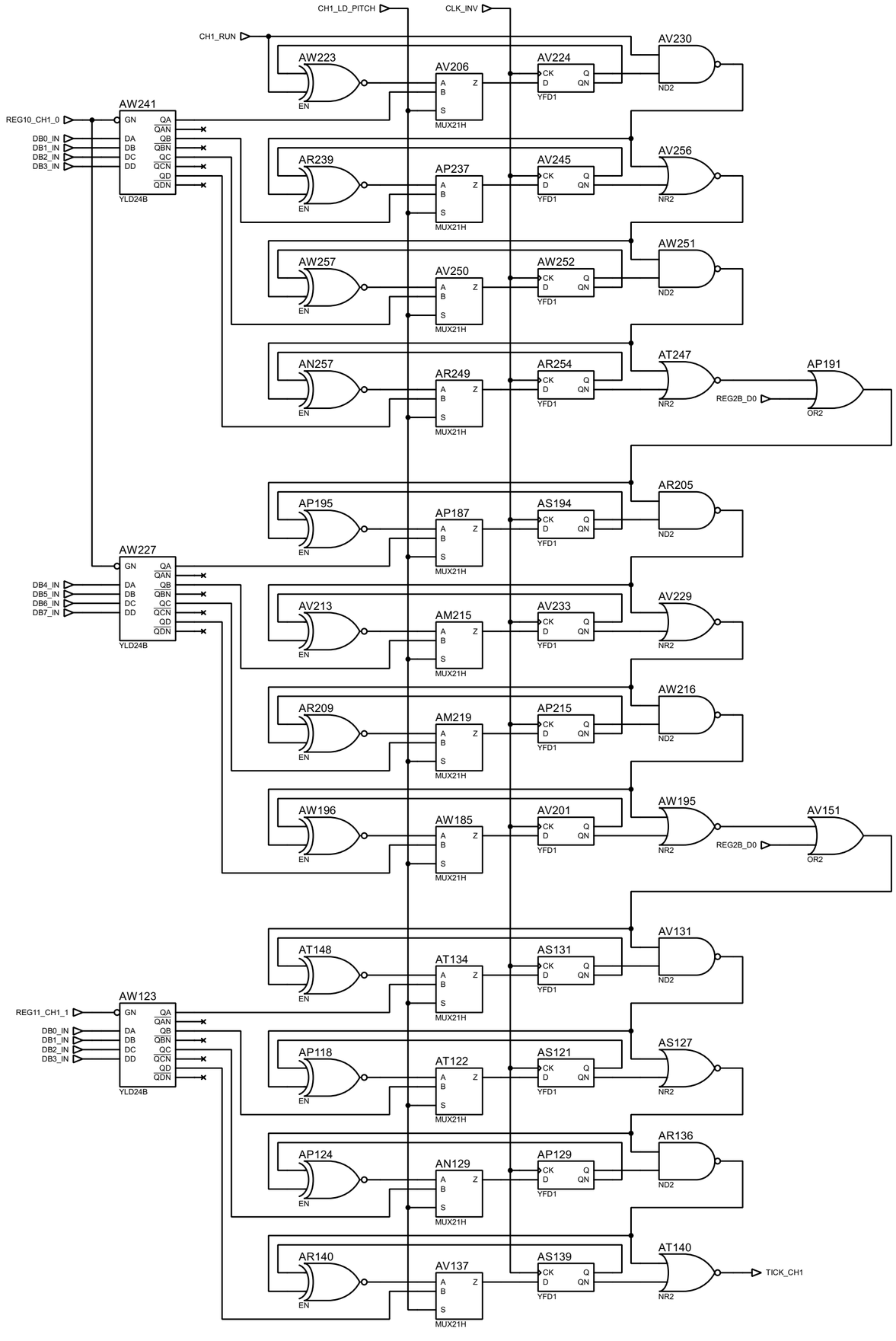
TITLE: Konami 053260 PRE VOL MUX	DATE: 9/19/2025
BY: Sean Gonsalves REV: A	PAGE: 21/34



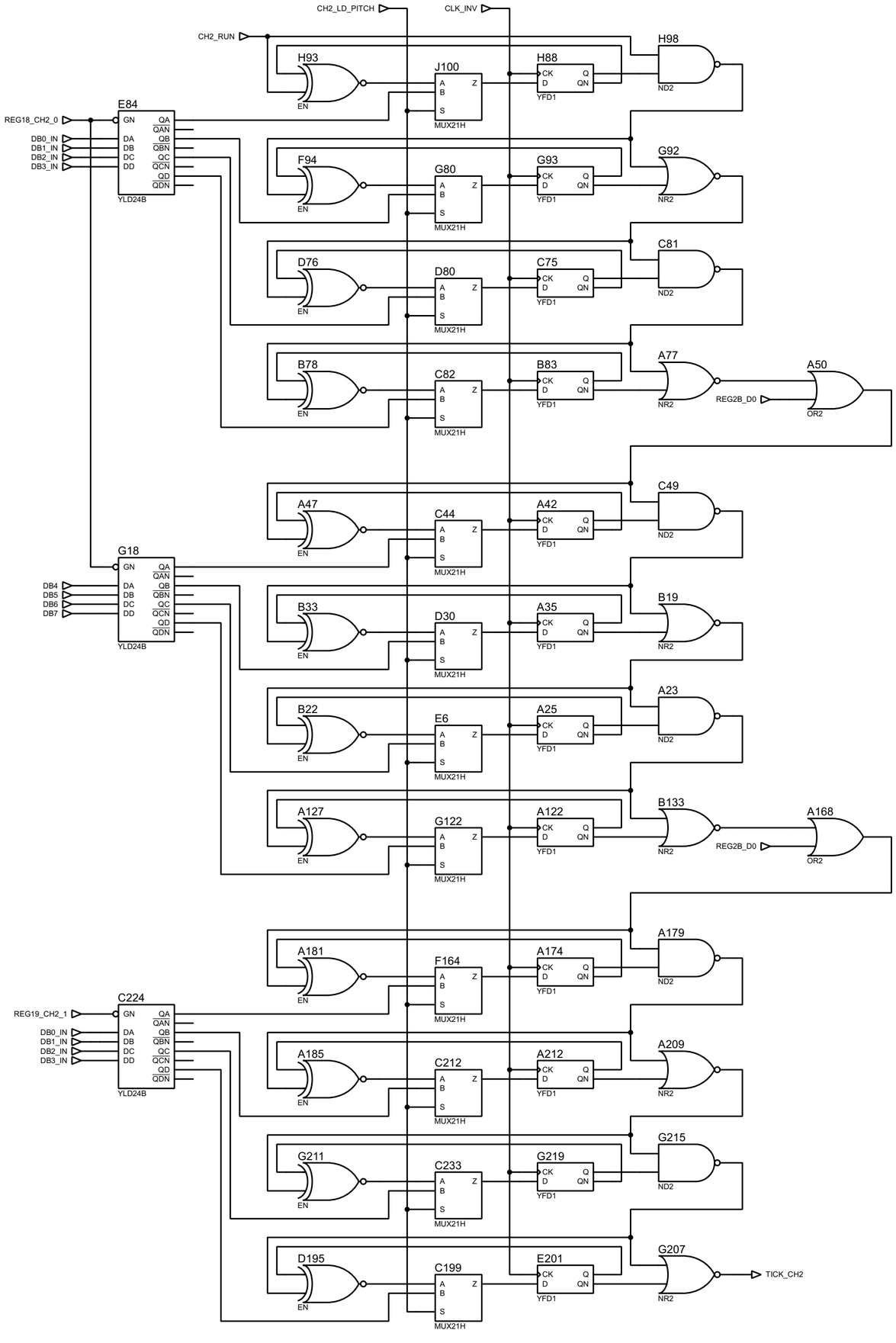
TITLE: Konami 053260 MULTIPLIER	DATE: 9/19/2025
BY: Sean Gonsalves REV: A	PAGE: 22/34



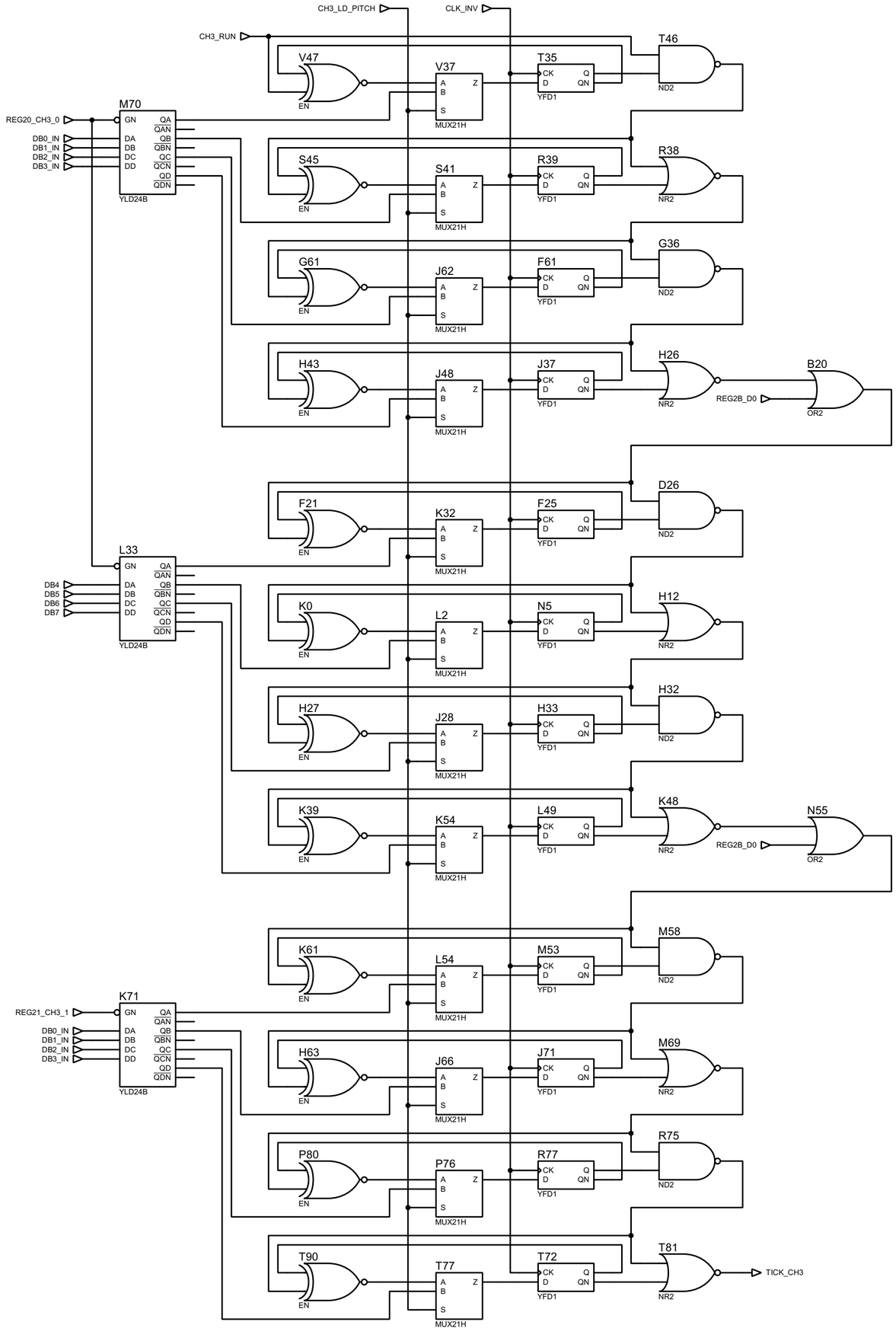
TITLE:	DATE:
Konami 053260 CH0 PITCH	9/19/2025
BY: Sean Gonsalves REV: A	PAGE: 23/34



TITLE: Konami 053260 CH1 PITCH	DATE: 9/19/2025
BY: Sean Gonsalves REV: A	PAGE: 24/34

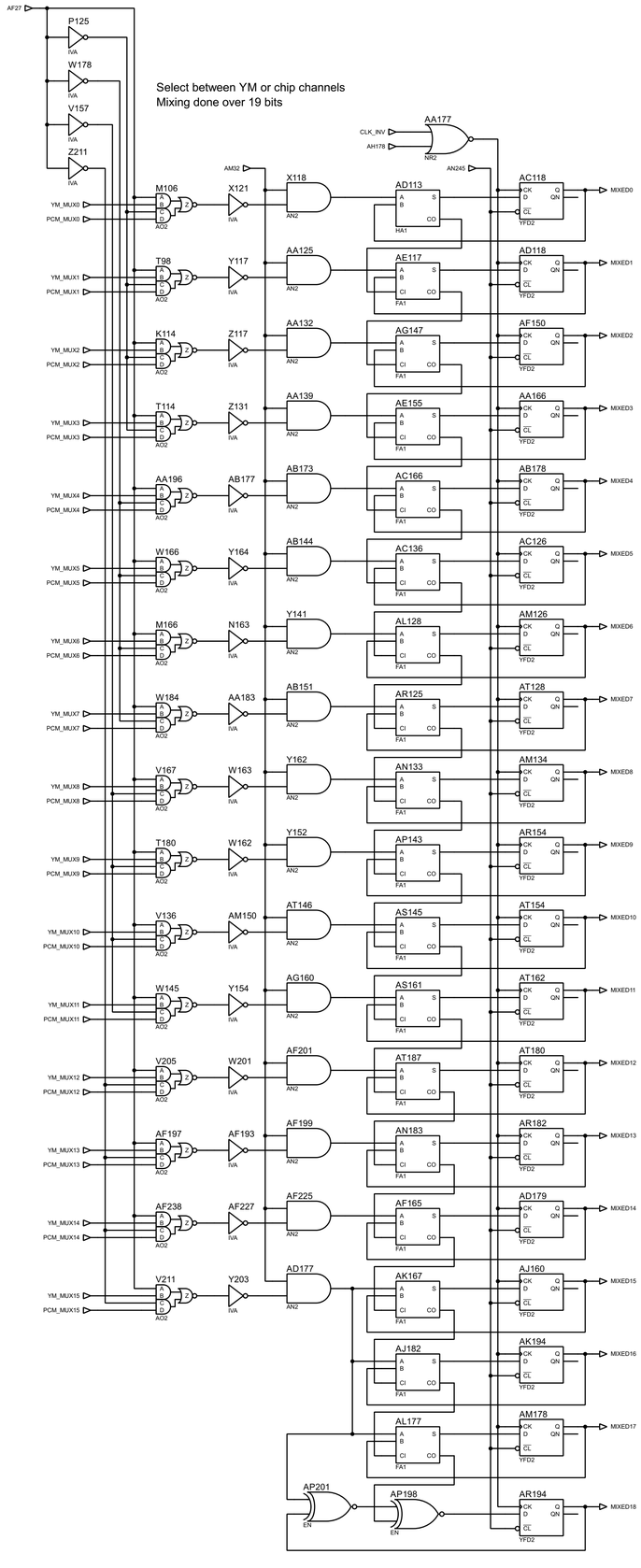


TITLE:	DATE:
Konami 053260 CH2 PITCH	9/19/2025
BY: Sean Gonsalves REV: A	PAGE: 25/34

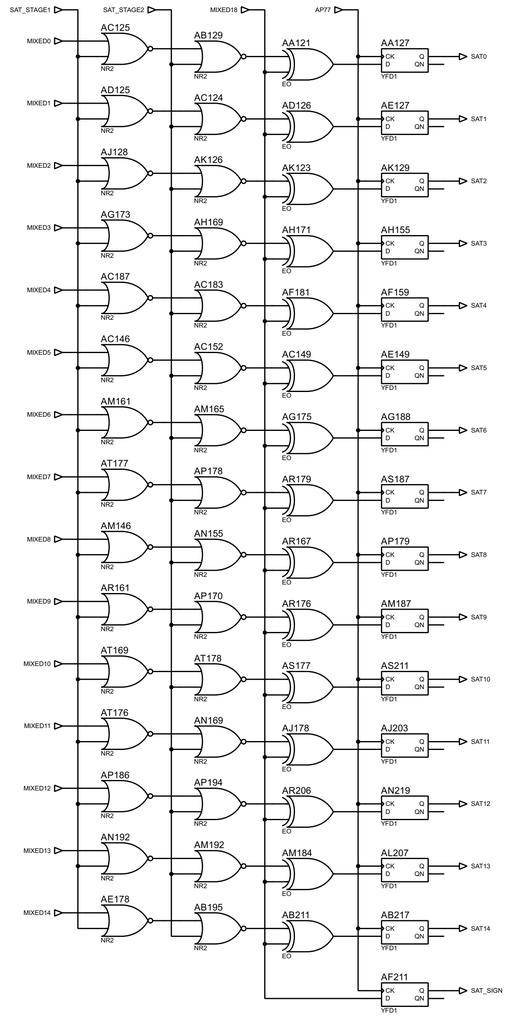


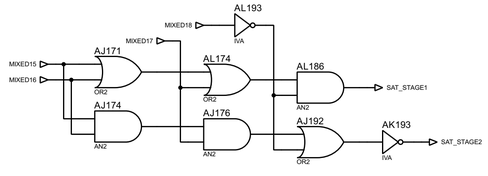
TITLE: Konami 053260 CH3 PITCH	DATE: 9/19/2025
BY: Sean Gonsalves REV: A	PAGE: 26/34

Select between YM or chip channels
Mixing done over 19 bits



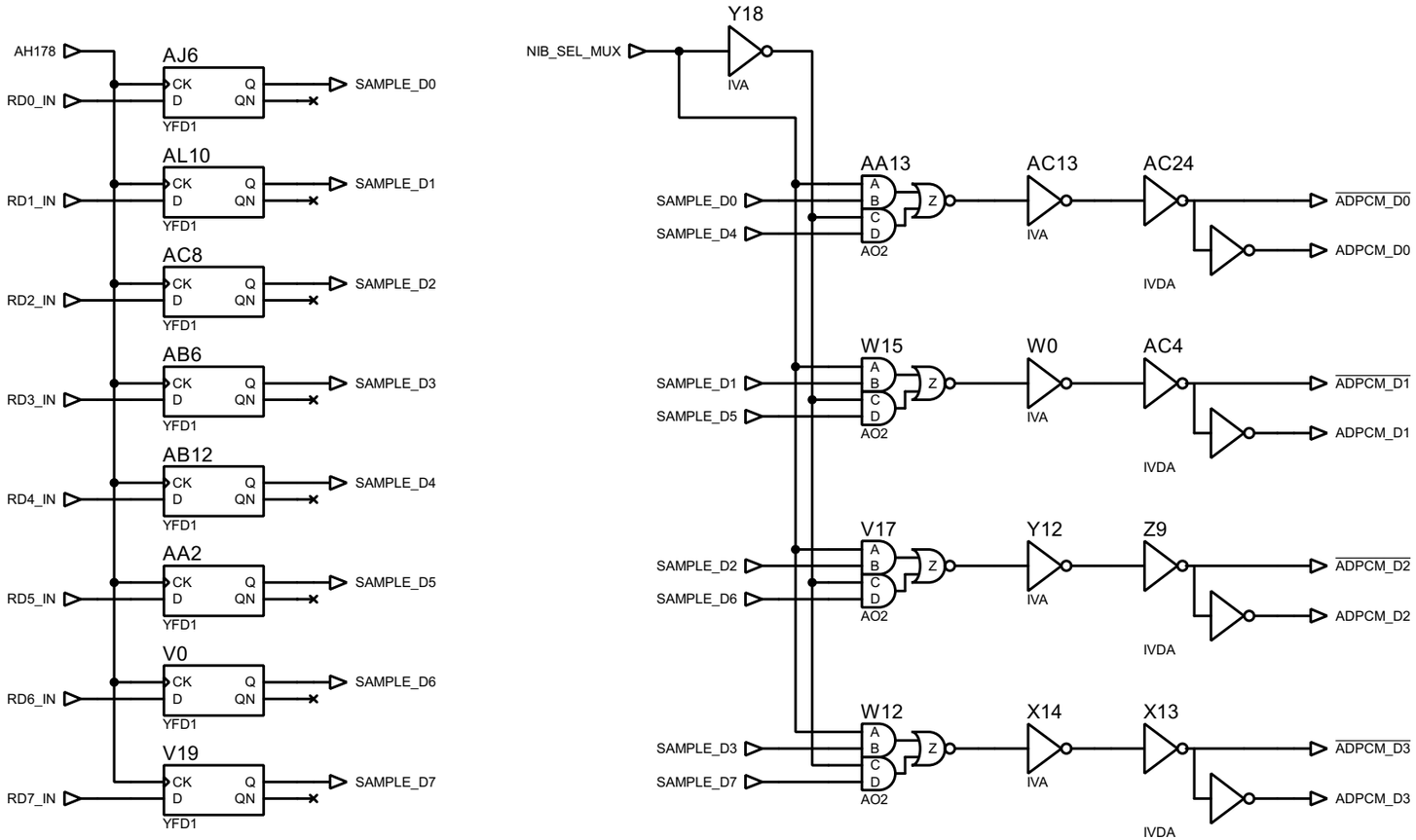
Saturation
Unsigned to signed



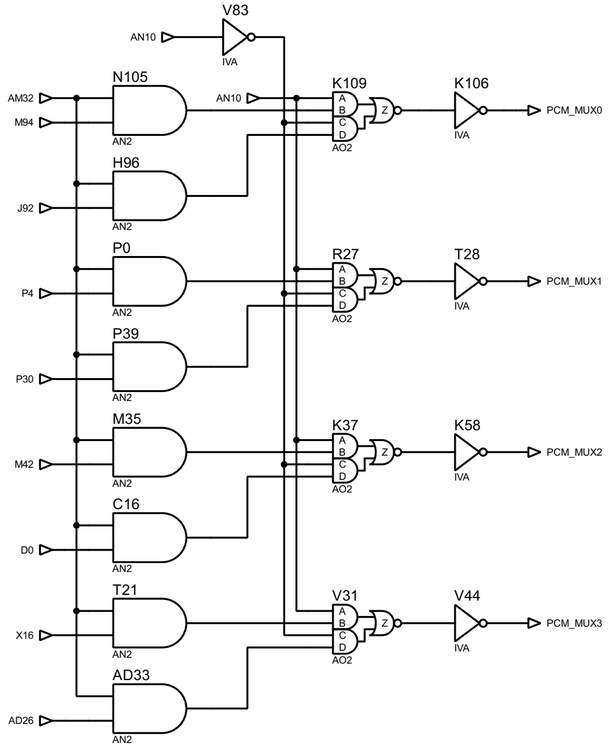


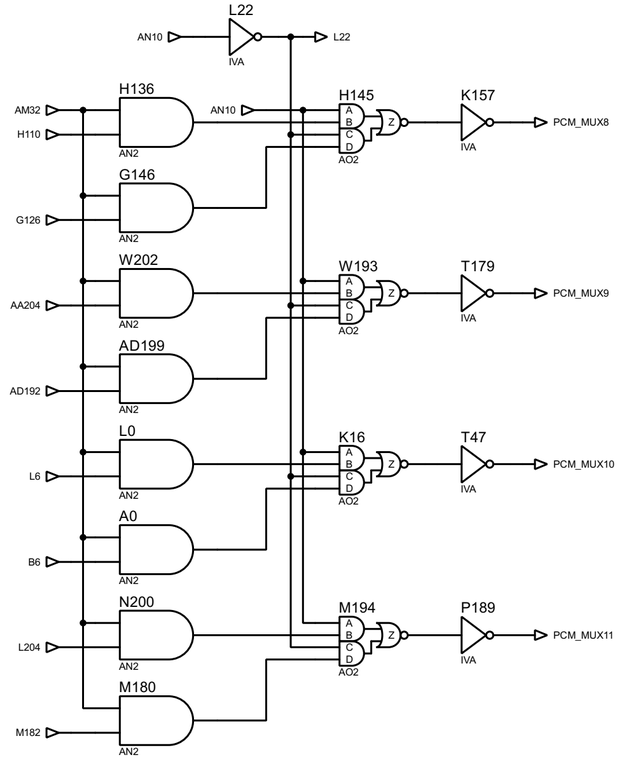

```
Saturation
s       FEDCBA98 76543210
0 11111111 11111111 = 7FFFF =  262143 @ 1
1 11111111 11111111 = 3FFFF =  262144 @ 0

First stage:
18 17 16 15 AL186
x  0  0  0  0
1  x  x  x  0

Second stage:
18 17 16 15 AK193
x  1  1  1  0
0  x  x  x  0

00: through
01: 0000
10: 1111
11: 0000

0000 0 0 through (between 0 and 32767)
0001 1 0 max
0010 1 0 max
0011 1 0 max
0100 1 0 max
0101 1 0 max
0110 1 0 max
0111 1 0 max
1000 0 1 min
1001 0 1 min
1010 0 1 min
1011 0 1 min
1100 0 1 min
1101 0 1 min
1110 0 1 min
1111 0 0 through (between -1 and -32768)
```

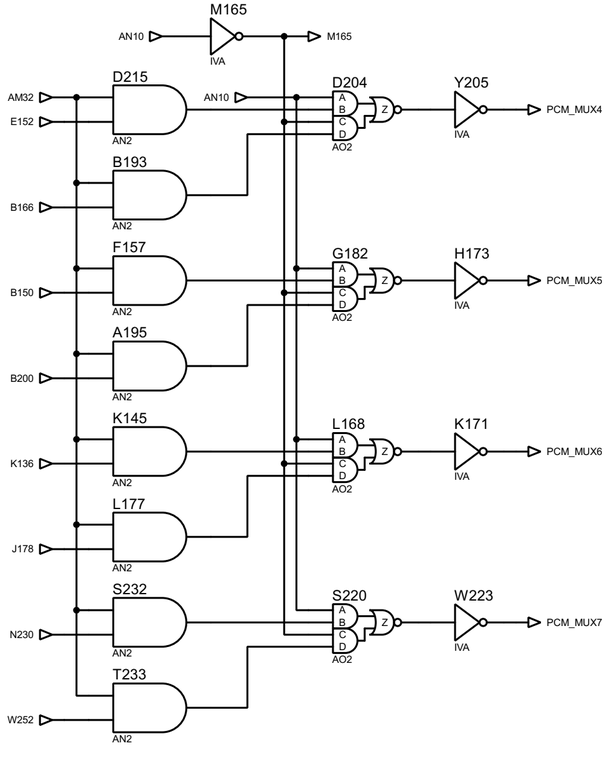
TITLE: Konami 053260 ACCUMULATOR		DATE: 9/19/2025
BY: Sean Gonsalves	REV: A	PAGE: 27/34

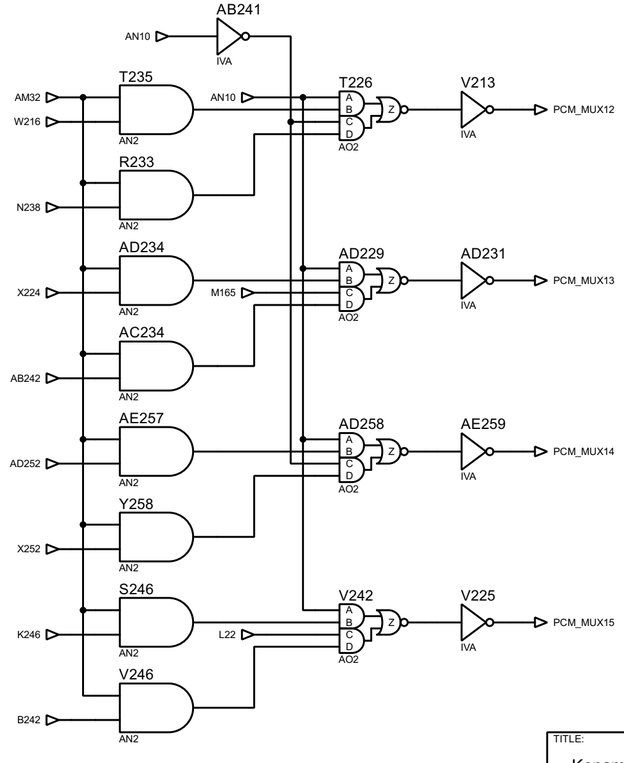


TITLE:	DATE:
Konami 053260 ROM READ	9/19/2025
BY: Sean Gonsalves REV: A	PAGE: 28/34



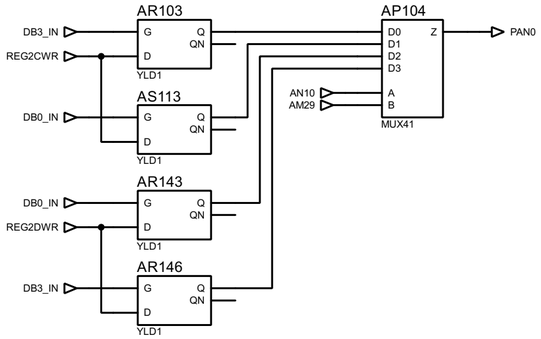


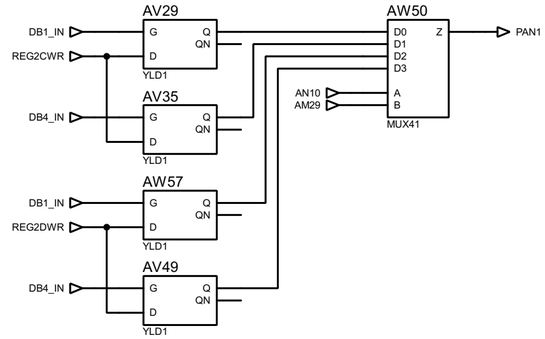


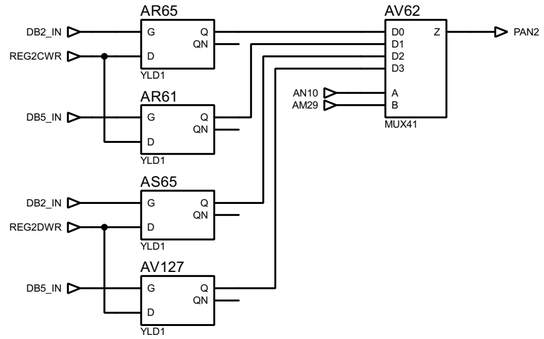


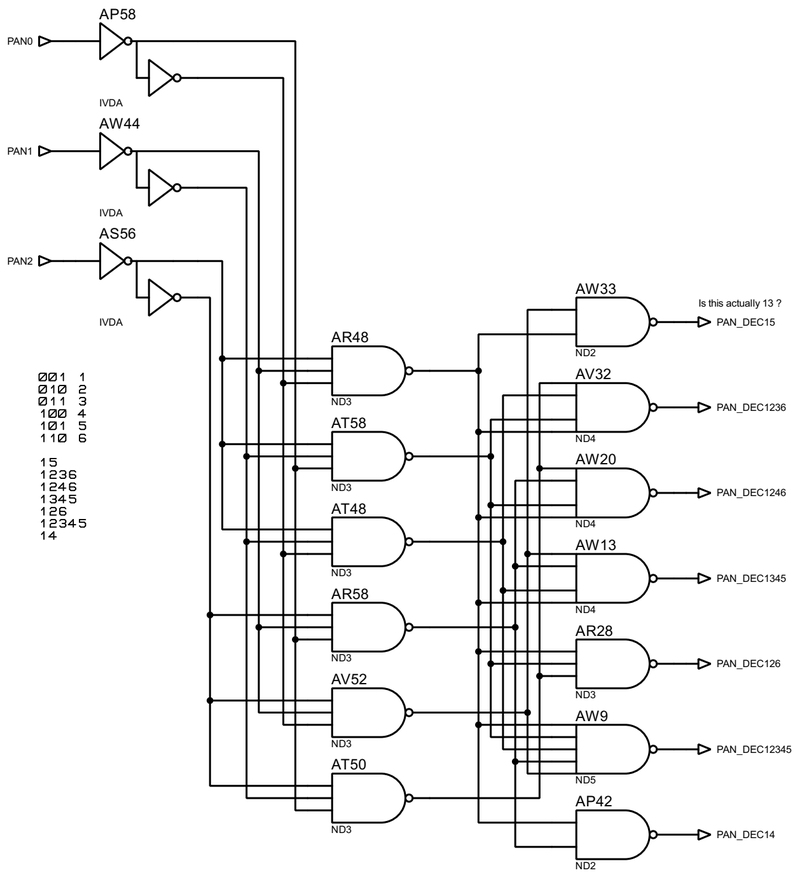
TITLE:	DATE:
Konami 053260 PCM L/R MUX	9/19/2025
BY: Sean Gonsalves REV: A	PAGE: 29/34

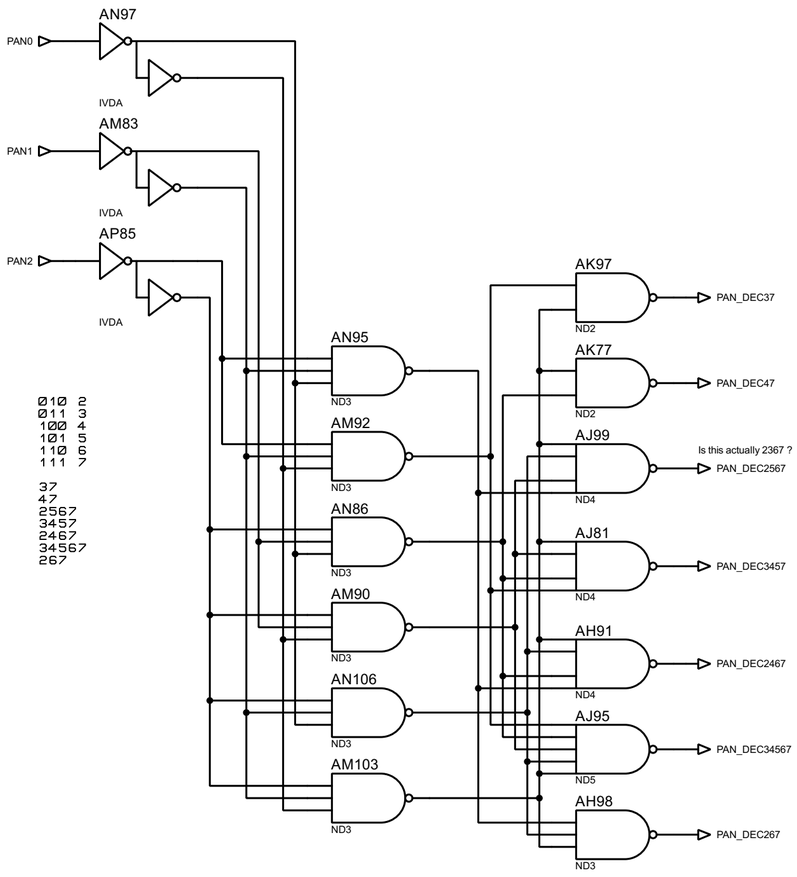
Shouldn't these two be swapped ?





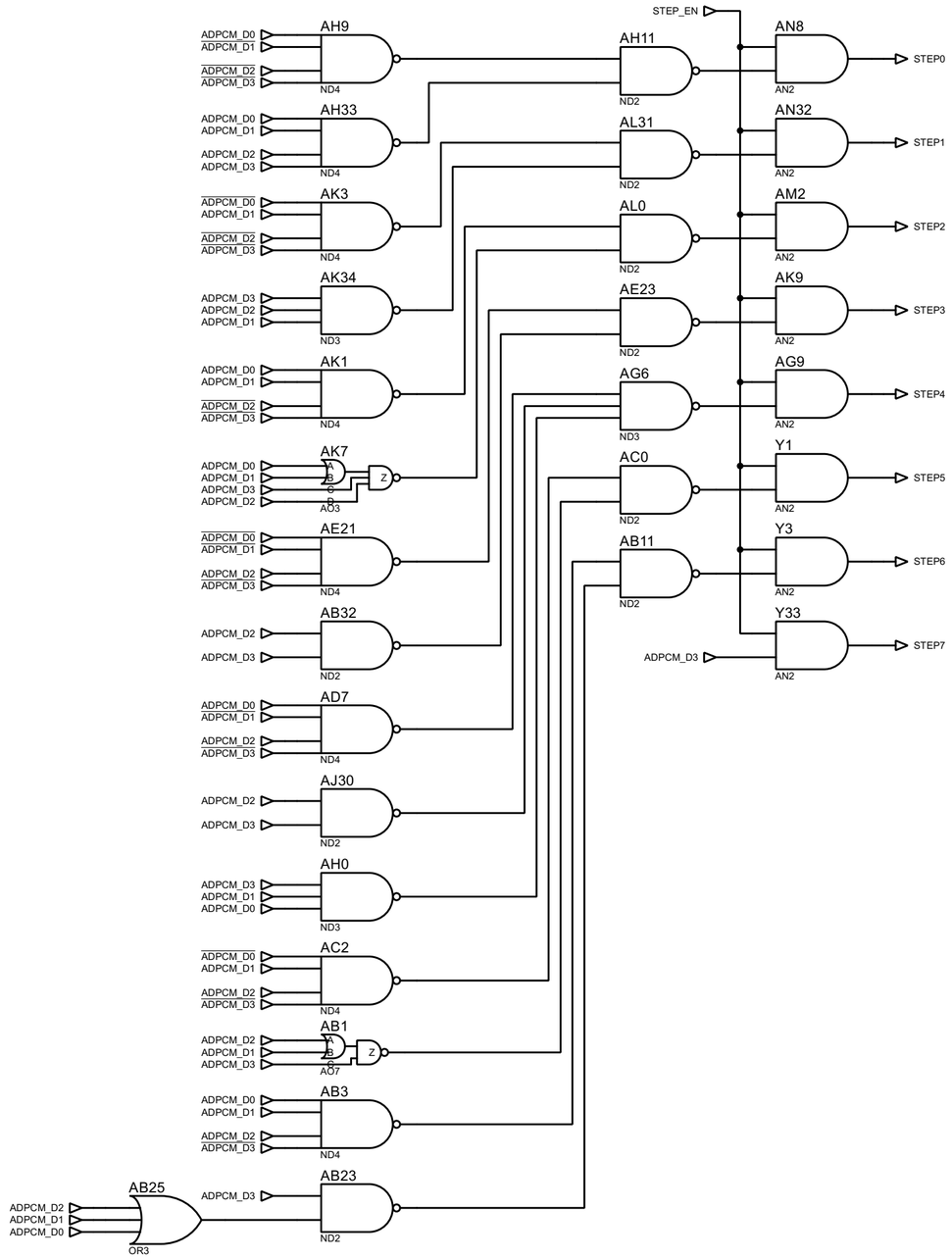






This stuff decodes the 8 possible pan values to a 16 signals used to modify the channel's volume setting

TITLE: Konami 053260 PAN LUT	DATE: 9/19/2025
BY: Sean Gonsalves REV: A	PAGE: 30/34

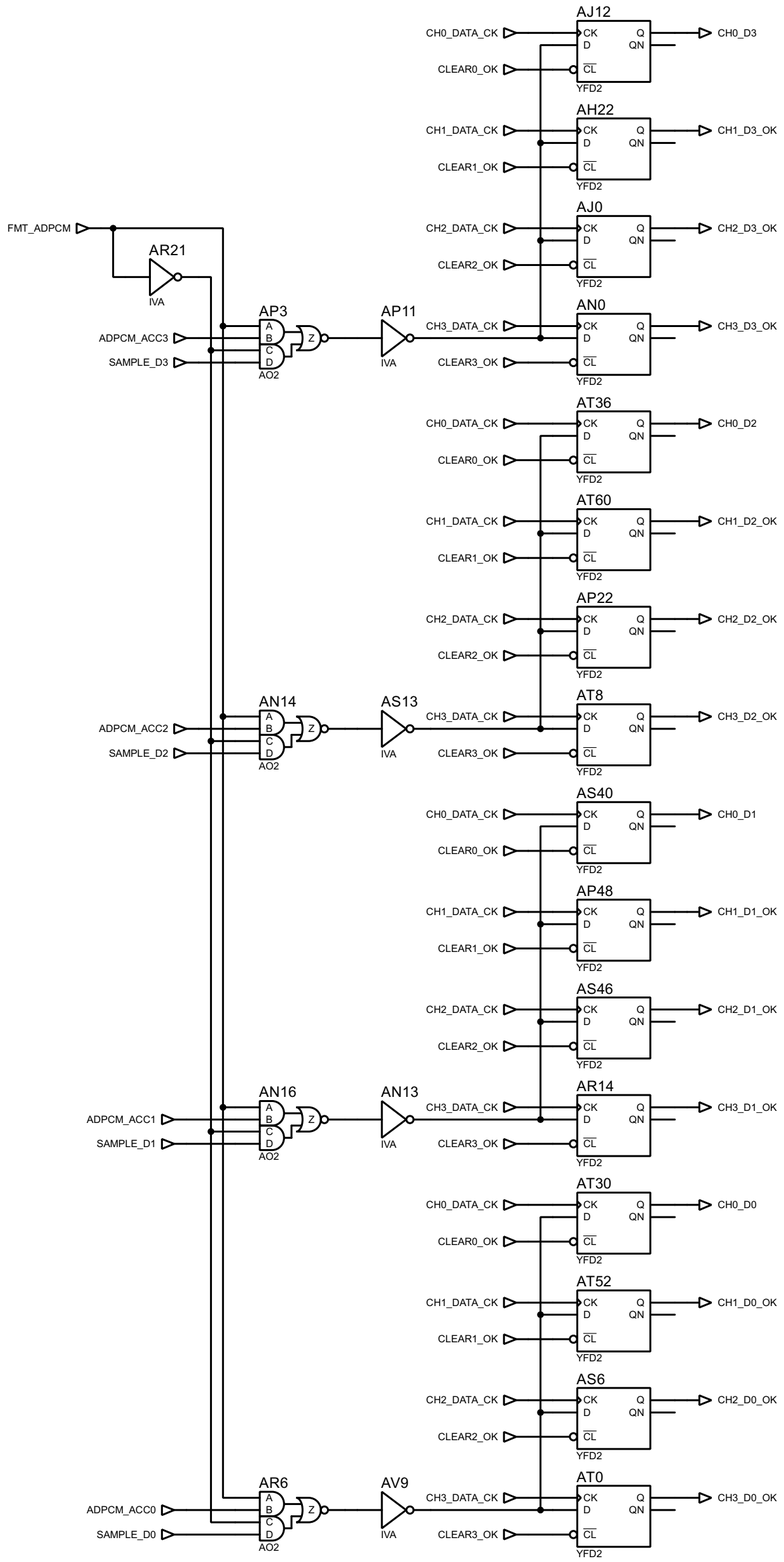


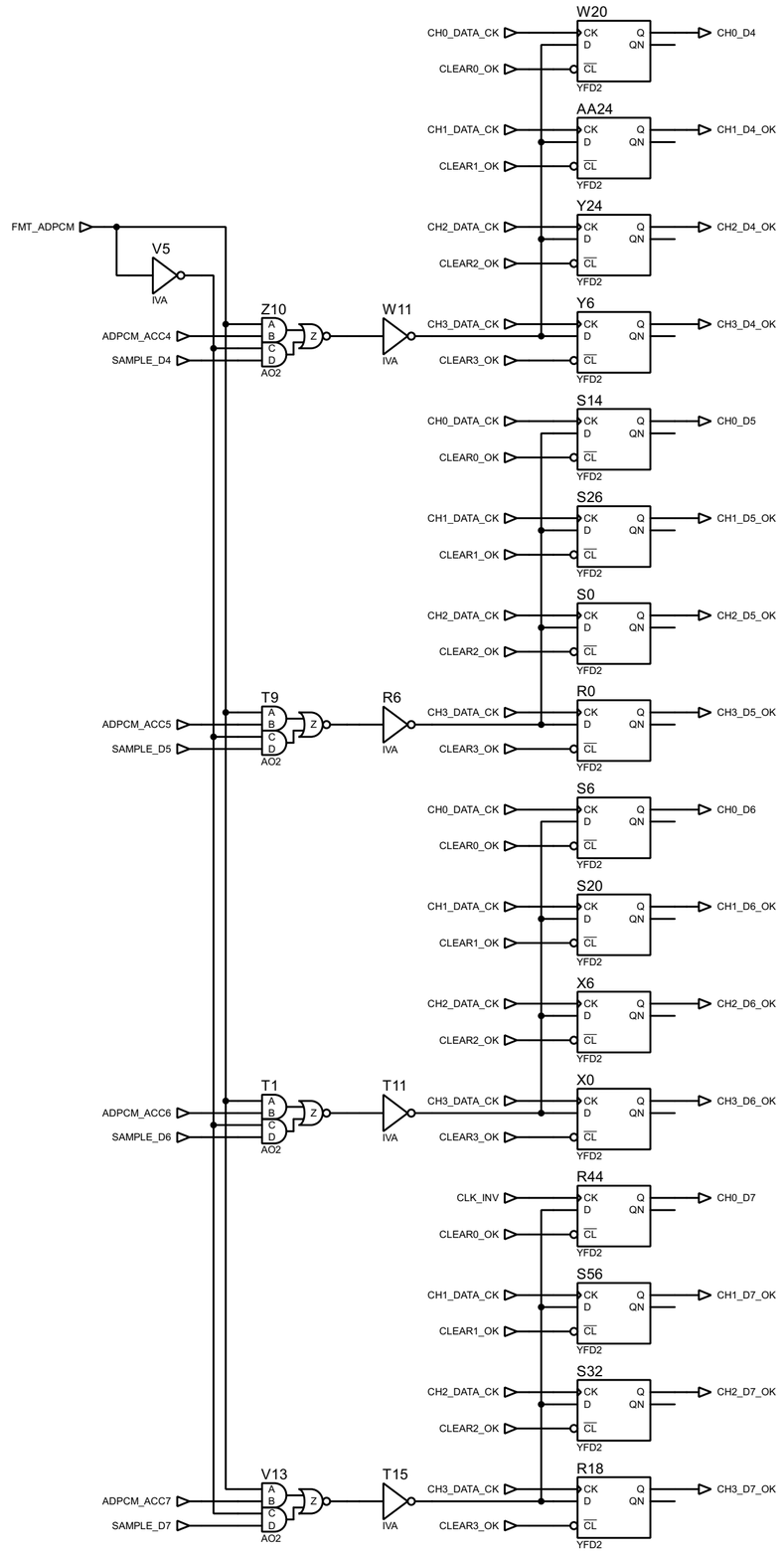
This translates the 4-bit ADPCM sample
to a signed value that must be added
to the channel's accumulator.
Should match MAME's kadpcm_table[].

IN:OUT
0:0
1:1
2:2
3:4
4:8
5:16
6:32
7:64
8:-128
9:-64
A:-32
B:-16
C:-8
D:-4
E:-2
F:-1

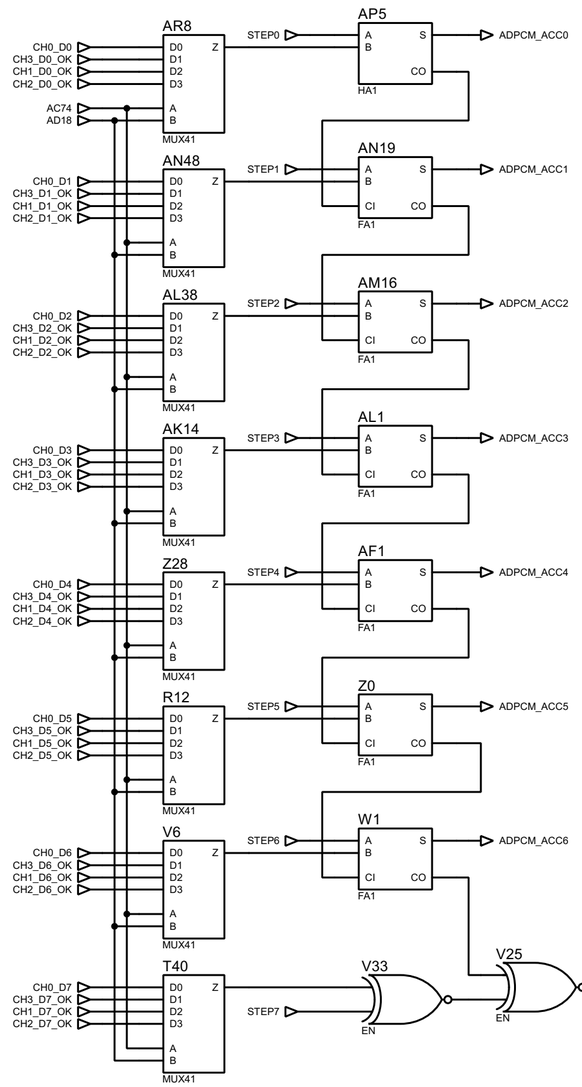
TITLE:	DATE:
Konami 053260 ADPCM STEP GEN	9/19/2025
BY: Sean Gonsalves REV: A	PAGE: 31/34

4 CH x 8-bit regs for sample values
Either load from ROM, or acc ADPCM

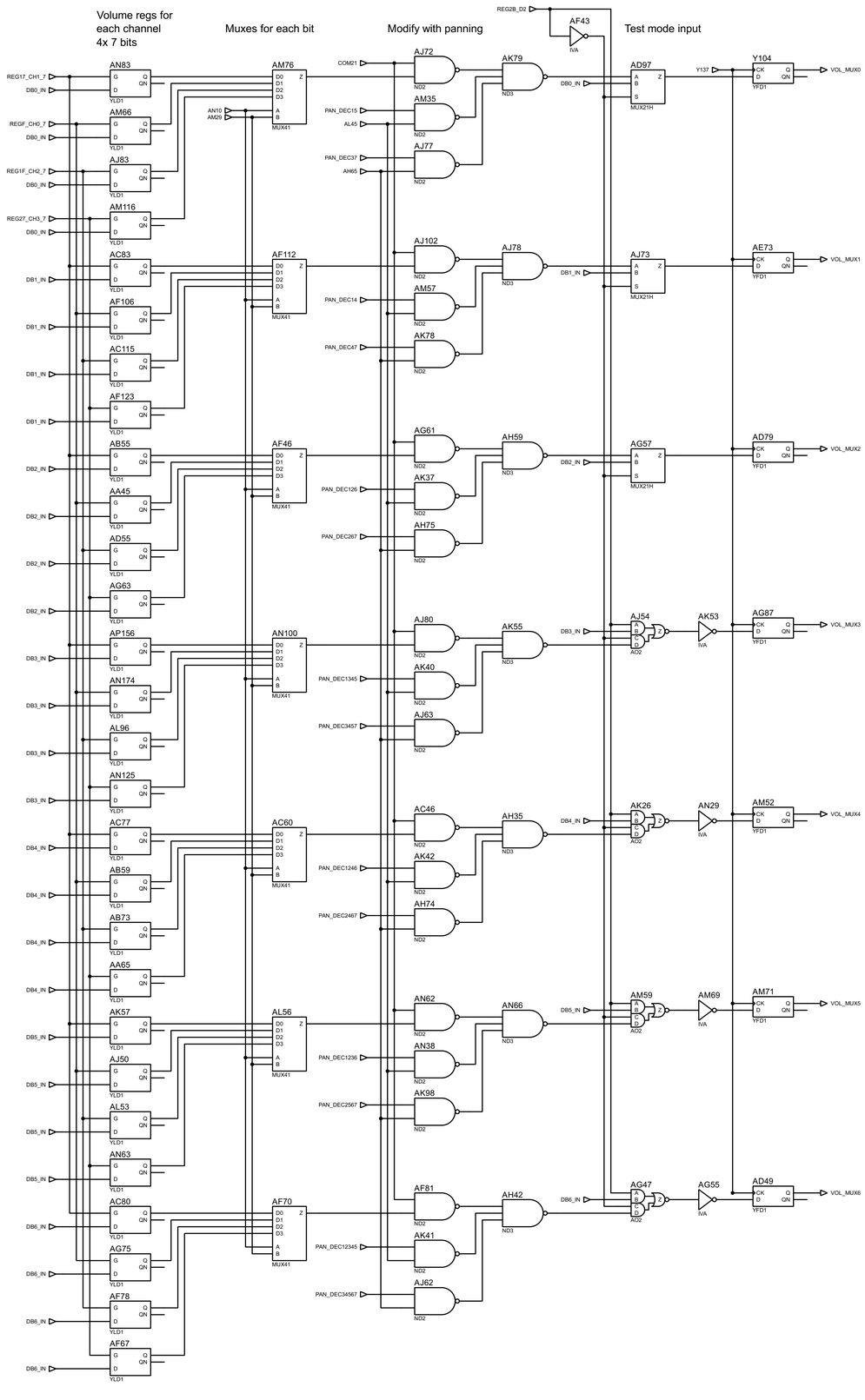




ADPCM acc

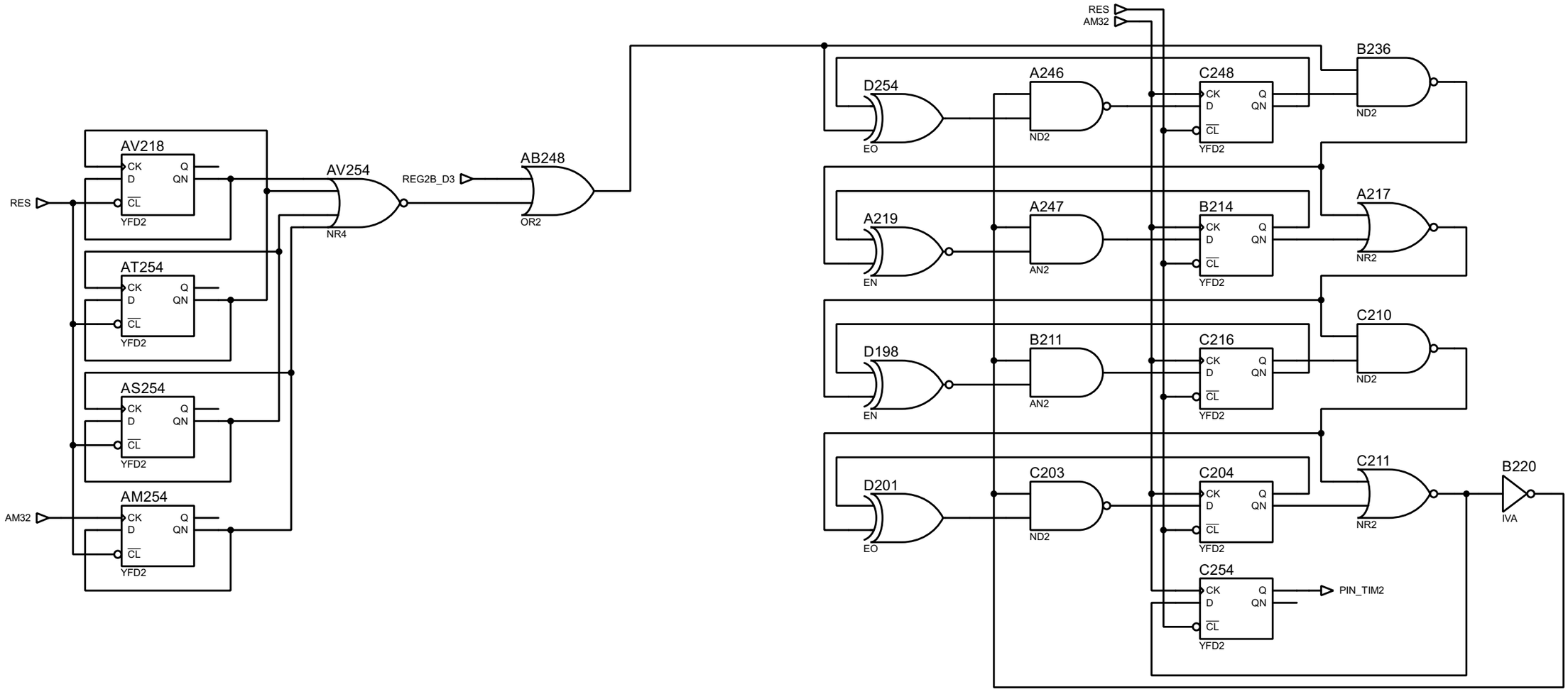


TITLE: Konami 053260 SAMPLE REGs	DATE: 9/19/2025
BY: Sean Gonsalves REV: A	PAGE: 32/34



TITLE:	DATE:
Konami 053260 VOLUME	9/19/2025
BY: Sean Gonsalves REV: A	PAGE: 33/34

Further clock division for TIM2 output



TITLE:	DATE:
Konami 053260 TIMER OUTPUT	9/19/2025
BY: Sean Gonsalves REV: A	PAGE: 34/34