University of Verona
Department of Computer Science
Laurea Magistrale Degree in Computer Science and Engineering

Automatic generation of self-adaptive TLM protocols from PSL assertions

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Abstract

Acknowledgements

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Thesis Contribution

In this thesis, we have developed a methodology

Outline

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qui ci va la spiegaxione del tuo lavoro

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qui invece ci puoi mettere a livello implementativo il tuo lavoro

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This thesis proposes a methodology

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Acronyms

CTL	Computation Tree Logic
EFSM	Extended Finite State Machine
LTL	Linear Temporal Logic
PSL	Property Specification Language
DUV	design under verification
RTL	register transfer level
TLM	Transaction Level Modelling
AT	Approximately Timed
LT	Loosely Timed
UT	Untimed TLM
CA	Cycle Accurate
M^I_{TLM}	TLM Initiator Model
M^T_{TLM}	TLM Target Model
M^T_{RTL}	RTL Target Model