Air Defense System



Introductions



Sam Cooper



Harrison Doll



Jake Neau



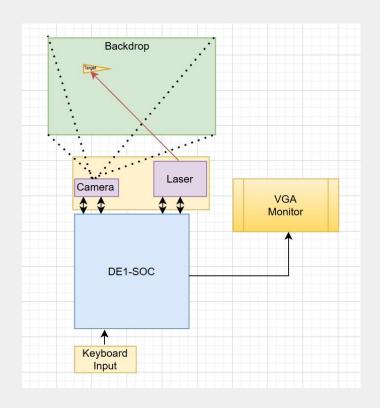
Cullen Krasselt



Nathan Woolf

Project Overview

- Develop a system to detect objects in flight
- Main Design Components
 - Backdrop / Setting
 - Fixed / Not Fixed
 - VGA Camera Module
 - Movable Laser tracker
 - DE1-SOC Development board
 - Image Processing
 - Neural Network
 - Matrix Estimation
 - VGA monitor output
 - Display Camera + More
 - Interactive Keyboard configuration
 - Avoid reprogramming
 - Allow arming / disarming
 - Allow different modes



Motivations

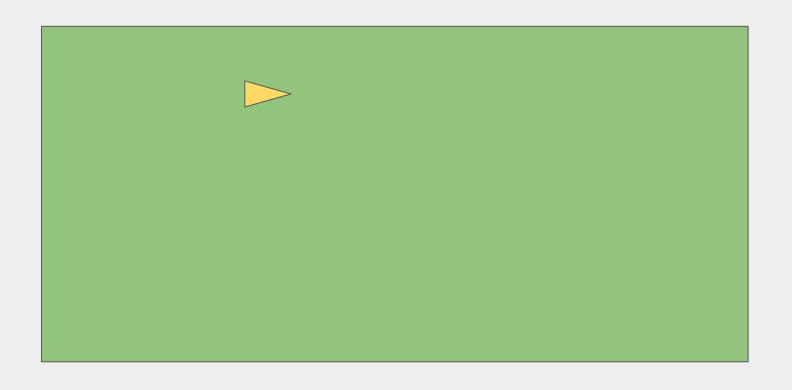
- This project is a small simulation for a defensive application for an ASIC
- In certain defense applications, processing calculations need to be performed as fast as possible
 - A CPU may be too slow such that the system is less effective
 - A CPU and the surrounding cooling may add too much bulk to systems
- Designing an ASIC to handle time sensitive tasks is crucial
 - The cost and volume that these systems are sold at can justify the setup cost for an ASIC



Approach

- Interface with multiple different types of modules for input / output
 - laser output
 - motor control
 - image processing from camera
- Tracking needs to happen on a continual basis, potentially requiring accelerators for fast decisions
 - A neural network accelerator can be used for object detection and tracking
- A unit to efficiently get to the desired rotation angle is needed

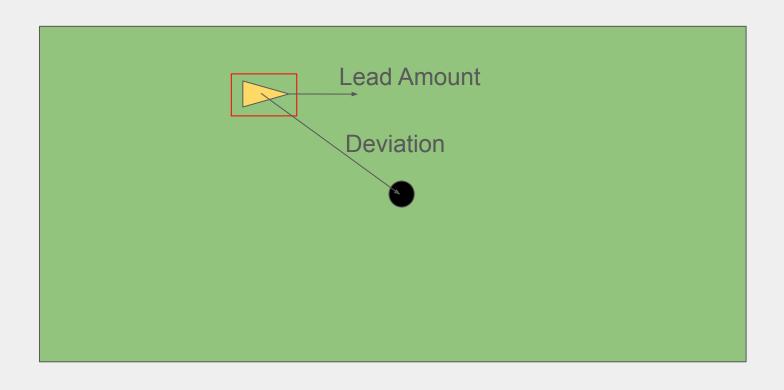
Approach: Camera Capture



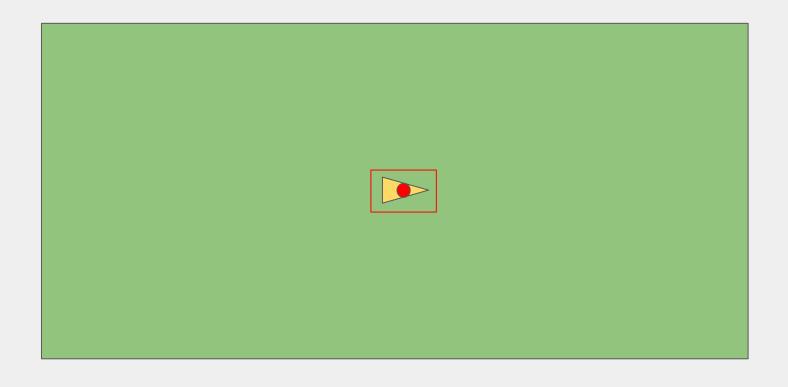
Approach: Bounding Box



Approach: Targeting



Approach: Firing



Anticipated Challenges

Aiming Mount

- Physical / Mechanical Design
 - Type of Motor
 - Board Mounting
 - Trigger
- Motor Control
 - Precision Control
 - Speed

Identification

- Airplane Profiling / False Positives
 - Contrasting Airplane / Background
 - Neural Network
- Airplane Positioning
 - IR Sensors
 - Ultrasonic Sensors
 - Multiple Cameras

FPGA Resources

- Memory Constraints
 - Image Processing
 - Neural Network Weights
- Speed Requirements

Debugging / Testing

- Difficult High Level Simulation
- Controlled Testing Environment

Risk Management

Aiming Mount

- Consult TeamLab / Makerspace personnel
- Design mount to have interchangeable motors
- Optimize motor control modules
 - Predictive Tracking

Identification

- Have our own backdrop
- Simplify neural network to meet constraints
- Use depth estimation from single camera

FPGA Resources

- Downscale / compress images
- Use smaller weights for neural network

Debugging / Testing

- Use SignalTap for high level debugging
- Setup controlled environment with backdrop in similar conditions

Milestones and Evaluation

WBS	TASK TITLE	TASK DESCRIPTION	DEPENDENCIES	TASK OWNER	PCT OF TASK COMPLETE	SCHEDULED START	SCHEDULED FINISH	ACTUAL START	ACTUAL FINISH	FINISH VARIANCE	DURATION IN DAYS						W7 V	V8 W9		W11
40	Arch Review				0%	2/25/2025	3/4/2025	2/25/2025			-32652	2123	3/4	3/11 3/	10 3/23	4/1	4/0 4	13 4/22	1 4/23	3/6
	High Level Schematic	Interfaces between different project components			0%	2/25/2025	3/4/2025	2/25/2025			0					+			_	
-	Processor Design Decisions	clearly lay out what the proc will be responsible for			0%	2/27/2025	3/4/2025				0					-			-	
	Object Detection Classification	specify the requirements for object detection			0%	2/27/2025	3/4/2025				0				_	+		_	_	+
	DVI Monitor Output	understand camera requirements for object detection understand camera requirements for higher frame output			0%	2/27/2025	3/4/2025				0					-			_	
1.5	DVI Monitor Output	understand camera requirements for higher frame output			0%	2/2//2025	3/4/2023				0		-			+		_		-
1.6					0%						0				_	_				
	Micro Arch Review		All of milestone 1		0%	3/4/2025	3/11/2025	3/4/2025			-32657									
	Camera Modules	Develop additional camera modules required for project			0%	2/27/2025	3/11/2025	3/4/2023			0					+				+
	Motor Controller	Develop verilog for pan-tilt of laser/camera			0%	2/27/2025	3/11/2025				0					+		_		+
-	Motor Mount Hardware Design	Design hardware for how hardware movements will occur			0%	2/27/2025	3/13/2025				0									
	Processor I/O	Develop high level interfaces between various modules			0%	2/27/2025	3/13/2025				0					_				
2.5	Flocessor I/O				0%						0									
2.6					0%						0									
	Basic Building Blocks Imp				0%	3/11/2025	3/20/2025	3/11/2025			-32662									
	Object Detection Testing	Have camera proc modules onto FPGA, verify approx function	Camera Modules		0%	3/4/2025	3/20/2025	GITTIEGES			0									
	Processor Validation	Interface all modules together, verify functionality	Processor IO		0%	3/4/2025	3/20/2025				0									
	Motor Unit Testing	Have motor contorller verilog moving hardware	motor modules		0%	3/11/2025	3/18/2025				0									
-	Motor Mount Proof of concept		Purchased all motor components		0%	3/4/2025	3/20/2025				0									
3.5					0%						0									
3.6					0%						0									
	Complete System Imp				0%	3/20/2025	4/15/2025	3/20/2025			-32669									
		Validate transfer function from camera coordinates to physical pos	Motor modules tested		0%	3/20/2025	4/15/2025				0									
	Full Unit Testing and Validation	Sample demos and debugging			0%	3/27/2025	4/15/2025				0									
	Processor Improvements	Make processor improvements under the requirement for more spe	eed, better accuracy, etc		0%	4/8/2025	4/15/2025				0									
4.4	*				0%						0									
4.5					0%						0									
4.6					0%						0									
5.0 F	Poster Design				0%	4/15/2025	4/25/2025	4/15/2025			-32687									
5.1 8	System Videos/images	Capture documentation of fully functioning demo			0%	4/15/2025	4/25/2025				0									
	High Level Diagrams	Produce diagrams for the system			0%	4/15/2025	4/25/2025				0									
5.3	-				0%						0									
5.4					0%						0									
5.5					0%						0									
5.6					0%						0									

Google Sheets with Team's Gantt Chart

Team Responsibilities

Image Processing & Laser/Camera Implementation

Samuel Cooper & Harrison Doll

Motor Mount Design & FPGA Interface

Nathan Woolf

Motor Interfacing & Control Modules

Cullen Krasselt

Targeting Processor Configuration

Jake Neau