Faruk **Volkan Mutlu**

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Education

Northeastern University — *Boston, MA*

PhD in Computer Engineering — *Sep 2018 – Jun 2023 (Expected)*

- **GPA:** 3.94. **Courses:** Analysis and Design of Data Networks, Mobile and Wireless Networks, Graph Theory, Numerical Optimization, Computer Architecture, High Performance Computing, Machine Learning.
- **Machine Learning Project:** Implemented class partitioning heuristics for fast binary tree SVM training. Used Python with the sklearn library to test heuristics against other methods.
- **Computer Architecture Project:** Designed an ISA extension to accelerate common NDN functions like SipHash and SHA256 computations on RISC-V. Simulated extension in gem5 using RISC-V GNU toolchain.

Middle East Technical University — *Ankara, Turkey*

BSc in Electrical and Electronics Engineering, Computer Engineering Specialization — *Sep 2014 – Jun 2018*

- **GPA:** 3.45. **Specialization GPA:** 4.00.
- **Courses:** Data Structures, Computer Architecture, Operating Systems, Microprocessors, Computer Networks.

Experience

Northeastern University — *Boston, MA*

Graduate Research Assistant — *Sep 2018 – Present*

- **Transmission Delay Minimization via Joint Power Control and Caching in Wireless HetNets**
  - Developed an algorithm that outperforms existing methods by 15-50% as measured by average delay, by jointly optimizing caching and power resources.
  - Led numerical analysis efforts for the project by using MATLAB for prototyping, Julia to speed up simulations, and Python with the SimPy library to analyze distributed version of algorithm.
- **SDN-Assisted Named Data Networking (NDN) for Data Intensive Experiments (NSF CC* Award Project)**
  - Improved NDN forwarder throughput by integrating a novel joint caching / forwarding algorithm and by coding a hash table that keeps forwarder state in C++.
  - Formulated multi-tier caching optimization algorithm for DRAM and SSD hybrid caching system.
  - Built 10GbE-equipped local testbed. Assembled computers and set up networking equipment.

ASELSAN — *Ankara, Turkey*

Undergraduate Intern — *December 2017 – March 2018*

- Prototyped DRAM controller and AHB & APB peripherals for proprietary RISC-V chip on FPGA using Verilog.
- Wrote functional verification environment for proprietary RISC-V chip using SystemVerilog and UVM.

Middle East Technical University — *Ankara, Turkey*

Undergraduate Researcher — *March 2017 - March 2018*

- Enabled an energy-harvesting device model to achieve 80% of the performance of an ideal device as measured by an emergent data freshness metric (Age-of-Information), by formulating a battery-aware update policy.
- Coordinated simulations for the project using MATLAB.

Technical Skills

Programming Languages: C/C++, Python, Julia, MATLAB, Assembly (x86, ARM, RISC-V)
Other Skills: Git, Bash, Linux, Verilog and SystemVerilog

Publications

- D. Malak, **F. V. Mutlu**, J. Zhang and E. Yeh, "Transmission Delay Minimization via Joint Power Control and Caching in Wireless HetNets", to appear in WiOpt 2021.
- B. T. Bacinoglu, Y. Sun, E. Uysal–Bivikoglu and **V. Mutlu**, "Achieving the Age-Energy Tradeoff with a Finite-Battery Energy Harvesting Source," 2018 IEEE International Symposium on Information Theory (ISIT).