TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9459N, TC9459F

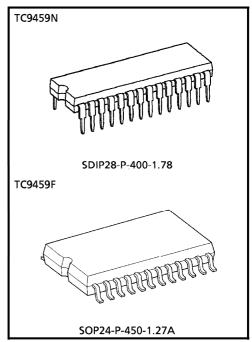
ELECTRONIC VOLUME CONTROL

The TC9459N, TC9459F are electronic volume control ICs developed for use in home stereos and other audio equipment.

Using serial data input from external sources, it controls the sound volume, balance and loudness circuits.

FEATURES

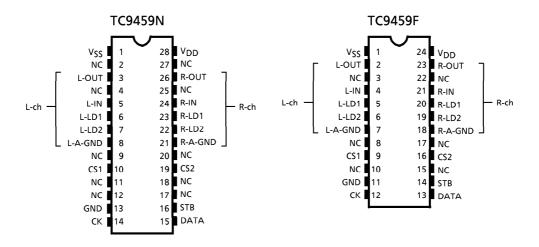
- Sound volume can be controlled in 91 steps from 0 to
 89dB or up to an infinite level in 1dB increments.
- Incorporating two channels of volume control circuits, the device allows independent volume control: therefore, it also provides the balancing function.
- A loudness circuit (20dB tap) is built in.
- Can operate with a single or dual power supplies.
- Can control up to 4 chips on the same bus by using chip select input.
- Thanks to its polysilicon resistor, the device allows you to configure a low-distortion, high-performance volume control system.



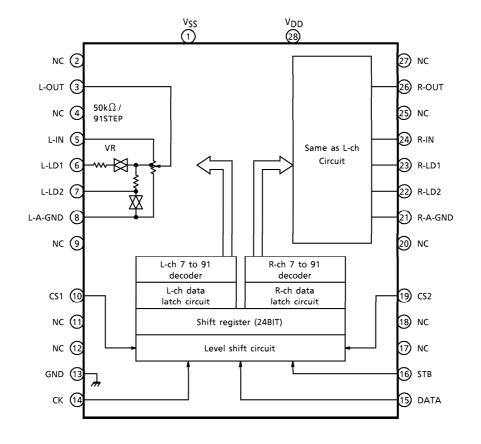
Weight

SDIP28-P-400-1.78 : 2.2g (Typ.) SOP24-P-450-1.27A : 0.44g (Typ.)

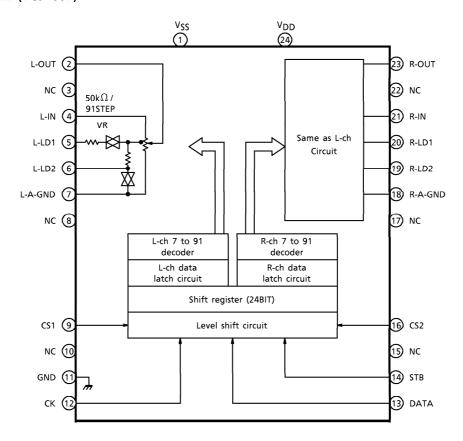
PIN CONNECTIONS



BLOCK DIAGRAM (TC9459N)



BLOCK DIAGRAM (TC9459F)



PIN DESCRIPTION

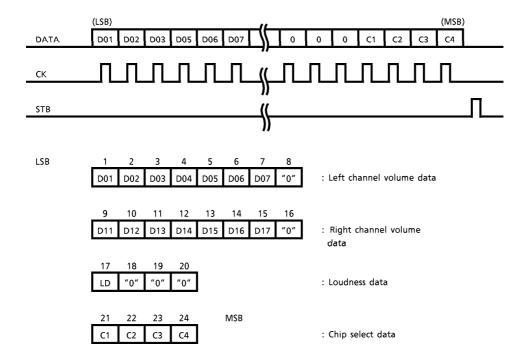
Numeral in () means the pin No. of TC9459F.

PIN No.	SYMBOL	PIN NAME	FUNCTION	REMARK
1 (1)	V _{SS}	Negative power supply pin	When using $V_{DD} = 6.0 \sim 17V$ dual power $GND = 0V$	
28 (24)	V _{DD}	Positive power supply pin	supplies $V_{SS} = -6.0 \sim -17V$ When using a $V_{SS} = -6.0 \sim -10V$	_
13 (11)	GND	Digital GND pin	single power Supply $V_{DD} = 6.0 \sim 18V$ $V_{DD} = 6.0 \sim 18V$ $V_{DD} = 0.0 \sim 18V$ $V_{DD} = 0.0 \sim 18V$	
3 (2)	L-OUT	Volume output	Volume circuit	
26 (23)	R-OUT	pin	оит О	
5 (4)	L-IN		IN O VR	
24 (21)	R-IN	Volume input pin	LD1 0 7.4kΩ LA1 26.3kΩ	
6 (5)	L-LD1		LD2 O 18,7kΩ	
23 (20)	R-LD1	Loudness tap	A-GND O	_
7 (6)	L-LD2	output pin	in	
22 (19)	R-LD2]	LA1 LA2	
8 (7)	L-A-GND	Analan CND min	LOUDNESS "ON" ON OFF LOUDNESS "OFF" OFF ON	
21 (18)	R-A-GND	Analog GND pin	EGGENESS OF OF ON	
10 (9)	CS1	Chip select input	Up to 4 chips on the same bus can	
19 (16)	CS2	pin	be used by switching over chip select code.	_
14 (12)	СК	Clock input pin	Data transfer clock input	Low
15 (13)	DATA	Data input pin	Volume setup serial data input	threshold value
16 (14)	STB	Strobe input pin	Data write strobe input	input pin
2 (3) 27 (22)				
4 25 9 (8)	NC	No connection	_	_
20 (17) 11 18				
12 (10) 17 (15)				

DEVICE OPERATION

Setting up volume value (amount of attenuation)
 Serial data consisting of 24bits is used to set a volume value.

• Data format



(1) Chip select data

The bits "C1" through "C4" are the chip select code data.

These bits set the code data that corresponds to the CS1 and CS2 inputs.

CS1	CS2	C1	C2	С3	C4
L	L	0	0	0	1
Н	L	1	0	0	1
L	Н	0	1	0	1
Н	Н	1	1	0	1

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(2) Loudness setting

The bit "LD" is the loudness setup data. Loudness is turned on when LD = 1.

(3) Volume setup data

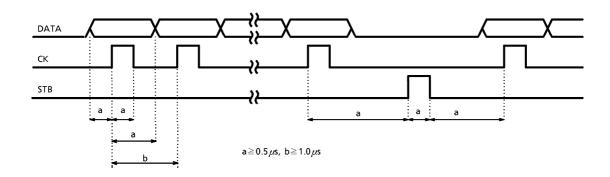
The bits "D01" through "D07" are the left channel volume setup data, the bits "D11" through "D17" are the right channel volume setup data. For details, see the tables below.

VOLUME VALUE D01 D01 D02 D03 D04 D05 D06 D07 D15 D16 D17 D06 D07 D15 D16 D17 0dB 0	D17 G1	e tile				voidi		P
OdB 0 0 0 0 0 0 0 -1 1 0 0 0 0 0 0 -2 0 1 0 0 0 0 0 -3 1 1 0 0 0 0 0 -4 0 0 1 0 0 0 0 -5 1 0 1 0 0 0 0 -6 0 1 1 0 0 0 0 -7 1 1 1 0 0 0 0 -9 1 0 0 1 0 0 0 -10 0 1 0 1 0 0 0 -11 1 1 0 1 0 0 0 -11 1 1 1 1 0 0								
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-2 0 1 0 0 0 0 0 -3 1 1 0 0 0 0 0 -4 0 0 1 0 0 0 0 -5 1 0 1 0 0 0 0 -6 0 1 1 0 0 0 0 -7 1 1 1 0 0 0 0 -8 0 0 0 1 0 0 0 -9 1 0 0 1 0 0 0 -10 0 0 1 0 0 0 0 -11 1 1 0 1 0 0 0 -12 0 0 1 1 0 0 0 -11 1 1 1 1 0 0		1	0	0	0	0	0	
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	– 45	1	0	1	1	0	1	0

ta.	a. For details, see the tables below.									
	VOLUME	D01	D02	D03	D04	D05	D06	D07		
_	VALUE	D11	D12	D13	D14	D15	D16	D17		
L	– 46dB	0	1	1	1	0	1	0		
	– 47	1	1	1	1	0	1	0		
	– 48	0	0	0	0	1	1	0		
	- 49	1	0	0	0	1	1	0		
	– 50	0	1	0	0	1	1	0		
	– 51	1	1	0	0	1	1	0		
	- 52	0	0	1	0	1	1	0		
	- 53	1	0	1	0	1	1	0		
	- 54	0	1	1	0	1	1	0		
	- 55	1	1	1	0	1	1	0		
	- 56	0	0	0	1	1	1	0		
	– 57	1	0	0	1	1	1	0		
	- 58	0	1	0	1	1	1	0		
	- 59	1	1	0	1	1	1	0		
Г	- 60	0	0	1	1	1	1	0		
	– 61	1	0	1	1	1	1	0		
F	- 62	0	1	1	1	1	1	0		
	- 63	1	1	1	1	1	1	0		
Н	- 64	0	0	0	0	0	0	1		
H	- 65	1	0	0	0	0	0	1		
Н	- 66	0	1	0	0	0	0	1		
H	- 67	1	1	0	0	0	0	1		
\vdash	- 68	0	0	1	0	0	0	1		
H	- 69	1	0	1	0	0	0	1		
\vdash	- 70	0	1	1	0	0	0	1		
\vdash	-70	1	1	1	0	0	0	1		
\vdash	-71	0	0	0	1	0	0	1		
\vdash	-73	1	0	0	1	0	0	1		
\vdash	- 73 - 74	0	1	0	1	0	0	1		
\vdash	- 7 4 - 75	1	1	0	1	0	0	1		
\vdash				1	1		0	1		
\vdash	– 76 – 77	0 1	0	1	1	0	0	1		
\vdash										
\vdash	<u>- 78</u>	0	1	1	1	0	0	1		
\vdash	- 79 80							'		
\vdash	- 80 81	0	0	0	0	1	0	1		
\vdash	- 81 82	1	0	0	0	1	0	1		
\vdash	- 82	0	1	0	0	1	0	1		
\vdash	- 83	1	1	0	0	1	0	1		
\vdash	- 84	0	0	1	0	1	0	1		
\vdash	- 85 - 85	1	0	1	0	1	0	1		
\vdash	<u>- 86</u>	0	1	1	0	1	0	1		
\vdash	<u>- 87</u>	1	1	1	0	1	0	1		
\vdash	- 88	0	0	0	1	1	0	1		
	– 89	1	0	0	1	1	0	1		
L	_ ∞	0	1	0	1	1	0	1		

2. Serial data timing

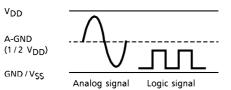
Make sure that CK, DATA and STB are input to the device at the timings shown below.



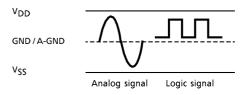
3. Operating with a single or dual power supplies

The TC9459N, TC9459F can operate with either a single power supply or dual power supplies.

• Operation with single power supply



Operation with dual power supplies



MAXIMUM RATINGS (Ta = 25°C)

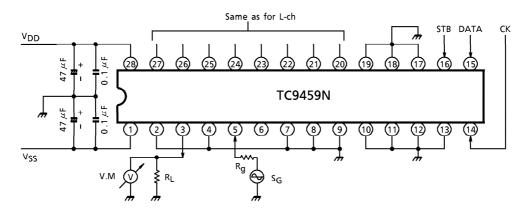
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage (1)	V _{DD} -V _{SS}	-0.3~36	V
Supply Voltage (2)	V _{DD} -GND	-0.3~20	٧
GND Block Input Voltage	V _{IN} (1)	-0.3~V _{DD} +0.3	٧
V _{SS} Block Input Voltage	V _{IN} (2)	$V_{SS} - 0.3 \sim V_{DD} + 0.3$	٧
Power Dissipation	PD	300	mW
Operating Temperature	T _{opr}	- 40~85	°C
Storage Temperature	T _{stg}	-65~150	°C

ELECTRICAL CHARACTERISTICS (Referenced to $V_{DD} = 15V$, $V_{SS} = -15V$, $V_{SS} = -15$

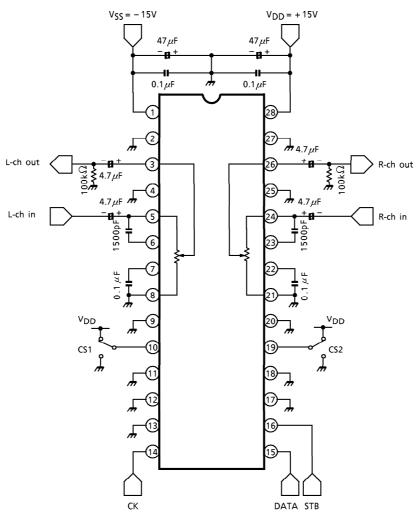
(יייי טטיי	. 33	,	7 = 01 at 1a = 23 e amess oc		,		
CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Su (1)	upply Voltage	V _{DD} -V _{SS}	1	Operating with dual power supplies	12	?	34	V
Operating Su (2)	upply Voltage	V _{DD} -GND	ı	Operating with single power supply	6.0	?	18	V
Operating Su	apply Current	I _{DD}	1	Non-loaded, no input		0.5	2.0	mA
Input	"H" Level	V _{IH} (1)		CK, DATA, STB pins	4.0	~	V_{DD}	v
Voltage	"L" Level	V _{IL} (1)	_	V _{DD} = 6.0∼18V	GND	~	1.0	
Input	"H" Level	V _{IH} (2)		CS1 and CS2 pins	$V_{DD} \times 0.7$?	V_{DD}	\ \
Voltage	"L" Level	V _{IL} (2)	_	CST and CS2 pins	GND	~	$V_{DD} \times 0.3$	V
Input	"H" Level	ΙΗ		CK, DATA, STB, V _{IH} = 15V	- 1.0	~	1.0	
Current	"L" Level	I _Ι L	_	CS1, CS2 pins $V_{IL} = 0V$	- 1.0	~	1.0	μ A
Operating Frequency		fop			0	~	1.0	MHz
Min. Operating Clock Width		Tck	_	CK, DATA, STB pins	0.5	_	_	μs
Volume Resi	stance	R _{VR}	_	When loudness OFF	20.5	29.3	38.2	kΩ
Step Deviation	on	∆VR	_	Deviation between volume steps	- 1.2	~	1.2	dB
Analog Swite	ch ON-	RON (1)		Analog switch LA2 only	_	350	_	
Analog Switch ON- Resistance		R _{ON} (2)		All analog switch except for LA2		750	1500	Ω
Analog Switch Leakage Current		lOFF	_	Internal analog switch	- 0.1	{	0.1	μΑ
Total Harmonic Distortion		THD		f _{IN} = 1kHz	_	0.005	_	%
Maximum Attenuation		ATTMAX	1	V _{IN} = 1Vrms	_	100	_	dB
Output Noise Voltage		٧N	'	$R_g = 600\Omega$, $R_L = 100k\Omega$	_	1.0	-	μ V $_{rms}$
Crosstalk		C·T		BW = 20Hz~20kHz	_	100	_	dB

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TEST CIRCUIT 1 (IDD/THD/ATTMAX/VN/CT)



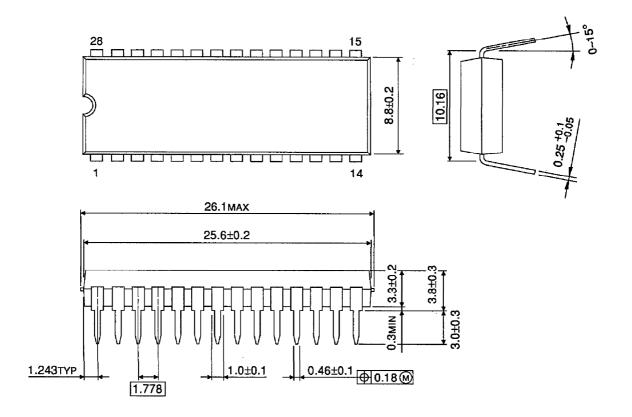
EXAMPLE OF APPLICATION CIRCUIT (TC9459N)



(Note) Since a high-frequency digital signal is input to the CK, DATA and STB pins, corrective measures must be taken to prevent it from getting mixed in the analog circuit to generate noise by, for example, guarding the above signal lines with ground patterns or using shielding wire for these lines.

PACKAGE DIMENSIONS

SDIP28-P-400-1.78 Unit: mm



Weight: 2.2g (Typ.)

Weight: 0.44g (Typ.)

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000707EBA

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