Loopback Implementation in Baseband Processor Mix-signal Testing

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Agenda

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- Proposed implementation of loopback
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Background

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- Highly-integrated SOC devices, such as the cellular base band processor is very sensitive in terms of cost of test. Lowering the costs for testing these devices is becoming a competitive challenge.

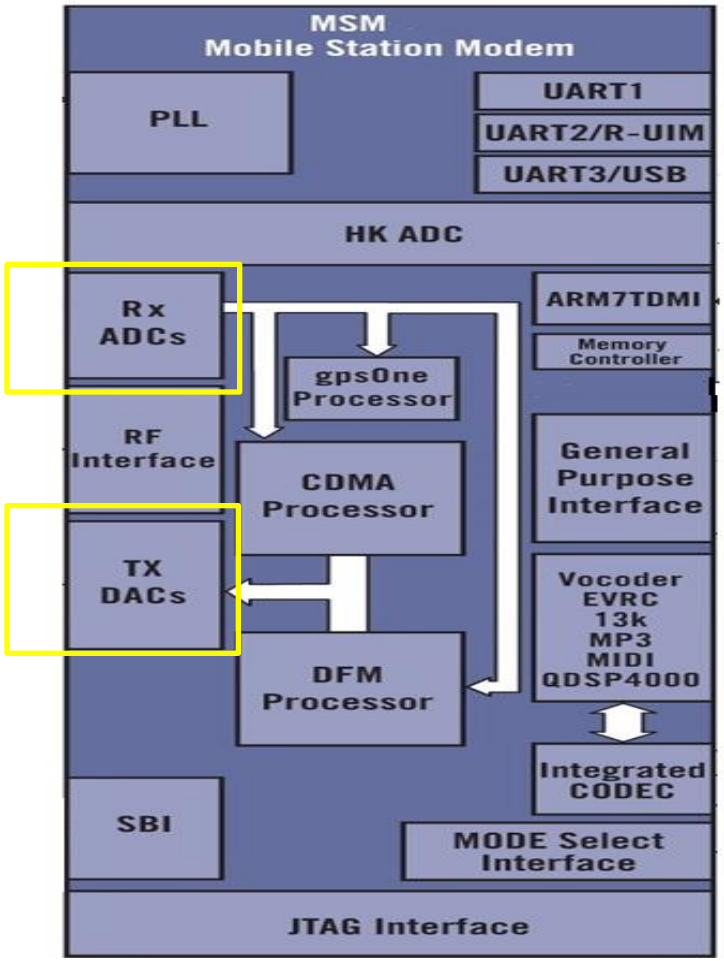
- Moreover the integration of more and more features into the device, like high speed digital interfaces, analog and RF prevents the use of wafer sort tester without analog resource.

- To bring some mix-signal tests coverage (CalDACs and BBRxs) into wafer sort with existing wafer sort tester configuration, which would increase the yield of final test and reduce total test cost.

- A CalDACs to BBRxs loopback test within the base band processor has been proposed. Hardware setup of the loopback test is to connect output of CalDACs to the input of BBRxs on the loadboard (relay or jumper wire).

Device application and system config

MSM(Mobile Station Modem) Device



This device embeds:

I/Q receive ADCs (BBRxs)

Transmit DACs (CalDACs)

Analog board (**MCE/MCB**) is needed to test BBRxs and CalDACs module separately.

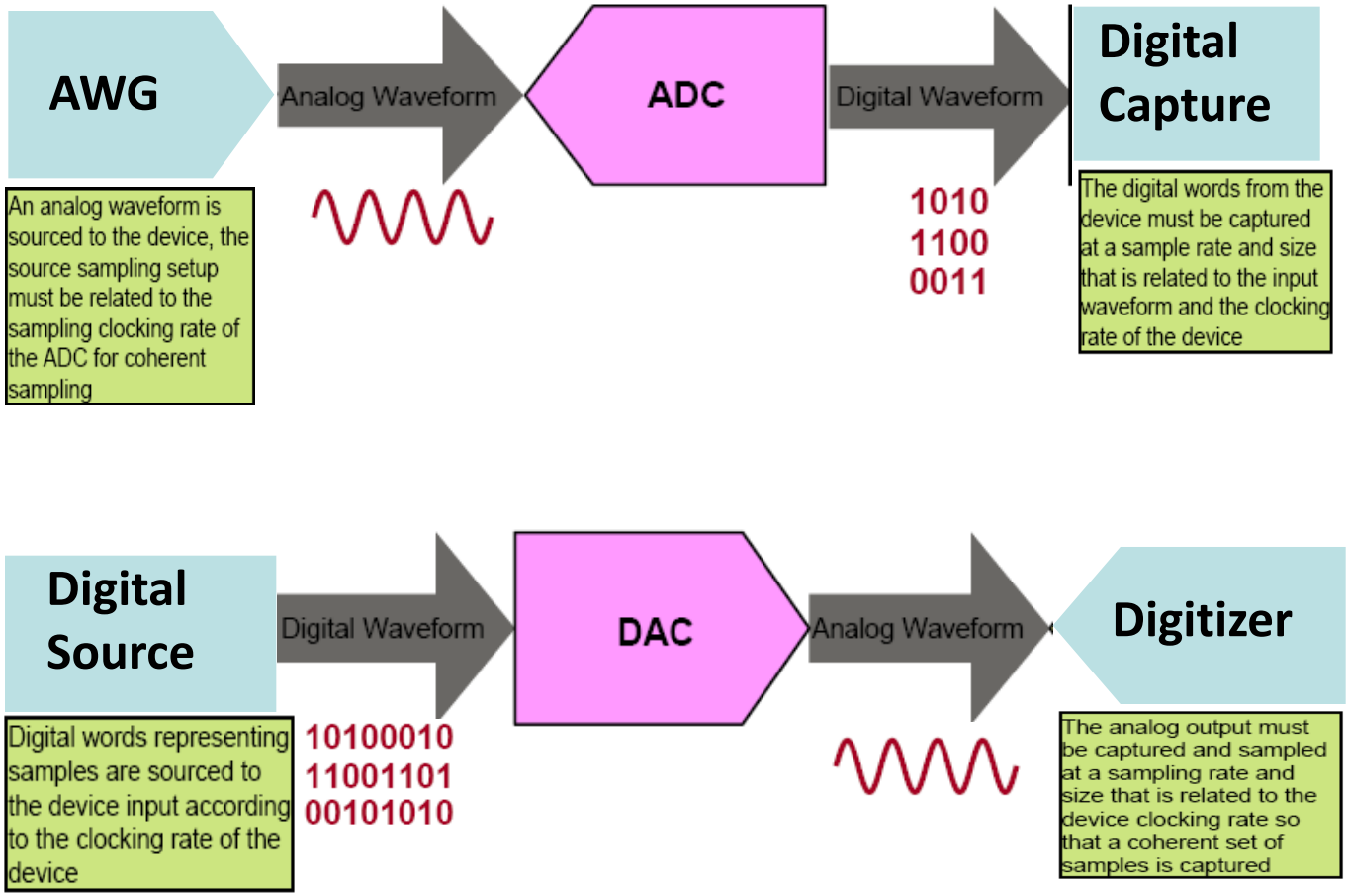
A CalDACs to BBRxs loopback test within the DUT was proposed to bring some mix-signal tests coverage for CalDACs and BBRxs, which no analog board is needed.

The proposed test-system configuration is an Advantest V93000 Smart Scale system with existing wafer sort tester configuration: **PS1600** and **DPS32** only.

Allows for testing 8 devices in parallel.

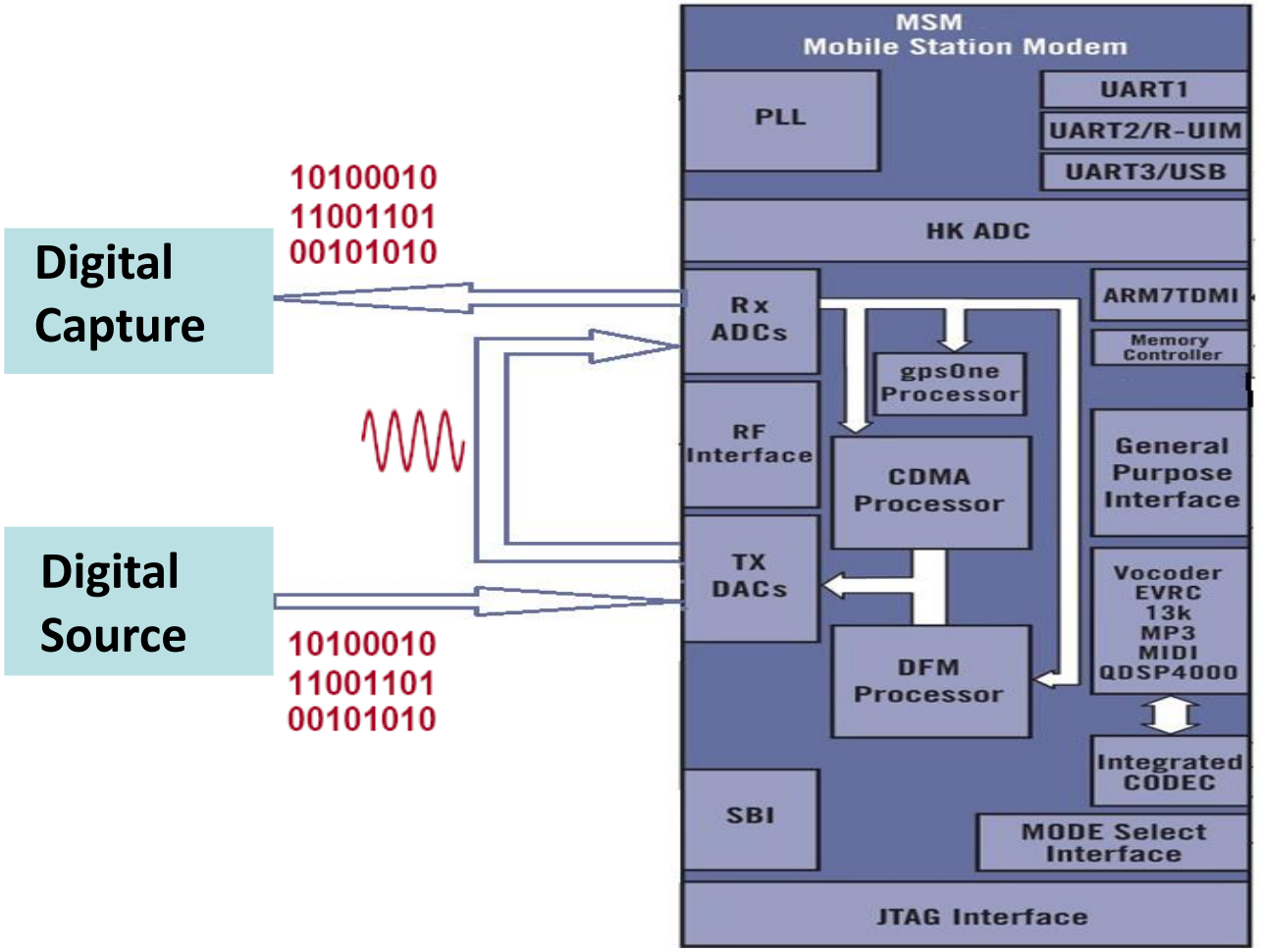
Current solution to test ADCs and DACs

To test these SOC devices, we will need instruments which are capable of applying analog and/or digital signals to the DUT and capture + analyzing analog and/or digital responses.



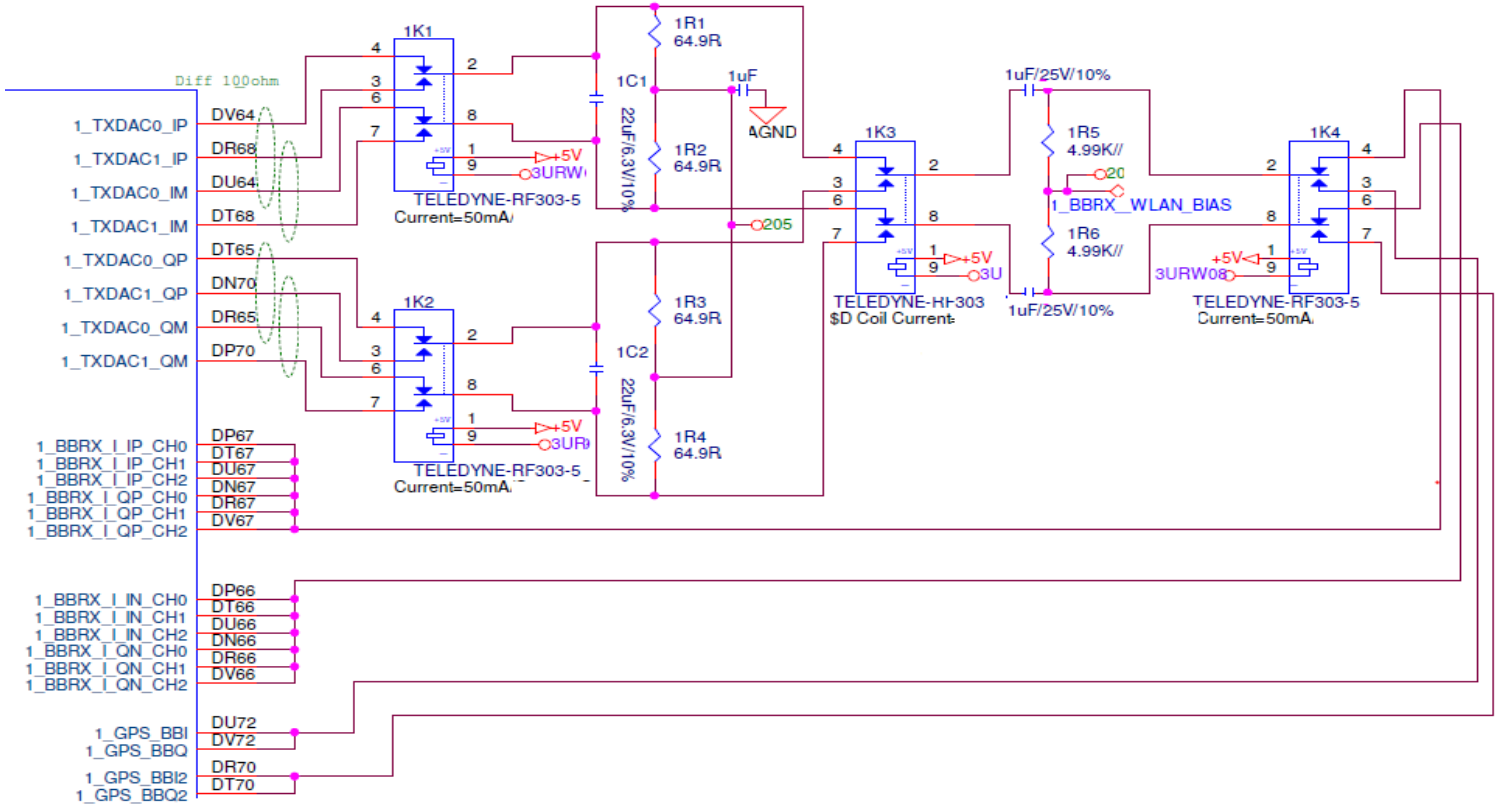
Proposed implementation of loopback

In order to have mixed signal test coverage with wafer sort tester configuration, A CalDACs to BBRxs loopback test within the DUT was proposed. No Analog board is needed for this mix-signal test.



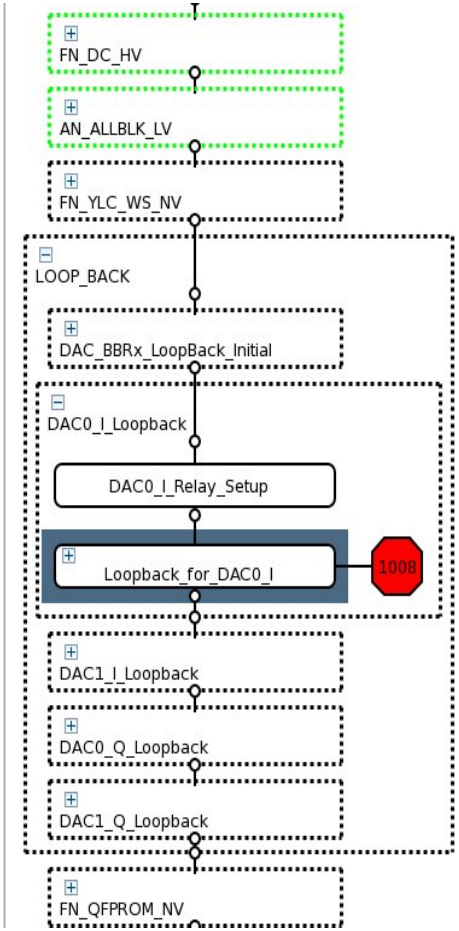
Loopback hardware and testsuits setup

Hardware setup of the loopback test is to connect output of CalDACs to the input of BBRXs on the loadboard (relay or jumper wire).



The CalDACs (DAC0,DAC1) I/Q signal fan-out to be the input of 3 BBRxs (ADC0,ADC1,ADC2) I/Q separately.

Loopback hardware and testsuits setup



Primaries	...
Timing	15, 1, 1
Level	1, @LVL_SPEC + 7, 2
Analog	
Pattern	txdac_BBR_GSM_loopback
Context	DEFAULT
Test Type	M
Test Method	Waverider_rsb_tml.BBRx.MEMPOOL
Parameters	BBRX_LTE20_ATTEN_100K_9M, , bbrx_8k_cap_loopback, O
Analog Set Name	BBRX_LTE20_ATTEN_100K_9M
adc_pin	
Vect_Var_Name	bbrx_8k_cap_loopback
Connect	OPEN
capt_pts	8192
BBRX Design	ATLAS
Data Process	MEMPOOL
DAC_ref_voltage (V	1.2
Device Operating M	LTE20
ATE Test Mode	1TONE_SNDR
IRDCoffset	OFF
Noise_bw_l	4
Noise_bw_h	191
Fundamental_bin	14
Fundamental_bin_2	28
Fundamental_bin_3	42
Fundamental Leaka	5

Digital Source for CalDAC input and Digital Capture output of BBRx are combined in one vector.

No Analog set required as no analog instrument is used. (for debugging purpose only)

Vector variable is created for digital capture.

No need to connect to any analog instrument.

4 testsuits: DAC0_I_Loopback, DAC0_Q_Loopback, DAC1_I_Loopback, DAC1_Q_Loopback are created for 4 different loopbacks.

Debugging procedure for loopback

The loopback debugging could be a challenging job. The loopback test is used to measure the overall performance of CalDAC and BBRx. To check the CalDAC and BBRx separately, analog instruments (MCE, MCB) is needed.

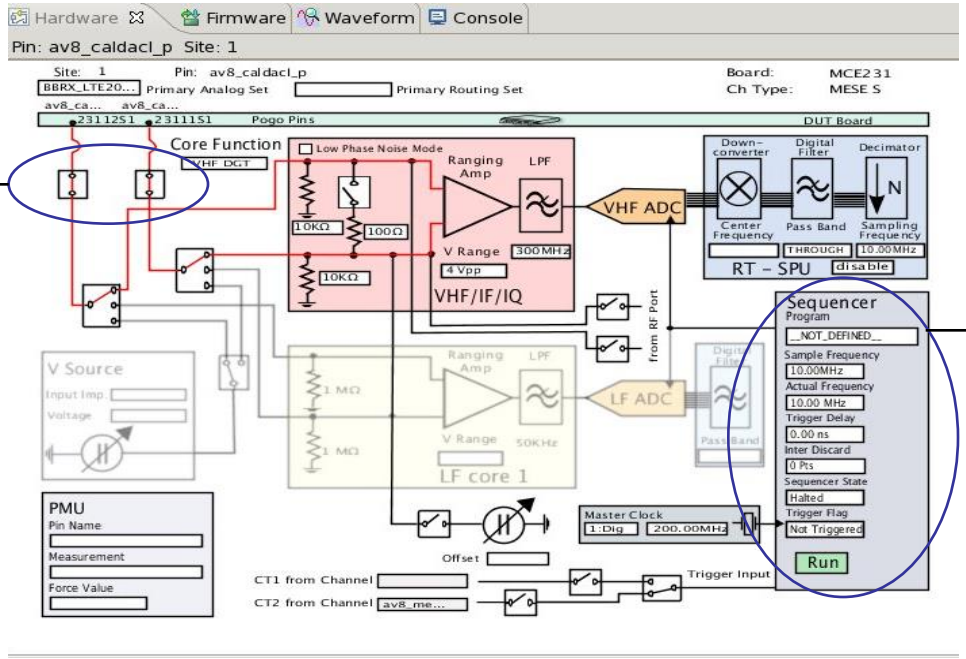
Step 1: To check CalDAC performance, make sure it working correctly. Connect the output of CalDAC to Digitizer by relay or jumper wire.

Keep the digital input of CalDAC looping on by looping the vector:

Task>> SQGB ELPT, ; SQST RUN

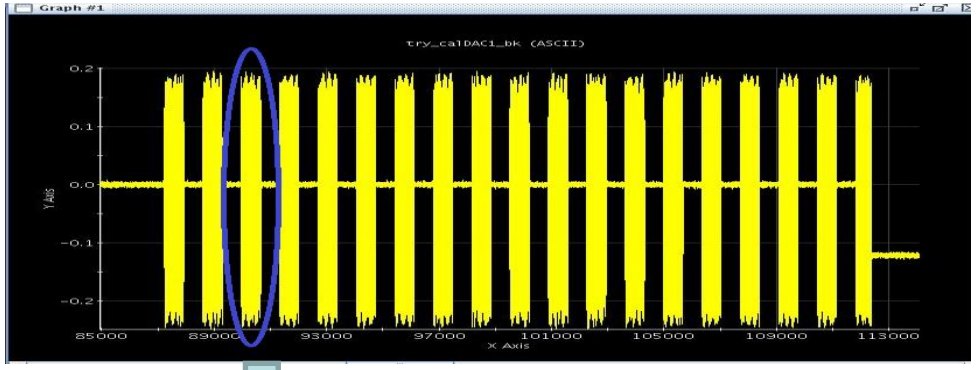
Set the digitizer for capture as following:

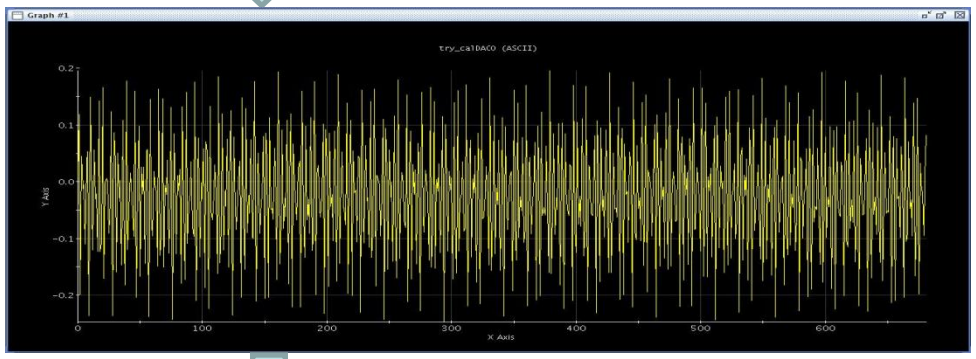
Connect the digitizer to output of CalDAC



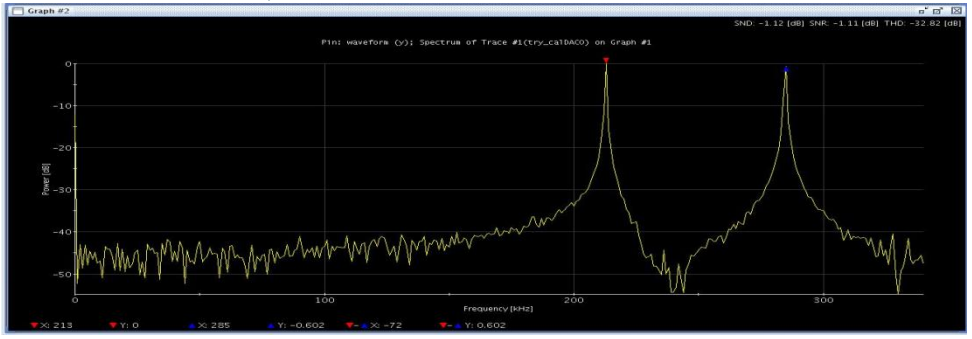
Set up the digitizer sample frequency (Fs) and manually trigger the digitizer to get samples of CalDAC output.

Debugging procedure for loopback





Spectrum Analyzer in Frequency domain



Repeated waveforms are captured on output of CalDAC as the digital input of CalDAC keeping looping.

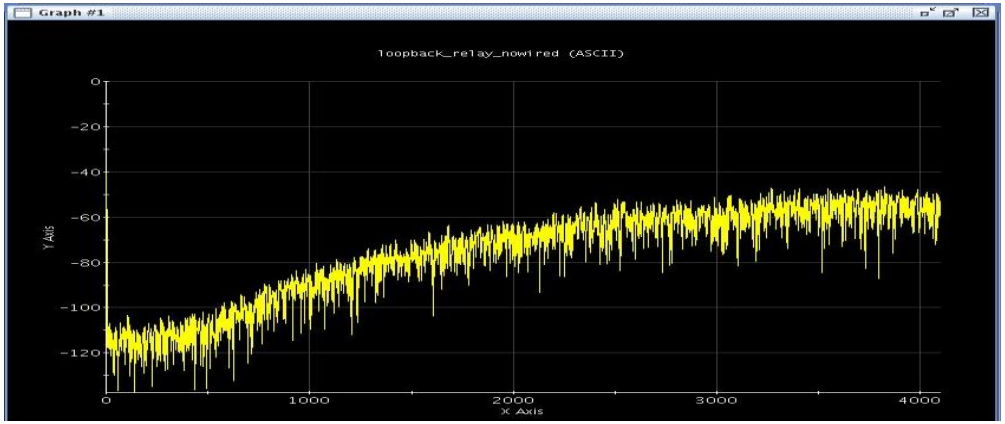
Take single waveform as example, the spectrum in frequency domain shows a dual tone signal.

Tester digitizer setup:
Sampling frequency Fs=10 MHz
The capture points for single waveform: N=680

Spectrum show frequency bin :
Freq1=213 Freq2=285
The two tone frequency:
Ft1=Freq1*Fs/N = 3.13MHz
Ft2=Freq2*Fs/N = 4.19MHz

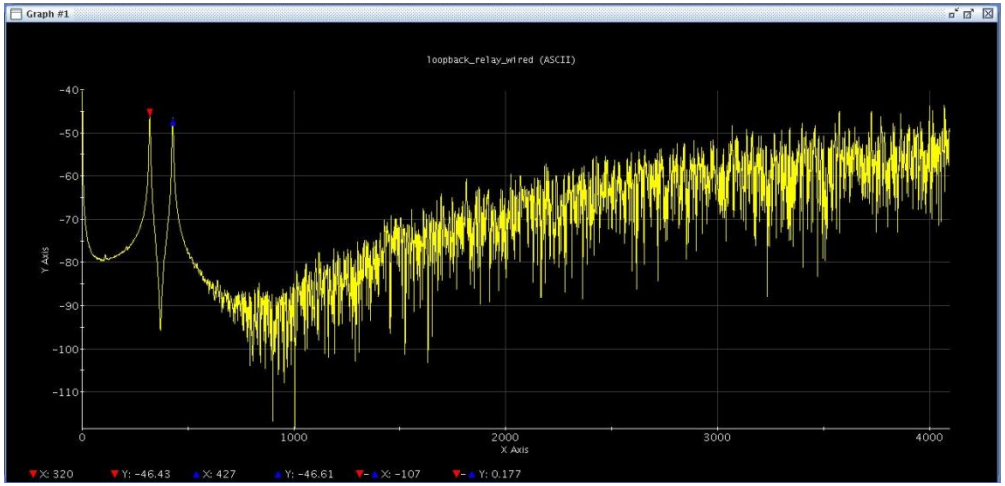
Debugging procedure for loopback

Step 2: Make sure the output of CalDAC correctly, We can use output of CalDAC as analog input of BBRx to check the performance of BBRx. Disconnect the Digitizer from output of CalDAC and switch the output of CalDAC to input of BBRx.



Open circuit (no input of BBRx)

Open connection between CalDAC and BBRx, no signal tone (other than noise level) is captured on output of BBRx.



Loopback circuit (Output of CalDAC as input of BBRx)

Switch the output of CalDAC to input of BBRx. a dual tone signal is captured on output of BBRx.

Debugging procedure for loopback

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A dual tone signal is captured on output of BBRx, which is consistent with what is captured directly from output of CalDAC by using tester digitizer setup.

Above Spectrum shows dual tone frequency bin:

Freq1'=320

Freq2'=427

BBRx samples: N=8192.

Probably calculation on BBRx conversion rate:

Fs = 80.12MHz (Based on Freq1')

Fs'= 80.38MHz (Based on Freq2')

Above BBRx conversion rate is matching with device spec. The whole loopback circuit working correctly, and loopback test success executing some analog testing without analog instrument.

Real device implementation and results

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The loopback tests have been verified to measure performance of CalDAC and BBRx with 8-site wafer probe.

Used V93000 SmartScale System without any analog instruments (MCE, MCB), but digital channel card PS1600 and power supply DPS32 only.

Got good correlation with previous results with analog instruments(MCE).

CalDAC Channel # and I/Q	BBRx Channel # and I/Q	LoopBack
DAC0_I	CH0_I	txDAC0_I----BBRxCh0_I
	CH0_Q	txDAC0_I----BBRxCh0_Q
	CH1_I	txDAC0_I----BBRxCh1_I
	CH1_Q	txDAC0_I----BBRxCh1_Q
	CH2_I	txDAC0_I----BBRxCh2_I
	CH2_Q	txDAC0_I----BBRxCh2_Q
DAC0_Q	CH0_I	txDAC0_Q----BBRxCh0_I
	CH0_Q	txDAC0_Q----BBRxCh0_Q
	CH1_I	txDAC0_Q----BBRxCh1_I
	CH1_Q	txDAC0_Q----BBRxCh1_Q
	CH2_I	txDAC0_Q----BBRxCh2_I
	CH2_Q	txDAC0_Q----BBRxCh2_Q
DAC1_I	CH0_I	txDAC1_I----BBRxCh0_I
	CH0_Q	txDAC1_I----BBRxCh0_Q
	CH1_I	txDAC1_I----BBRxCh1_I
	CH1_Q	txDAC1_I----BBRxCh1_Q
	CH2_I	txDAC1_I----BBRxCh2_I
	CH2_Q	txDAC1_I----BBRxCh2_Q
DAC1_Q	CH0_I	txDAC1_Q----BBRxCh0_I
	CH0_Q	txDAC1_Q----BBRxCh0_Q
	CH1_I	txDAC1_Q----BBRxCh1_I
	CH1_Q	txDAC1_Q----BBRxCh1_Q
	CH2_I	txDAC1_Q----BBRxCh2_I
	CH2_Q	txDAC1_Q----BBRxCh2_Q

24 loopbacks are formed by 4 CalDAC(I/Q) and 6 BBRx(ADCs I/Q), totally 24 different loopback test are done.

Real device implementation and results

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More production data about the SNR calculation for single tone input.

DAC_I_to_BBRx_loopback

Test Suite	Test	Lowe	Uppe	Unit	Min	Max	Mean	Sdev	Cpk	Coun	Fail	Time (ms
An_DAC0_BBRx_Loopback	An_DAC0_BBRx_Loopback_SNR_I_CH0	40	100	dB	58.34	59.77	59.07	0.3894	16.32	20	0	0.038
An_DAC0_BBRx_Loopback	An_DAC0_BBRx_Loopback_SNR_Q_CH0	40	100	dB	58.48	60.14	59.195	0.4039	15.84	20	0	0.029
An_DAC0_BBRx_Loopback	An_DAC0_BBRx_Loopback_SNR_I_CH1	40	100	dB	57.45	59.98	58.743	0.6493	9.622	20	0	0.051
An_DAC0_BBRx_Loopback	An_DAC0_BBRx_Loopback_SNR_Q_CH1	40	100	dB	57.21	60.69	59.102	0.8632	7.377	20	0	0.03
An_DAC0_BBRx_Loopback	An_DAC0_BBRx_Loopback_SNR_I_CH2	40	100	dB	57.86	59.31	58.674	0.3987	15.61	20	0	0.135
An_DAC0_BBRx_Loopback	An_DAC0_BBRx_Loopback_SNR_Q_CH2	40	100	dB	58	60.05	59.098	0.5544	11.48	20	0	0.037
An_DAC1_BBRx_Loopback	An_DAC1_BBRx_Loopback_SNR_I_CH0	40	100	dB	58.22	60.32	59.59	0.5896	11.08	20	0	0.053
An_DAC1_BBRx_Loopback	An_DAC1_BBRx_Loopback_SNR_Q_CH0	40	100	dB	58.43	60.41	59.468	0.5682	11.42	20	0	0.034
An_DAC1_BBRx_Loopback	An_DAC1_BBRx_Loopback_SNR_I_CH1	40	100	dB	58.59	60.77	59.596	0.5841	11.18	20	0	0.173
An_DAC1_BBRx_Loopback	An_DAC1_BBRx_Loopback_SNR_Q_CH1	40	100	dB	58.25	60.83	59.792	0.6073	10.86	20	0	0.041
An_DAC1_BBRx_Loopback	An_DAC1_BBRx_Loopback_SNR_I_CH2	40	100	dB	58.01	60.47	59.402	0.6176	10.47	20	0	0.035
An_DAC1_BBRx_Loopback	An_DAC1_BBRx_Loopback_SNR_Q_CH2	40	100	dB	58.6	60.24	59.419	0.5294	12.23	20	0	0.048

DAC_Q_to_BBRx_loopback

Test Suite	Test	Lowe	Uppe	Unit	Min	Max	Mean	Sdev	Cpk	Coun	Fail	Time (ms
An_DAC0_BBRx_Loopback	An_DAC0_BBRx_Loopback_SNR_I_CH0	40	100	dB	58.42	60.71	59.447	0.5354	12.11	20	0	0.041
An_DAC0_BBRx_Loopback	An_DAC0_BBRx_Loopback_SNR_Q_CH0	40	100	dB	58.36	60.34	59.277	0.5397	11.91	20	0	0.044
An_DAC0_BBRx_Loopback	An_DAC0_BBRx_Loopback_SNR_I_CH1	40	100	dB	57.96	60.03	59.04	0.5364	11.83	20	0	0.043
An_DAC0_BBRx_Loopback	An_DAC0_BBRx_Loopback_SNR_Q_CH1	40	100	dB	57.3	59.96	59.069	0.6249	10.17	20	0	0.04
An_DAC0_BBRx_Loopback	An_DAC0_BBRx_Loopback_SNR_I_CH2	40	100	dB	57.32	59.47	58.462	0.682	9.023	20	0	0.037
An_DAC0_BBRx_Loopback	An_DAC0_BBRx_Loopback_SNR_Q_CH2	40	100	dB	58.15	59.86	58.904	0.5006	12.59	20	0	0.042
An_DAC1_BBRx_Loopback	An_DAC1_BBRx_Loopback_SNR_I_CH0	40	100	dB	58.2	60.94	59.524	0.7275	8.946	20	0	0.045
An_DAC1_BBRx_Loopback	An_DAC1_BBRx_Loopback_SNR_Q_CH0	40	100	dB	59.37	60.74	59.954	0.4199	15.84	20	0	0.118
An_DAC1_BBRx_Loopback	An_DAC1_BBRx_Loopback_SNR_I_CH1	40	100	dB	57.82	60.3	59.242	0.6375	10.06	20	0	0.048
An_DAC1_BBRx_Loopback	An_DAC1_BBRx_Loopback_SNR_Q_CH1	40	100	dB	58.63	60.49	59.414	0.4587	14.11	20	0	0.058
An_DAC1_BBRx_Loopback	An_DAC1_BBRx_Loopback_SNR_I_CH2	40	100	dB	58.62	60.34	59.617	0.4645	14.08	20	0	0.194
An_DAC1_BBRx_Loopback	An_DAC1_BBRx_Loopback_SNR_Q_CH2	40	100	dB	58.53	60.4	59.453	0.5408	11.99	20	0	0.096

Summary and conclusion

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- A solution for testing CalDACs and BBRx within the base band processor in wafer sort tester configuration has been shown.
- Loopback implementation success executing some analog testing without analog instrument, bring some analog tests coverage for CalDAC and BBRx.
- Confirmed COT reduction by covering some analog tests during wafer sorting.
- This work shows that the digital Pins allows for testing CalDAC and BBRx within the base band processor without the need of additional and dedicated Mixed Signal hardware.
- The loopback test is to measure the overall performance of CalDAC and BBRx. However, to check the CalDAC and BBRx separately, analog instruments (MCE, MCB) is needed.