

AWG trigger issue with SOC_TML

During debugging digital capture test with SOC_TML, it is observed that the AWG trigger is enabled only for the first run, there will be no trigger enabled for the subsequent execution. The original flow has no analog set loaded as it will be generated during test execution. Adding a dummy analog set will help to fix the issue.

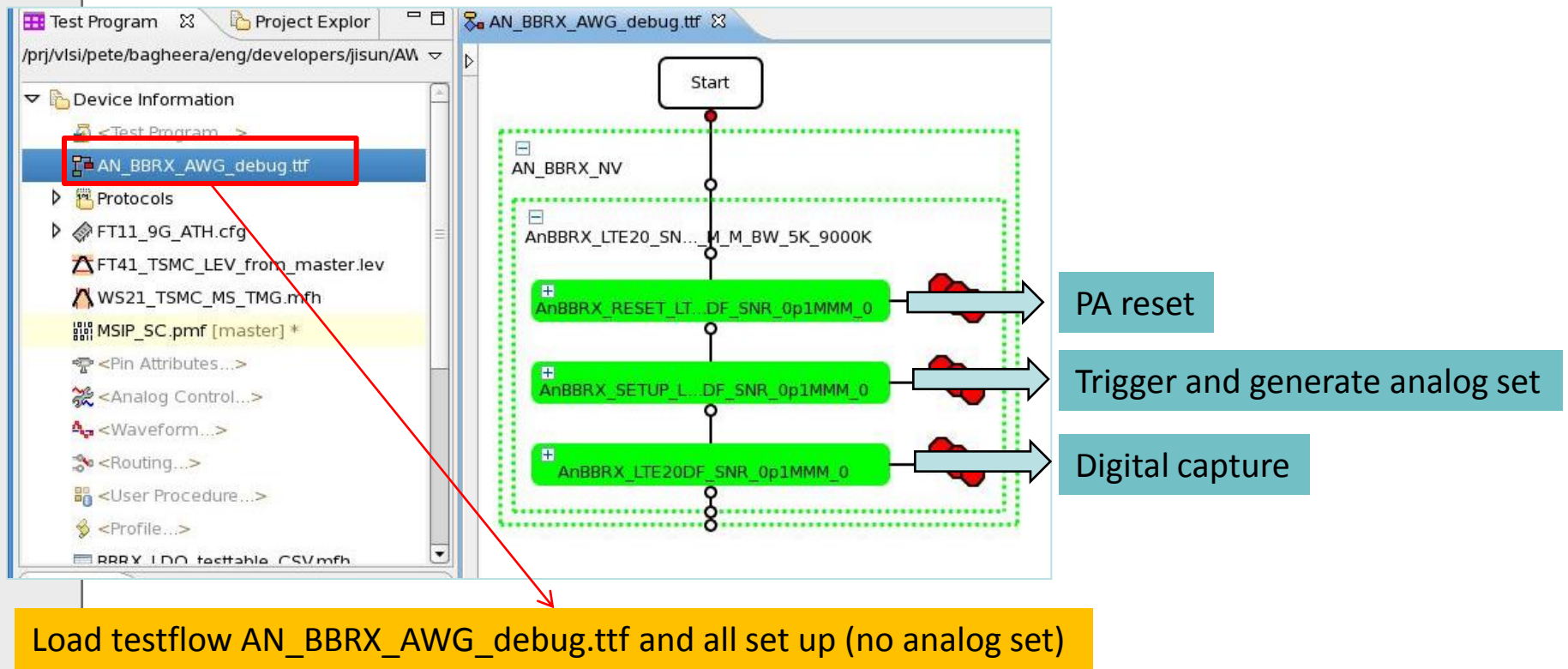
Is this behavior expected? If so, please help to document somewhere that an analog set (even dummy) is needed for mixed signal test.

If not, it think this case is a bug.

Please refer to following slides to reproduce the issue.

To produce. Step 1

- i. Download program “AWG_debug.tar.gz” from <ftp.verigy.com> under folder liyuan
- ii. Untar program and load testflow “AN_BBRX_AWG_debug.ttf” and all setups on R&D high pin count tester **online** under SMT7.2.1.3 with license [PS9G_on_ATH_PS1600_Site1.license]

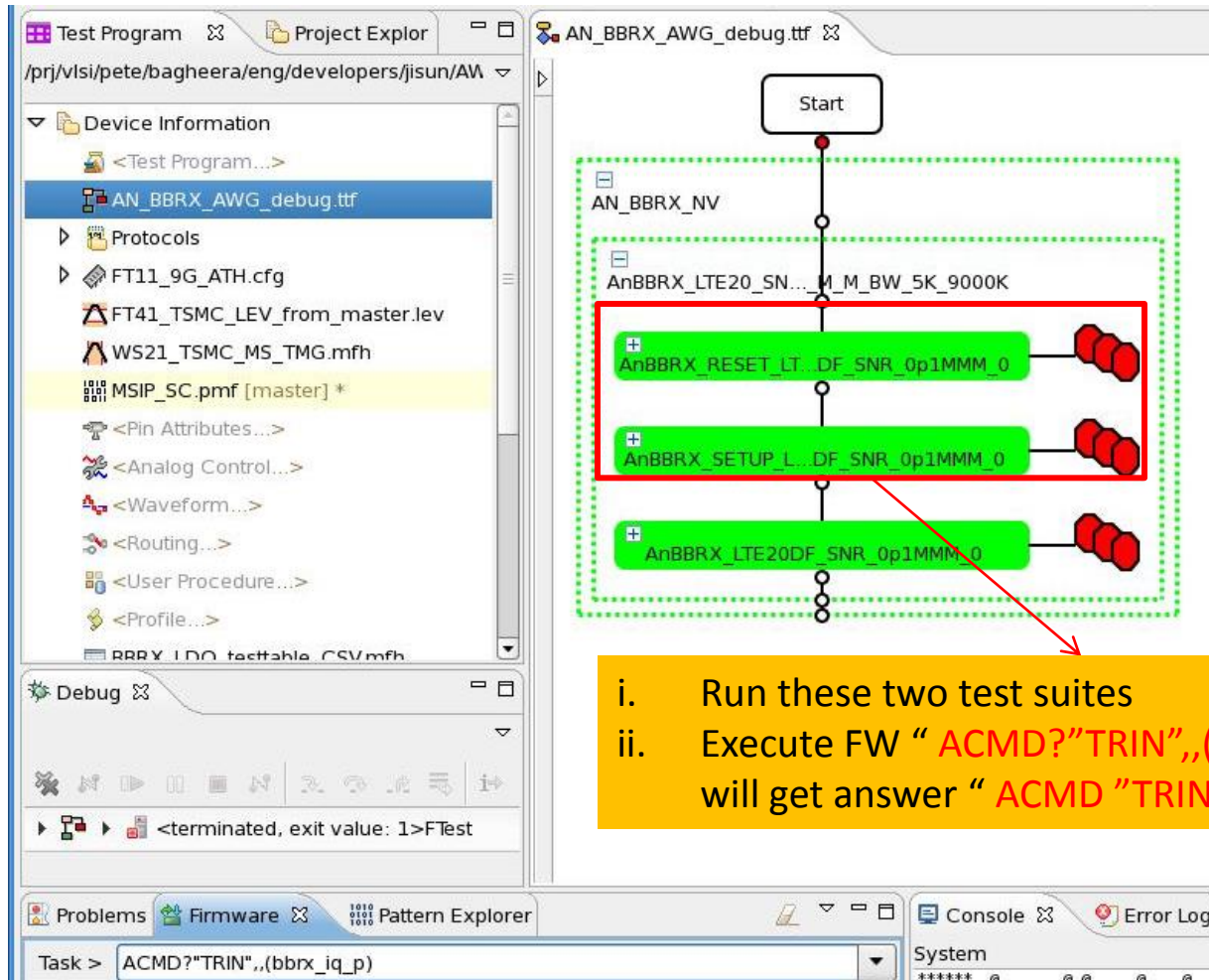


To produce. Step 2

- i. To use jumper wire to connect digital pin a241 (11615) to MCE23117-S2(CT1) which is to set up trigger connection (could use normal diagnostic board for wire connection)

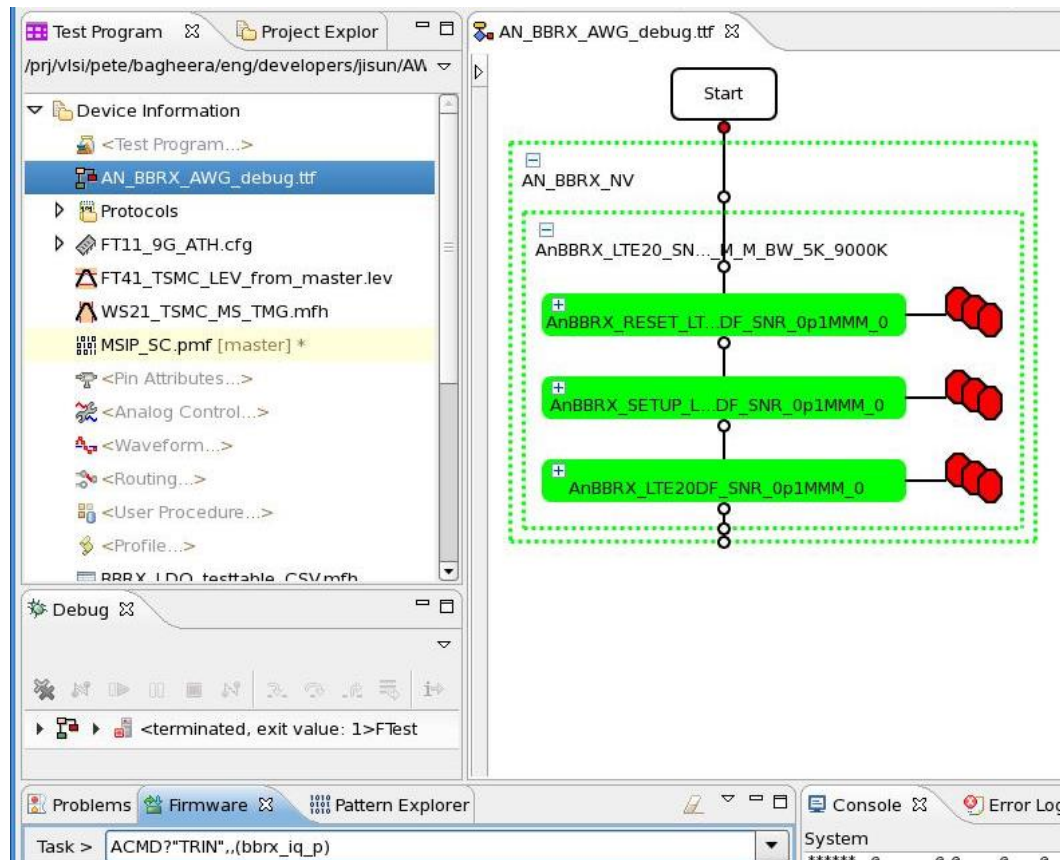
To produce. Step 3

- i. Run the first two test suites together
- ii. Execute FW “ACMD?"TRIN",,(bbrx_iq_p) “ and will get answer “ACMD "TRIN",YES,(bbrx_iq_p) “



To produce. Step 4

- i. Execute the all three test suites together
- ii. Then execute the first two test suites together
- iii. Execute FW “ACMD?“TRIN“, (bbrx_iq_p) “ and will get answer “ACMD“TRIN“,NO,(bbrx_iq_p) “ (No more trigger)
- iv. Reload pin configuration and everything could be reproduce again.



To produce. Step 5

- i. Create a dummy analog set and run those test suites according to step4 & 5
- ii. The trigger will always be enabled.

New Analog Control

Create analog control

Enter analog control name

Name: dummy

Location: /prj/vlsi/pete/bagheera/eng/developers/jisun/AWG_debug/analog_control

i. Create a dummy analog set

