TCE User Group Meeting
Effect of CTIM/CLEV/MEAS on Digital Capture

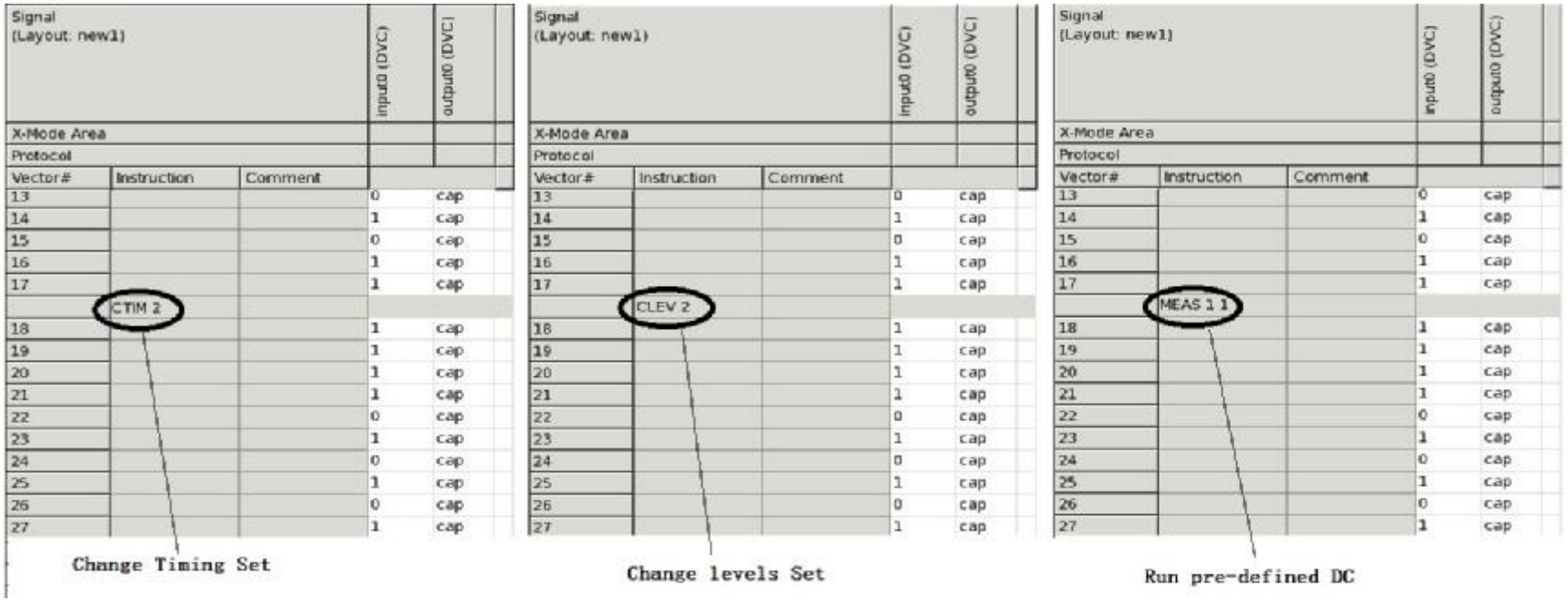
Presented by: Stephen Fu

05-Aug-2013

Issues with Digital Capture

During execution of a pattern, You may need to :

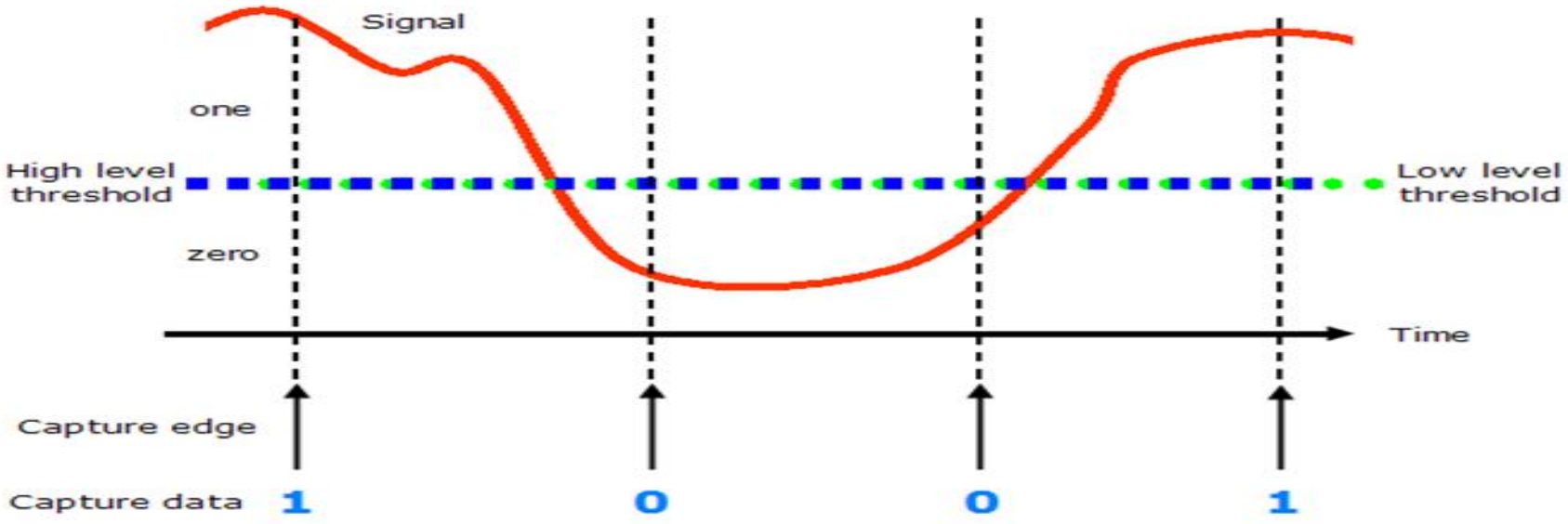
- Switch timing sets to run part of the pattern at a different frequency.
- Switch level sets to run part of the pattern at a different level.
- Run pre-defined PPMU tests within a pattern with the sequencer instruction MEAS.



These CTIM/CLEV/MEAS actions affect the digital capture action, which will cause capture of dead cycles (zeroes are captured).

Theory of Operation

The output from the device is compared for a logical low, and if the output of the particular comparison is a pass, then the bit captured is a zero, else a one is stored.



Two modes in which digital capture can be set up: Sequential and Selective.

In Sequential Mode, digital capture is carried out on every vector cycle. Resolution can be set in one of two ways: Single Mode or Double Mode.

In Selective Mode, digital capture takes place only on selected cycles.

Digital Capture Setup

Pin Configuration: pins on which digital capture will be carried out, can only be **o** or **io.**

Levels: identical values should always be set for the high and low level thresholds, at the intermediate value.

Timing: different timing setup requirements based on whether a sequential or a selective capture is being performed.

- Sequential Capture
  - Single mode (Only **r1** can be used.)
  - Double mode (**r1** and **r4** are used.)
- Selective Capture
  - Define unique wavetable: **r1:C** (capture),**r1:D** (don't capture)
  - Can be any strobe edges, up to x8 digital capture

Vectors: the pattern must be filled with the desired wavetable entries for the selected pins.

- For sequential capture, the entries are regular compare actions on the capture pins.
- For selective capture, the wavetable entries corresponding to capture actions are entered on the desired cycles. On all other entries where capturing is not required, the don't capture action must be explicitly entered.

Effect of CTIM on Digital Capture

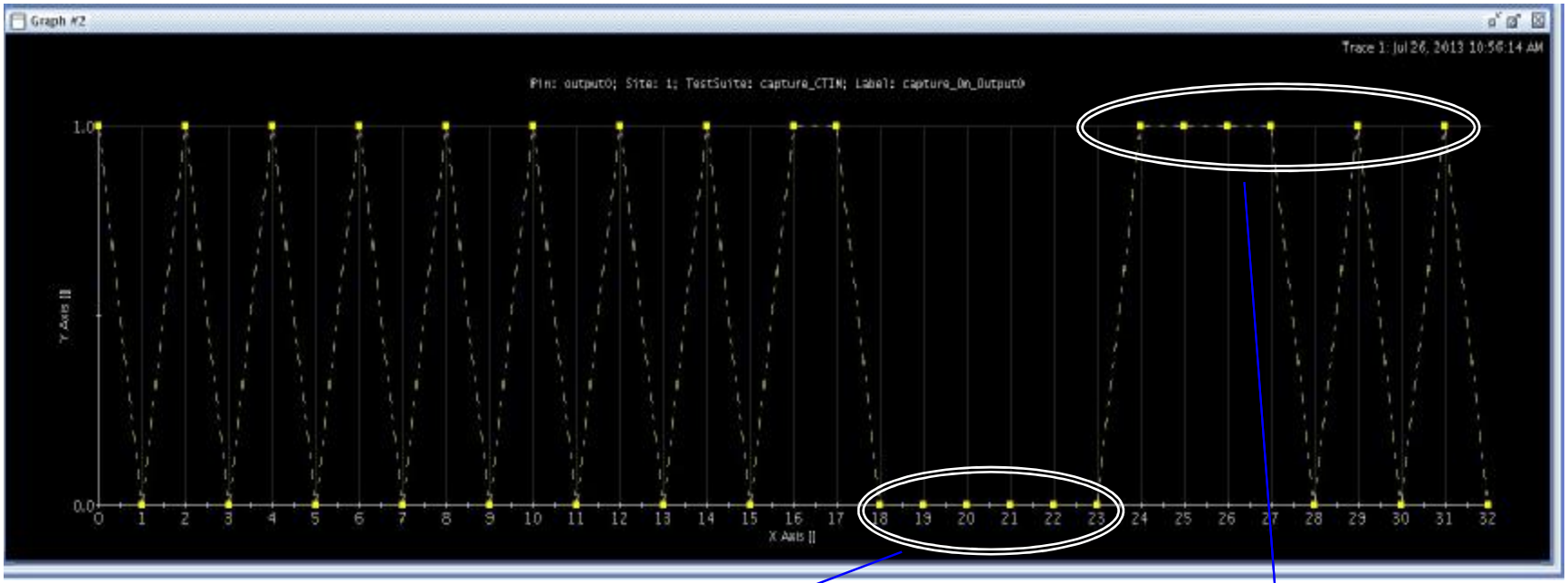
During execution of a pattern, switch timing sets to run part of the pattern at a different frequency. The setup of the pattern is shown below.

Signal (Layout: new1)			Capture_Output0 (Capture)	input0 (DVC)	output0 (DVC)
X-Mode Area					
Protocol					
Vector#	Instruction	Comment			
0			cap	1	cap
1			cap	0	cap
2			cap	1	cap
3			cap	0	cap
4			cap	1	cap
5			cap	0	cap
6			cap	1	cap
7			cap	0	cap
8			cap	1	cap
9			cap	0	cap
10			cap	1	cap
11			cap	0	cap
12			cap	1	cap
13			cap	0	cap
14			cap	1	cap
15			cap	0	cap
16			cap	1	cap
17			cap	1	cap
	CTIM 2				
18			cap	1	cap
19			cap	1	cap
20			cap	1	cap
21			cap	1	cap
22			cap	0	cap
23			cap	1	cap
24			cap	0	cap
25			cap	1	cap
26			cap	0	cap
27			cap	1	cap
28			cap	0	cap
29			cap	1	cap
30			cap	0	cap
31			cap	1	cap
32			cap	0	cap
	STOP				

Data is being driven on pin input0 and capturing actions are set on output0. Just before the CTIM is done after vector 17, a steady 1 signal is being driven by input0. The same is true right after the CTIM. We should expect to see a steady high signal capture around these vectors (16~21).

Effect of CTIM on Digital Capture

The result of switching the period from Tset1 (100ns) to Tset2 (200ns) is presented in the following figure.



6 dead cycles captured

after CTIM, following capturing shift

During the time it takes to switch the timing set, there is capture of dead cycles (zeroes are captured). The switch from 100ns to 200ns led to capturing of six 0 bits.

Effect of CTIM on Digital Capture

Upon further investigation, the following discovery is made:

The number of dead cycles is always equal to the number of cycles that the CTIM instruction is off from a modulo 8 boundary of capture cycles executed.

Signal (Layout: new1)				(CVC) (output)	(CVC) (output)
X-Mode Area					
Protocol					
Cycle#	Vector#	Instruction	Comment		
0	0	GENV 18		1	cap
1	1			0	cap
2	2			1	cap
3	3			0	cap
4	4			1	cap
5	5			0	cap
6	6			1	cap
7	7			0	cap
8	8			1	cap
9	9			0	cap
10	10			1	cap
11	11			0	cap
12	12			1	cap
13	13			0	cap
14	14			1	cap
15	15			0	cap
16	16			1	cap
17	17			1	cap
18	18	CTIM 2		BREAK	BREAK
19	18			BREAK	BREAK
20	18			BREAK	BREAK
21	18			BREAK	BREAK
22	18			BREAK	BREAK
23	18			BREAK	BREAK
24	18	GENV 15		1	cap
25	19			1	cap
26	20			1	cap
27	21			1	cap
28	22			0	cap
29	23			1	cap
30	24			0	cap
31	25			1	cap
32	26			0	cap
33	27			1	cap
34	28			0	cap
35	29			1	cap
36	30			0	cap
37	31			1	cap
38	32			0	cap
39	33	BRK		BREAK	BREAK

Before CTIM, 18 capture cycles is not divisible by 8, 18 modulo 8 is 2, as 18 is divided by 8, the remainder is 2, So system will generate 6 (8 minus 2) dead cycles.

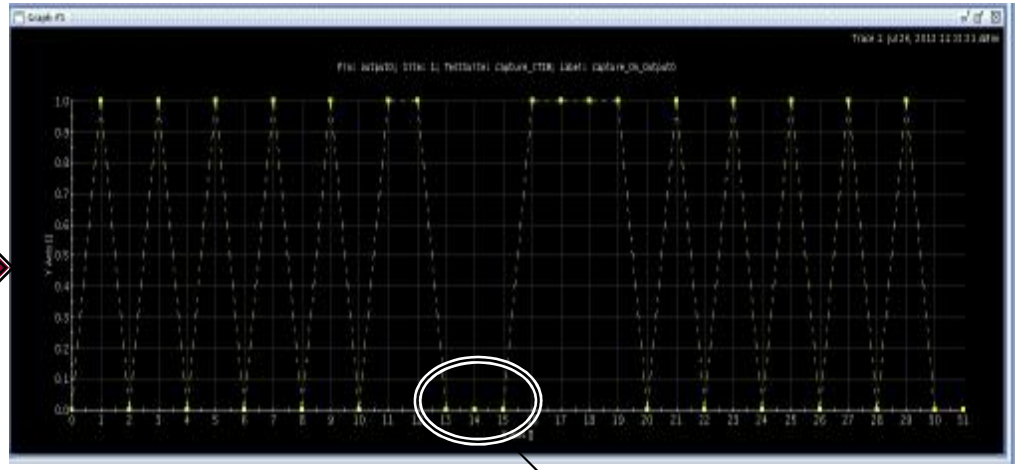
The break cycles are what cause the capturing of the unwanted bits?

Note: the number of user cycles before the CTIM instruction is not exactly divisible by 8, up to seven logged break cycles are generated. The break cycles are inserted immediately after the last user cycle that was generated with the old timing

Effect of CTIM on Digital Capture

Is it true that the break cycles are what cause the capturing of the unwanted bits?

Signal (Layout: new1)				input0 (DVC)	output0 (DVC)
X-Mode Area					
Protocol					
Cycle#	Vector#	Instruction	Comment		
0	0	GENV 18		1	nocap
1	1			0	nocap
2	2			1	nocap
3	3			0	nocap
4	4			1	nocap
5	5			0	cap
6	6			1	cap
7	7			0	cap
8	8			1	cap
9	9			0	cap
10	10			1	cap
11	11			0	cap
12	12			1	cap
13	13			0	cap
14	14			1	cap
15	15			0	cap
16	16			1	cap
17	17			1	cap
18	18	CTIM 2		BREAK	BREAK
19	18			BREAK	BREAK
20	18			BREAK	BREAK
21	18			BREAK	BREAK
22	18			BREAK	BREAK
23	18			BREAK	BREAK
24	18	GENV 15		1	cap
25	19			1	cap
26	20			1	cap
27	21			1	cap
28	22			0	cap
29	23			1	cap
30	24			0	cap
31	25			1	cap
32	26			0	cap
33	27			1	cap
34	28			0	cap
35	29			1	cap
36	30			0	cap
37	31			1	cap
38	32			0	cap
39	33	BRK		BREAK	BREAK



3 dead cycles captured

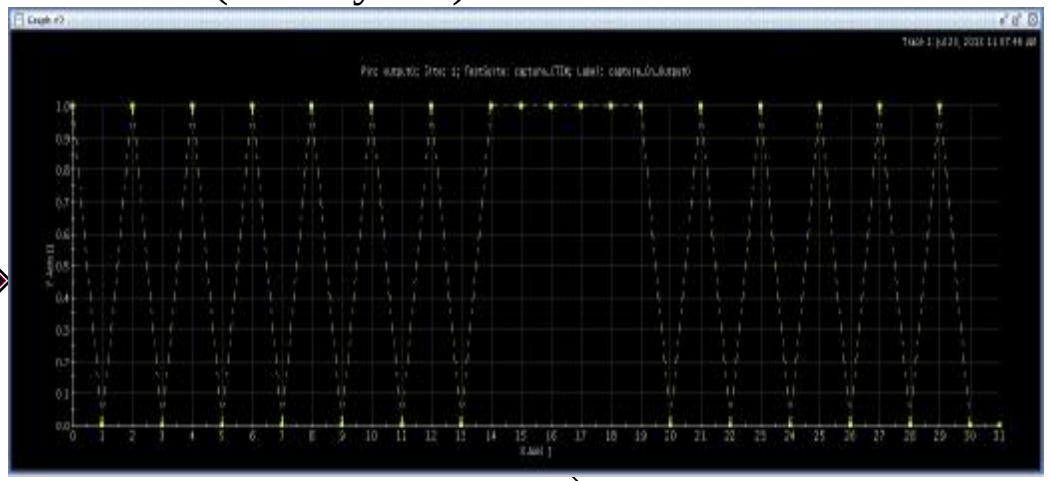
Before CTIM, now 13 capture cycles is not divisible by 8, 13 modulo 8 is 5, So system will generate 3 (8 minus 5) dead cycles.

The system still generate 6 break cycles, because the cycles executed before CTIM keeps the same 18 cycles.

Effect of CTIM on Digital Capture

What is the way to get rid of the unwanted bits (dead cycles)?

Signal (Layout: new1)				input0 (DVC)	output0 (DVC)
X-Mode Area					
Protocol					
Cycle#	Vector#	Instruction	Comment		
0	0	GENV 18		1	nocap
1	1			0	nocap
2	2			1	cap
3	3			0	cap
4	4			1	cap
5	5			0	cap
6	6			1	cap
7	7			0	cap
8	8			1	cap
9	9			0	cap
10	10			1	cap
11	11			0	cap
12	12			1	cap
13	13			0	cap
14	14			1	cap
15	15			0	cap
16	16			1	cap
17	17			1	cap
18	18	CTIM 2		BREAK	BREAK
19	18			BREAK	BREAK
20	18			BREAK	BREAK
21	18			BREAK	BREAK
22	18			BREAK	BREAK
23	18			BREAK	BREAK
24	18	GENV 15		1	cap
25	19			1	cap
26	20			1	cap
27	21			1	cap
28	22			0	cap
29	23			1	cap
30	24			0	cap
31	25			1	cap
32	26			0	cap
33	27			1	cap
34	28			0	cap
35	29			1	cap
36	30			0	cap
37	31			1	cap
38	32			0	cap
39	33	BRK		BREAK	BREAK



no dead cycles captured

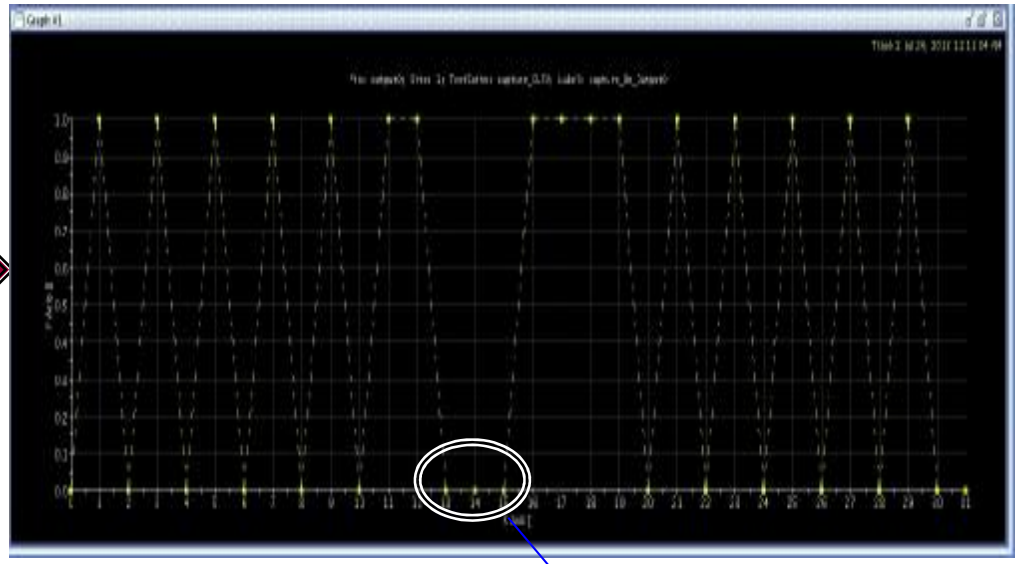
Before CTIM, now 16 capture cycles is divisible by 8, no dead cycles generated.

The system still generate 6 break cycles, but no dead cycles are observed on capture.

Effect of CLEV on Digital Capture

Sequencer instruction CLEV have the same effect on digital capture as CTIM do.

Signal (Layout: new1)			input0 (DVC)	output0 (DVC)
X-Mode Area				
Protocol				
Vector#	Instruction	Comment		
0			1	nocap
1			0	nocap
2			1	nocap
3			0	nocap
4			1	nocap
5			0	cap
6			1	cap
7			0	cap
8			1	cap
9			0	cap
10			1	cap
11			0	cap
12			1	cap
13			0	cap
14			1	cap
15			0	cap
16			1	cap
17			1	cap
	CLEV 2			
18			1	cap
19			1	cap
20			1	cap
21			1	cap
22			0	cap
23			1	cap
24			0	cap
25			1	cap
26			0	cap
27			1	cap
28			0	cap
29			1	cap
30			0	cap
31			1	cap
32			0	cap
	STOP			



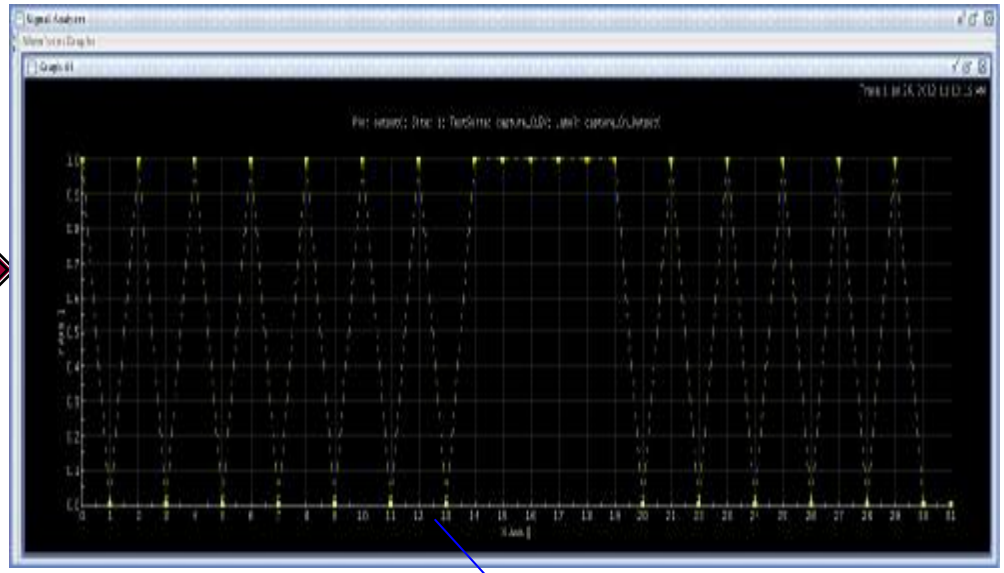
3 dead cycles captured

Before CLEV, 13 capture cycles is not divisible by 8, 13 modulo 8 is 5, So system will generate 3 (8 minus 5) dead cycles.

Effect of CLEV on Digital Capture

In order to get rid of dead cycles, make capture cycles before CLEV is divisible by 8.

Signal (Layout: new1)			input0 (DVC)	output0 (DVC)
X-Mode Area				
Protocol				
Vector#	Instruction	Comment		
0			1	nocap
1			0	nocap
2			1	cap
3			0	cap
4			1	cap
5			0	cap
6			1	cap
7			0	cap
8			1	cap
9			0	cap
10			1	cap
11			0	cap
12			1	cap
13			0	cap
14			1	cap
15			0	cap
16			1	cap
17			1	cap
	CLEV 2			
18			1	cap
19			1	cap
20			1	cap
21			1	cap
22			0	cap
23			1	cap
24			0	cap
25			1	cap
26			0	cap
27			1	cap
28			0	cap
29			1	cap
30			0	cap
31			1	cap
32			0	cap
	STOP			



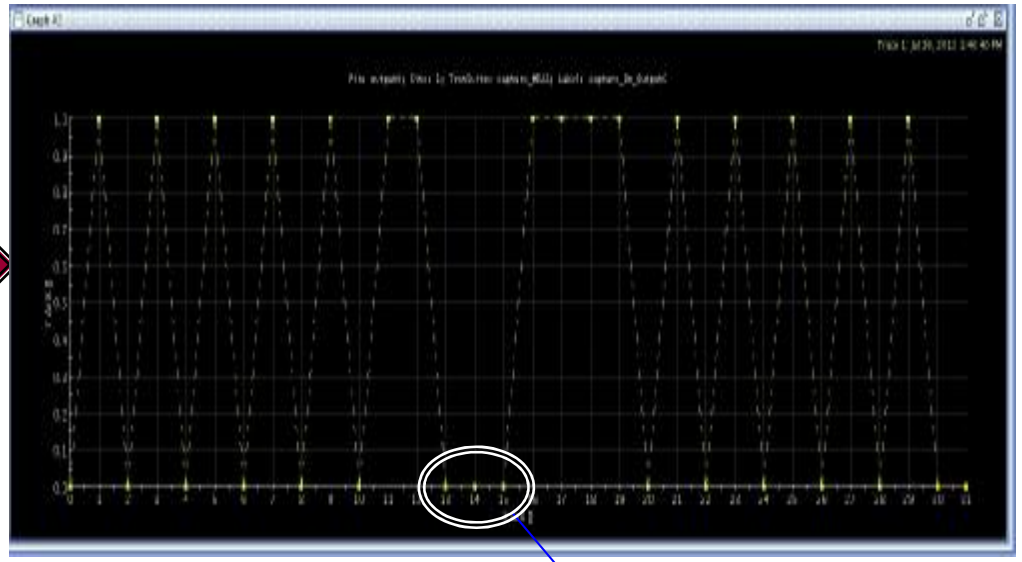
no dead cycles captured

Before CLEV, 16 capture cycles is divisible by 8, no dead cycles generated.

Effect of MEAS on Digital Capture

Another sequencer instruction MEAS have the same effect on digital capture.

Signal (Layout: new1)			input0 (DVC)	output0 (DVC)
X-Mode Area				
Protocol				
Vector#	Instruction	Comment		
0			1	nocap
1			0	nocap
2			1	nocap
3			0	nocap
4			1	nocap
5			0	cap
6			1	cap
7			0	cap
8			1	cap
9			0	cap
10			1	cap
11			0	cap
12			1	cap
13			0	cap
14			1	cap
15			0	cap
16			1	cap
17			1	cap
	MEAS 1 1			
18			1	cap
19			1	cap
20			1	cap
21			1	cap
22			0	cap
23			1	cap
24			0	cap
25			1	cap
26			0	cap
27			1	cap
28			0	cap
29			1	cap
30			0	cap
31			1	cap
32			0	cap
	STOP			



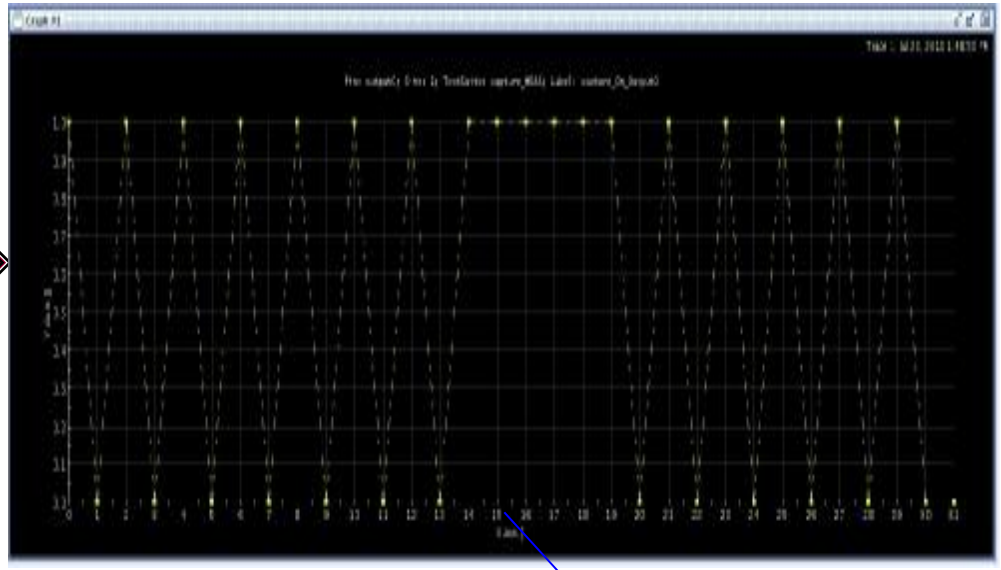
3 dead cycles captured

Before MEAS, 13 capture cycles is not divisible by 8, 13 modulo 8 is 5, So system will generate 3 (8 minus 5) dead cycles.

Effect of MEAS on Digital Capture

Do the same, make capture cycles before MEAS is divisible by 8.

Signal (Layout: new1)			input0 (DVC)	output0 (DVC)
X-Mode Area				
Protocol				
Vector#	Instruction	Comment		
0			1	nocap
1			0	nocap
2			1	cap
3			0	cap
4			1	cap
5			0	cap
6			1	cap
7			0	cap
8			1	cap
9			0	cap
10			1	cap
11			0	cap
12			1	cap
13			0	cap
14			1	cap
15			0	cap
16			1	cap
17			1	cap
	MEAS 1 1			
18			1	cap
19			1	cap
20			1	cap
21			1	cap
22			0	cap
23			1	cap
24			0	cap
25			1	cap
26			0	cap
27			1	cap
28			0	cap
29			1	cap
30			0	cap
31			1	cap
32			0	cap
	STOP			



no dead cycles captured

Before MEAS, 16 capture cycles is divisible by 8, no dead cycles generated.

Solutions and work around

In order to get rid of the unwanted bits, a few options are available:

1. If there is a section of the pattern before the CTIM/CLEV/MEAS instruction that can be looped without affecting the outcome of the test, then repeat/loop can be added to capture cycles that will make the location of the CTIM/CLEV/MEAS a modulo 8 boundary.

2. If the outcome will not be affected, move the CTIM/CLEV/MEAS a few cycles up or down to a modulo 8 boundary.

3. If totally unavoidable, collect the data with the dead cycles then in software after uploading. This requires the knowledge of exactly where the CTIM/CLEV/MEAS is and then removing the next (8 - remainder of capture cycles/8).

Note : A point to note is that in order to accommodate for the CTIM/CLEV/MEAS, if it is not at a modulo 8 boundary, the VV has to be increased by the number of expected dead cycles. Therefore, as an example, if there is an intention to capture 256 cycles and there is a CTIM/CLEV/MEAS in the pattern that leads to 4 dead cycles, the VV should be made of size 260 to be able to capture the extra dead cycles as well as the real data.

Digital Capture in a burst

From SMT 7.1.3 and up, it's possible to set up digital capture on a burst pattern with multiple main patterns that digital capture is done in them.

Signal	digital_capture_burst (Instructions)
Call#	
0	CALL capture_variable_define
1	CALL digital_capture_label
2	CALL digital_capture_label0
3	CALL digital_capture_label
4	CALL digital_capture_label0
5	CALL digital_capture_label
6	CALL digital_capture_label0
7	CALL digital_capture_label
8	CALL digital_capture_label0
9	BEND

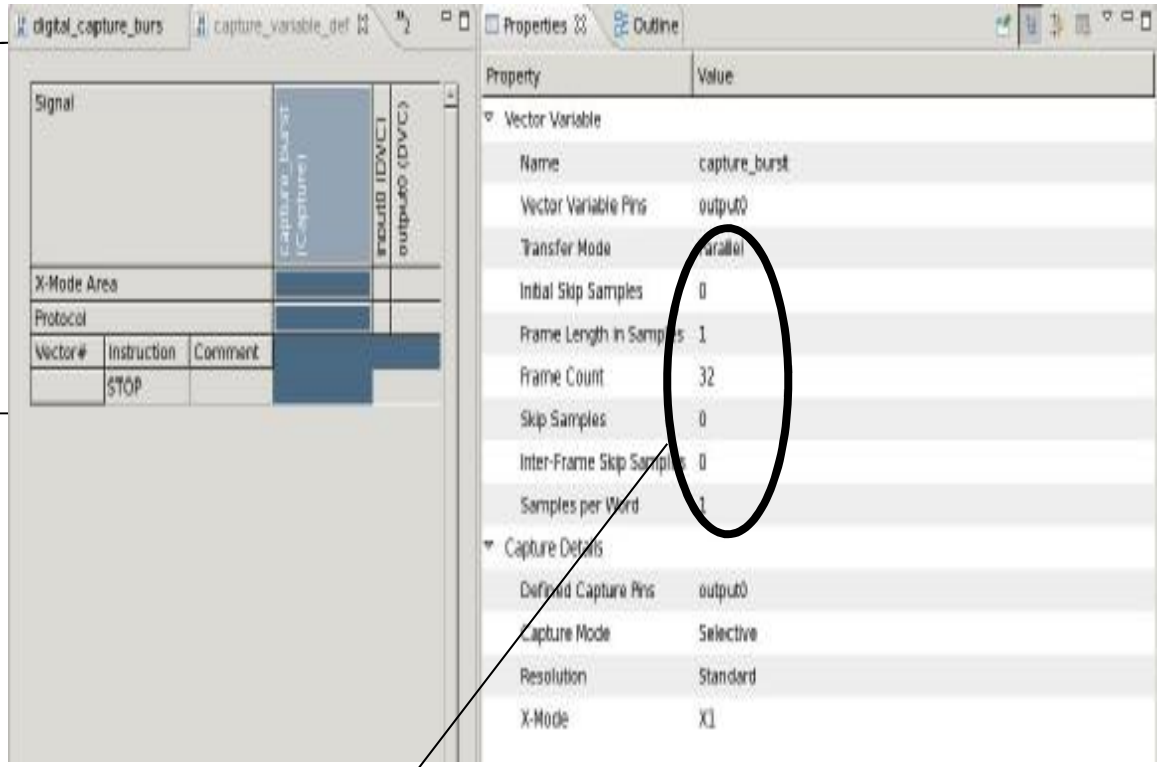
Define the Vector Variable to accommodate for all the digital captures in main patterns.

Digital capture was done in each main patterns.

Digital Capture in a burst

To define capture vector variables in the 1st label of the burst.

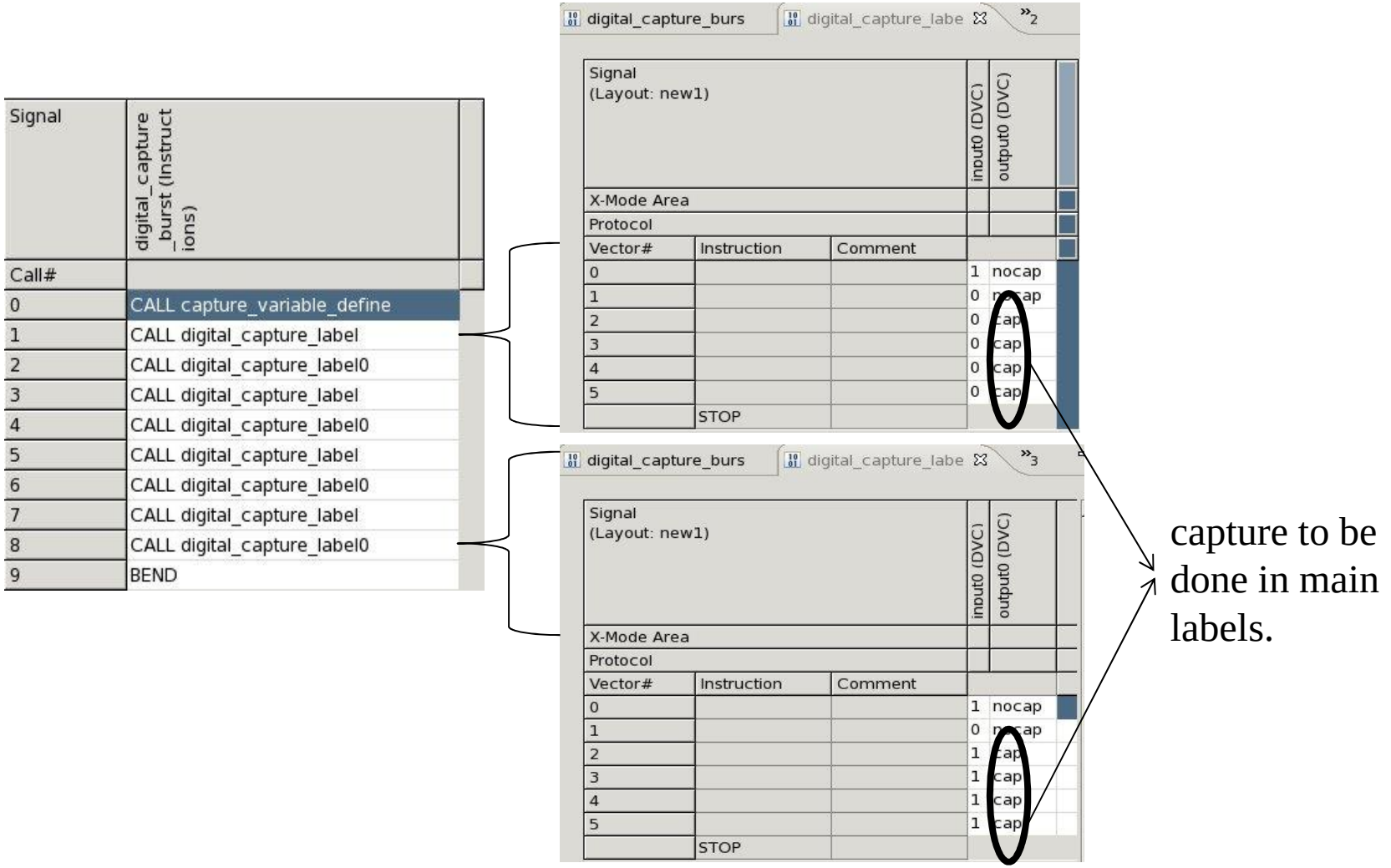
Signal	digital_capture_burst (Instructions)
Call#	
0	CALL capture_variable_define
1	CALL digital_capture_label
2	CALL digital_capture_label0
3	CALL digital_capture_label
4	CALL digital_capture_label0
5	CALL digital_capture_label
6	CALL digital_capture_label0
7	CALL digital_capture_label
8	CALL digital_capture_label0
9	BEND



Declare the number of capture points in following main labels – digital_capture_label & digital_capture_label0.

Digital Capture in a burst

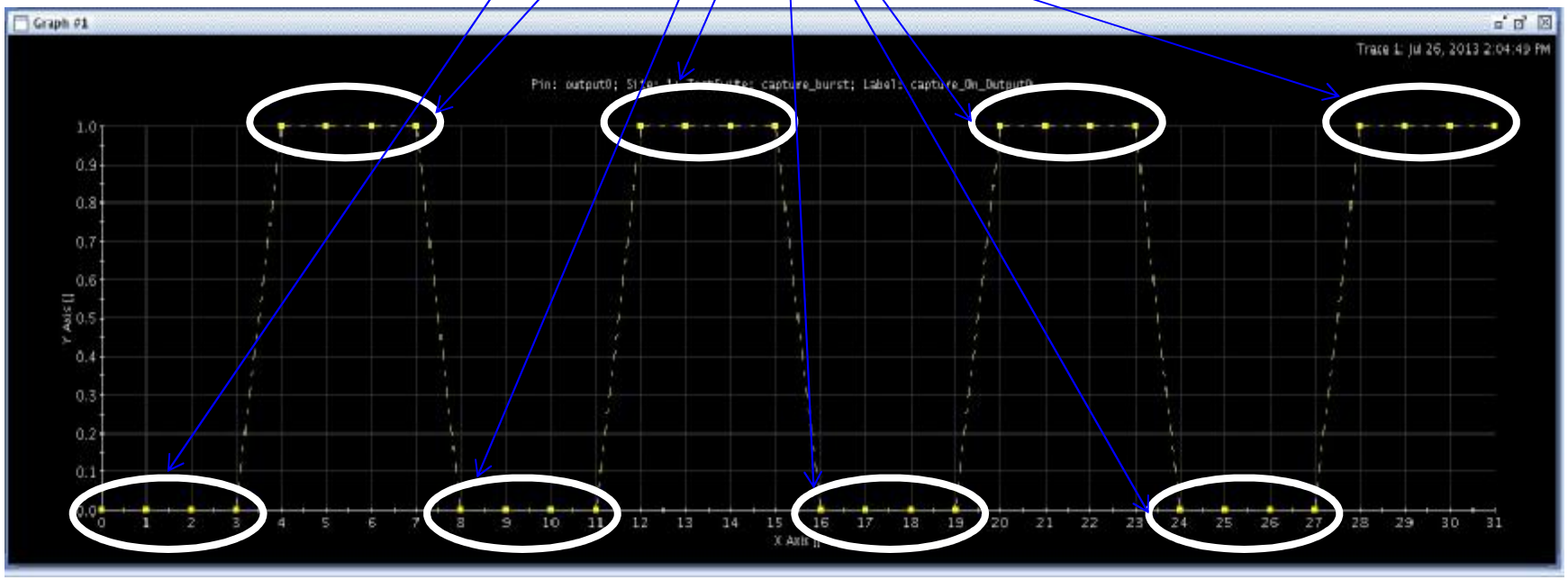
Digital capture to be implemented in following main labels in burst.



Digital Capture in a burst

With above setup, the following output is obtained:

Signal	digital_capture_burst (Instructions)
Call#	
0	CALL capture_variable_define
1	CALL digital_capture_label
2	CALL digital_capture_label0
3	CALL digital_capture_label
4	CALL digital_capture_label0
5	CALL digital_capture_label
6	CALL digital_capture_label0
7	CALL digital_capture_label
8	CALL digital_capture_label0
9	BEND



Summary of DigCap in a burst

1. A group of digital capture patterns (a group of main patterns) can be integrated into a burst.

2. Digital capture patterns type must be *Main.*

3. Need to define vector variable from the first called *Main* patterns in the burst and as a replacement of original vector variable definition in each digital capture patterns.

4. This new vector variable is the vector variable combination of all the digital capture patterns called in burst.

5. Make sure that each digital capture patterns does not generate more capture data than what was being described by the vector variable.

THANK YOU!