

PSRF Application Skill Development Project Report

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Participant	– Stephen Fu



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Outlines

❑ Background

- ◆ Project Introduction
- ◆ Project Schedule
- ◆ Pre-Requisites

❑ Test Program Development & Debugging

- ◆ Test Flow and Bin Summary
- ◆ Modulator (Baseband to RF) Test
- ◆ Datalog and Waveform Analysis for Modulator
- ◆ Demodulator (RF to Baseband) Test
- ◆ Datalog and Waveform Analysis for Demodulator

❑ Summary

Background

Project Introduction

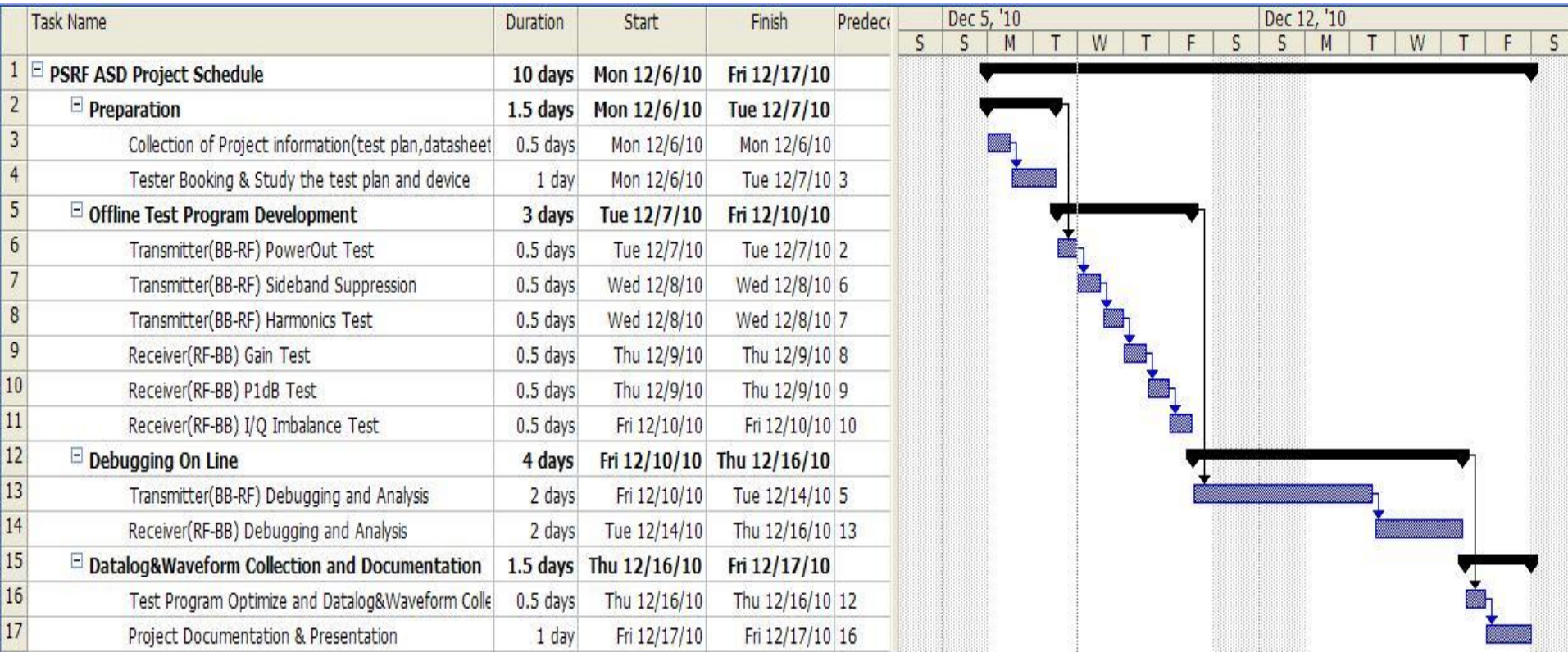
The purpose of this project is to further enhance AE's PSRF debugging and programming skill after attended the one week standard PSRF training. Treat this as customer project, AE will gain true learning RF project experience.

AE will also gain RF device knowledge after completing the project.

Background

Project Schedule

This project is planned to be finished within 2 weeks, schedule is created for project tracing.



Background

Pre-Requisites

Software

SmarTest version 6.5.2

RedHat Linux System

Hardware

Pin Scale V93000 tester platform, Port Scale RF with 12 ports and 2 Source cards and Analog module S/M in position 231.

RedHat workstation

Universal RF Loadboard Rev4

Modulator (MiniCircuits ZAMIQ-895M) & Demodulator (MiniCircuits ZAMIQ-895D)

4 pcs of pin->SMA and 4 pcs of SMA->SMA

Personnel/Manpower

Man-hours required:

$$8 * 10 = 80 \text{ (hours)}$$

Prerequisite knowledge/skill:

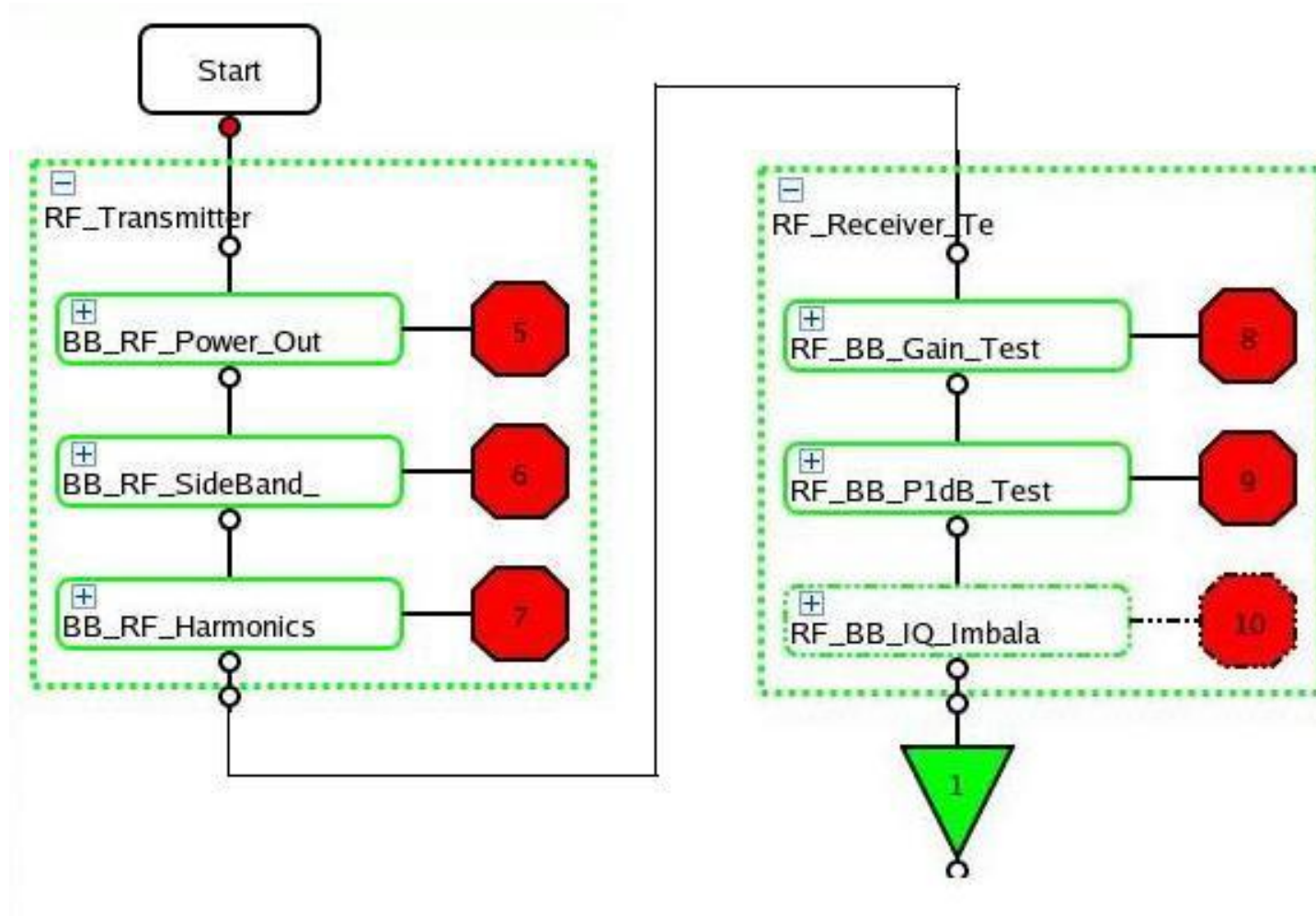
V93000 SOC Basic, Mix-Signal & PSRF Training

RF Fundamental Training or equivalent training

Knowledge of RF device testing concepts.

Test Program Development & Debugging

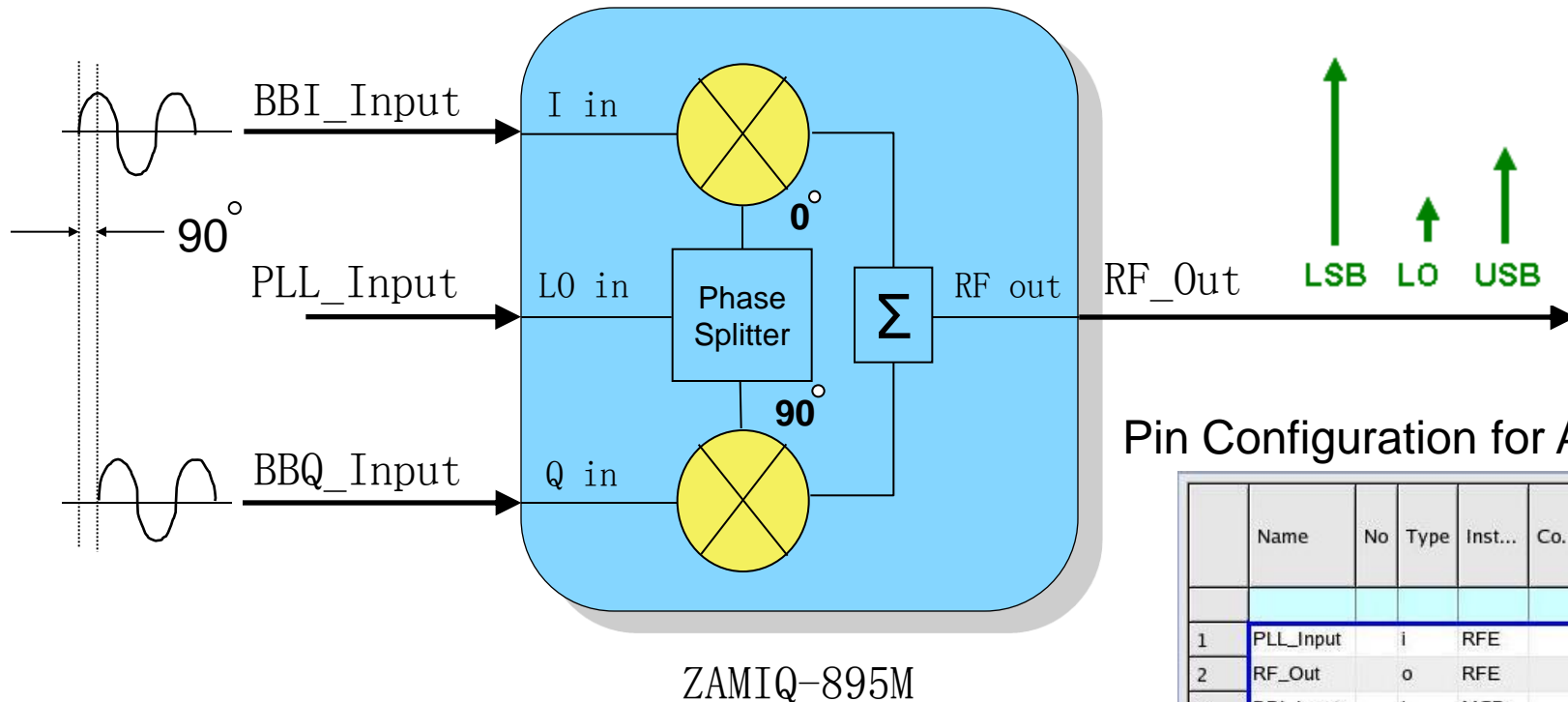
Test Flow and Bin Summary



Test Program Development & Debugging

Modulator (Baseband to RF) Test

Device Connections & Pin Names



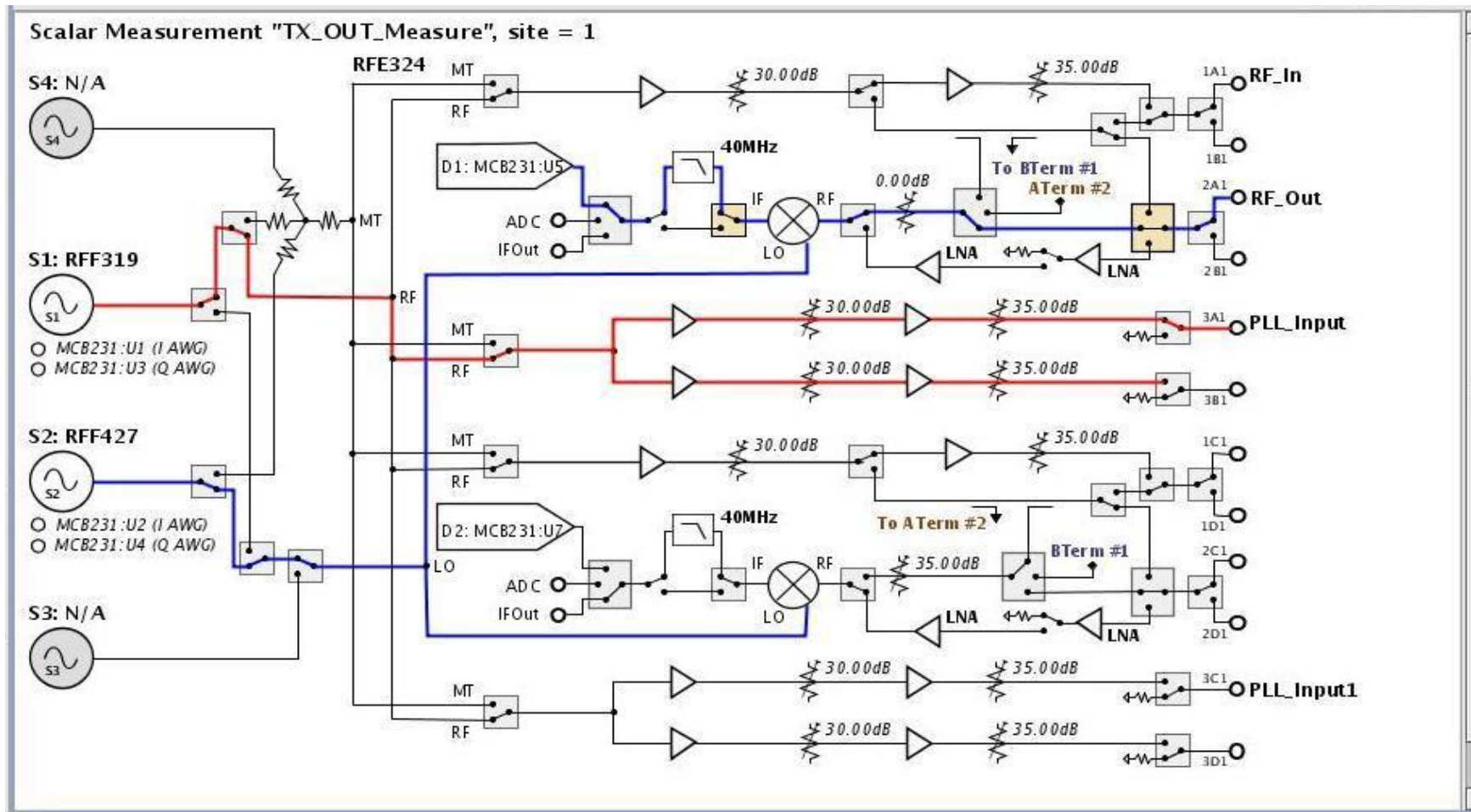
Pin Configuration for AWG access

	Name	No	Type	Inst...	Co...	Tester Channel	
						Site 1	
						Pogo	Pad
1	PLL_Input	i	RFE		324		3A1
2	RF_Out	o	RFE		324		2A1
3	BBI_Input	i	MCB		23116		S2
4	BBQ_Input	i	MCB		23112		S2
5	RF_In	i	RFE		324		1A1
6	BBI_Out	o	MCB		23116		S1
7	BBQ_Out	o	MCB		23112		S1
8	PLL_Input1	i	RFE		324		3C1

Test Program Development & Debugging

Modulator (Baseband to RF) Test

RF Port Block Diagram



Test Program Development & Debugging

Modulator (Baseband to RF) Test

Create the Frequency List for Power Out/Unwanted Sideband Suppression/
Harmonics Tests.

TX_OUT_Measure				
Data Definitions				
Name	Type	Description	Equation Definition	Evaluation Result
Carrier_Freq	Double Constant		880e6	880e6
Lower_Sideband	Double Constant		Carrier_Freq-Offset_Freq	877.8125e6
Lower_Sideband1	Double Constant		Carrier_Freq-Offset_Freq1	879.9e6
Lower_Sideband2	Double Constant		Carrier_Freq-Offset_Freq2	878e6
Offset_Freq	Double Constant		2.1875e6	2.1875e6
Offset_Freq1	Double Constant		0.1e6	100e3
Offset_Freq2	Double Constant		2e6	2e6
Offset_Freq3	Double Constant		3e6	3e6
RX_Test_Freq	Double Constant		Carrier_Freq+Offset_Freq3	883e6
Second_Harmonic	Double Constant		2*Lower_Sideband2	1.756e9
Upper_Sideband	Double Constant		Carrier_Freq+Offset_Freq	882.1875e6
Upper_Sideband1	Double Constant		Carrier_Freq+Offset_Freq1	880.1e6
Power_Sweep	Power List		step(-20,10,2)	-20 -18 -16 -14 -12 -10 -8 -6 -4 -2 0 2 4 6 8 10
RX_Stim_Freq	Frequency List		RX_Test_Freq	883e6
Ref_Clock_Freq	Frequency List		Carrier_Freq	880e6
TX_CS_SS	Frequency List		Lower_Sideband Carrier_Freq Upper_Sideband	877.8125e6 880e6 882.1875e6
TX_CS_SS1	Frequency List		Lower_Sideband1 Carrier_Freq Upper_Sideband1	879.9e6 880e6 880.1e6
TX_CS_SS2	Frequency List		Lower_Sideband2 Second_Harmonic	878e6 1.756e9
PowerValue	Double Variable		-20	-20

Test Program Development & Debugging

Modulator (Baseband to RF) Test

Create Ref_Clock_Stim.

The screenshot displays the Verigy test program development interface. The top window, titled "Ref_Clock_Stim (Stimulus)", shows the configuration for a stimulus. It is divided into two main sections: "Stimulus Configuration" and "Resource Allocation".

Stimulus Configuration:

- Pin Name: PLL_Input
- Stimulus Type: CW
- Cal State: Off
- Multi-Pin Stimulus: FALSE
- Export To Analog Sets: (empty)

Resource Allocation:

- Used with Definition: (empty)
- Minimum Power (dBm): -20
- Maximum Power (dBm): -20
- Frequency List: Ref_Clock_Freq
- Stimulus MUX: Direct
- Stim Instrument: S1: RFF319

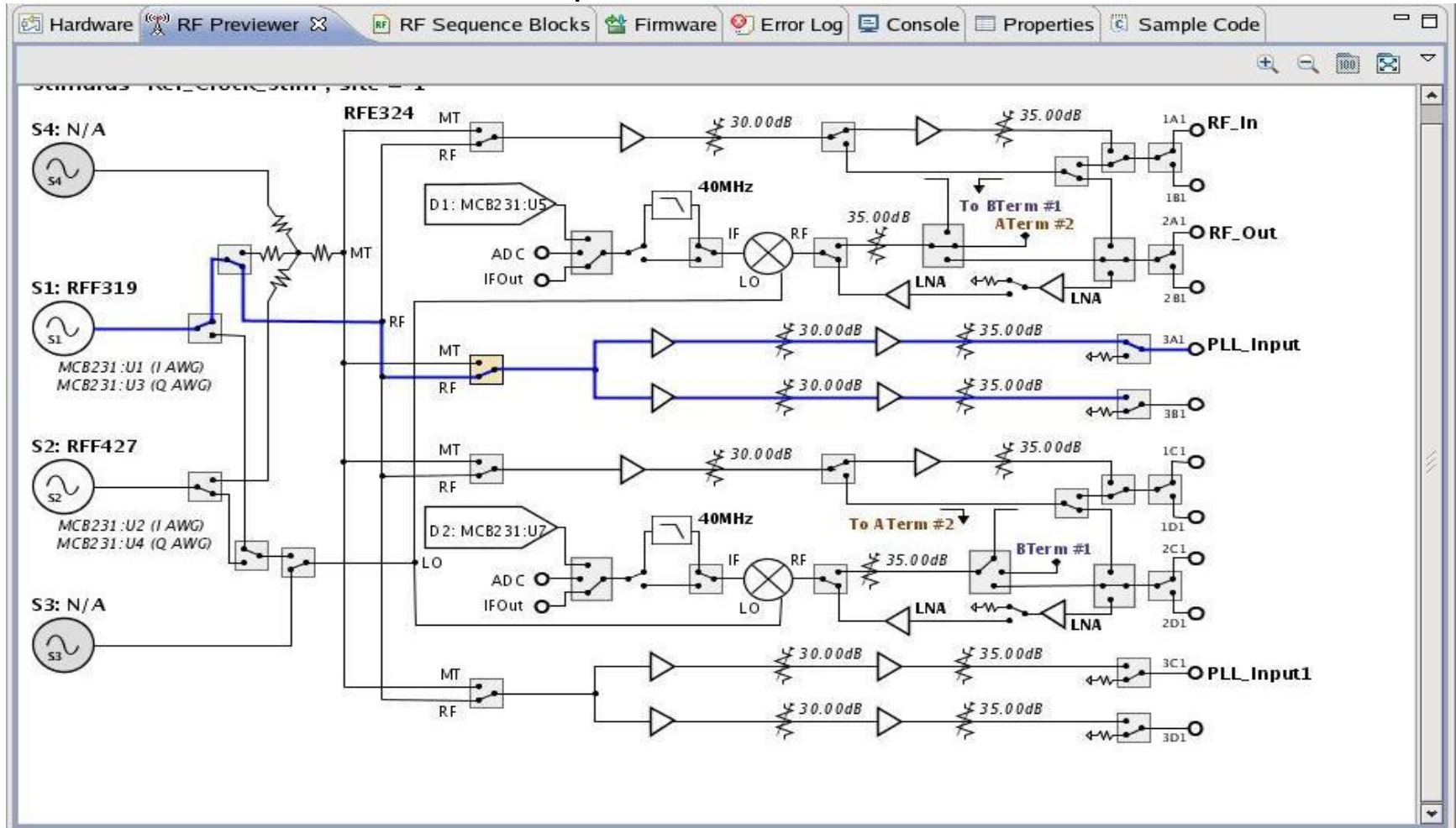
The bottom window, titled "Sequence Setting of 'Ref_Clock_Stim'", shows the functional block configuration. It contains a "Functional Block 1" which is a "Ref_Clock_Stim: Initial Settings" block. The settings for this block are:

- Comment: (empty)
- Stimulus State: On
- Frequency List Index: 0
- Output Power (dBm): -10

Test Program Development & Debugging

Modulator (Baseband to RF) Test

Ref_Clock_Stim Hardware Setup



Test Program Development & Debugging

Modulator (Baseband to RF) Test

Calculate F_s for AWG Waveform

Power Out Test: Baseband Signal $F_t = 2.1875\text{MHz}$

Number of Points $N = 512$

Frequency Bin $M = 7$

Sampling Frequency $F_s = 160\text{ MHz}$

Master Clock on the RF Measurement can be set to $F_s \cdot 3 = 480\text{MHz}$

Sideband Suppression Test: Baseband Signal $F_t = 100\text{KHz}$

Number of Points $N = 2048$

Frequency Bin $M = 5$

Sampling Frequency $F_s = 40.96\text{ MHz}$

Master Clock on the RF Measurement can be set to $F_s \cdot 10 = 409.6\text{MHz}$

Harmonics Test: Baseband Signal $F_t = 2\text{MHz}$

Number of Points $N = 256$

Frequency Bin $M = 5$

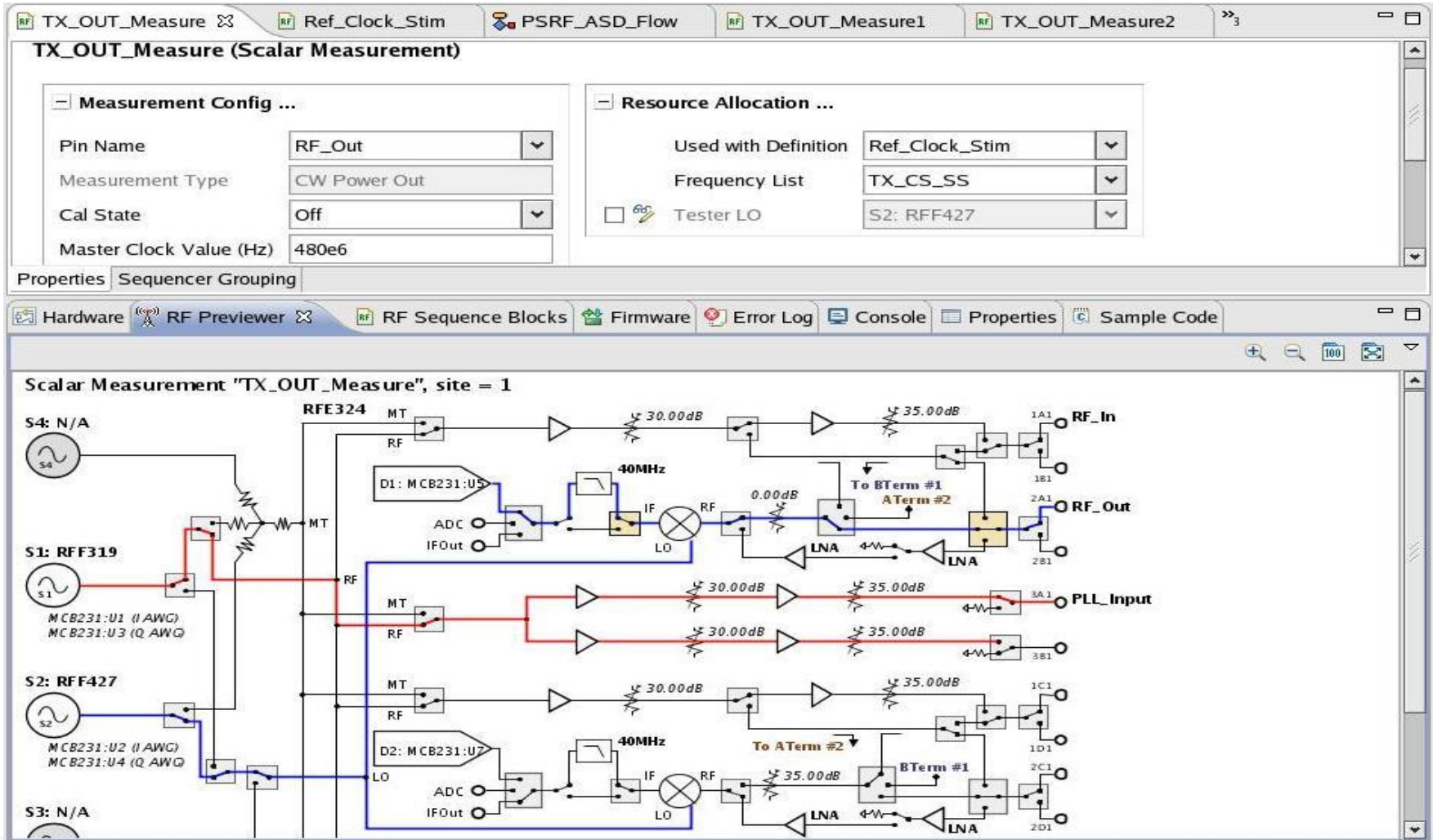
Sampling Frequency $F_s = 102.4\text{ MHz}$

Master Clock on the RF Measurement can be set to $F_s \cdot 4 = 409.6\text{MHz}$

Test Program Development & Debugging

Modulator (Baseband to RF) Test

Create the TX_OUT_Measure Meas Definition



Test Program Development & Debugging

Modulator (Baseband to RF) Test

Final RF Sequence Block View

Add RF measurement for different output frequency depending test Requirement, Change measurement Bandwidth accordingly and Change the Output power for Ref_Clock_Stim depending on the device specification.

The screenshot displays the 'RF Sequence Blocks' window in the Verigy test environment. The title bar includes tabs for Hardware, RF Previewer, RF Sequence Blocks, Firmware, Error Log, Console, Properties, and Sample Code. The main content area is titled 'Sequence Setting of "TX_OUT_Measure1"'. It contains three functional blocks connected sequentially by yellow squares:

- Functional Block 1: Ref_Clock_Stim: Initial Settings**
 - Comment: [Text Field]
 - Stimulus State: On (Dropdown)
 - Frequency List Index: 0 (Text Field)
 - Output Power (dBm): -10 (Text Field)
- Functional Block 2: TX_OUT_Measure1: Capture 1**
 - Comment: [Text Field]
 - Frequency List Index: 0 (Text Field)
 - Measurement Bandwidth (Hz): 50e3 (Text Field)
 - Number of Averages: 1 (Text Field)
 - Resource Allocation ... (Expandable Section)
 - Sampling Parameters ... (Expandable Section)
- Functional Block 3: TX_OUT_Measure1: Capture 2**
 - Comment: [Text Field]
 - Frequency List Index: 1 (Text Field, checked with a 60% icon)
 - Measurement Bandwidth (Hz): 50e3 (Text Field, unchecked with a 60% icon)
 - Number of Averages: 1 (Text Field, unchecked with a 60% icon)
 - Resource Allocation ... (Expandable Section)
 - Sampling Parameters ... (Expandable Section)

Test Program Development & Debugging

Modulator (Baseband to RF) Test

AWG Setups to TX_Out_Measure Analog Control Set

Analog Setup Tool

File Help

Analog Set Explorer Save Setup File Reset Config Snapshot

Setup Clock domain Setup Setup Focus: 0 Query Focus: 1

Clock Domain Setup

Analog clock source INT Append Set Name Set:TX_OUT_Measure Add

Timing Equation Set Waveform Set 1 Timing Set 1

Instrument MCB231_U1 Location CardCage 4 Slot 08 Change Delete

Clock Domain Analog Check domain Check All

Clock Value 480 MHz Clock Mode Fixed

Fs 160 MHz N 3

Rule Fixed Fs Value

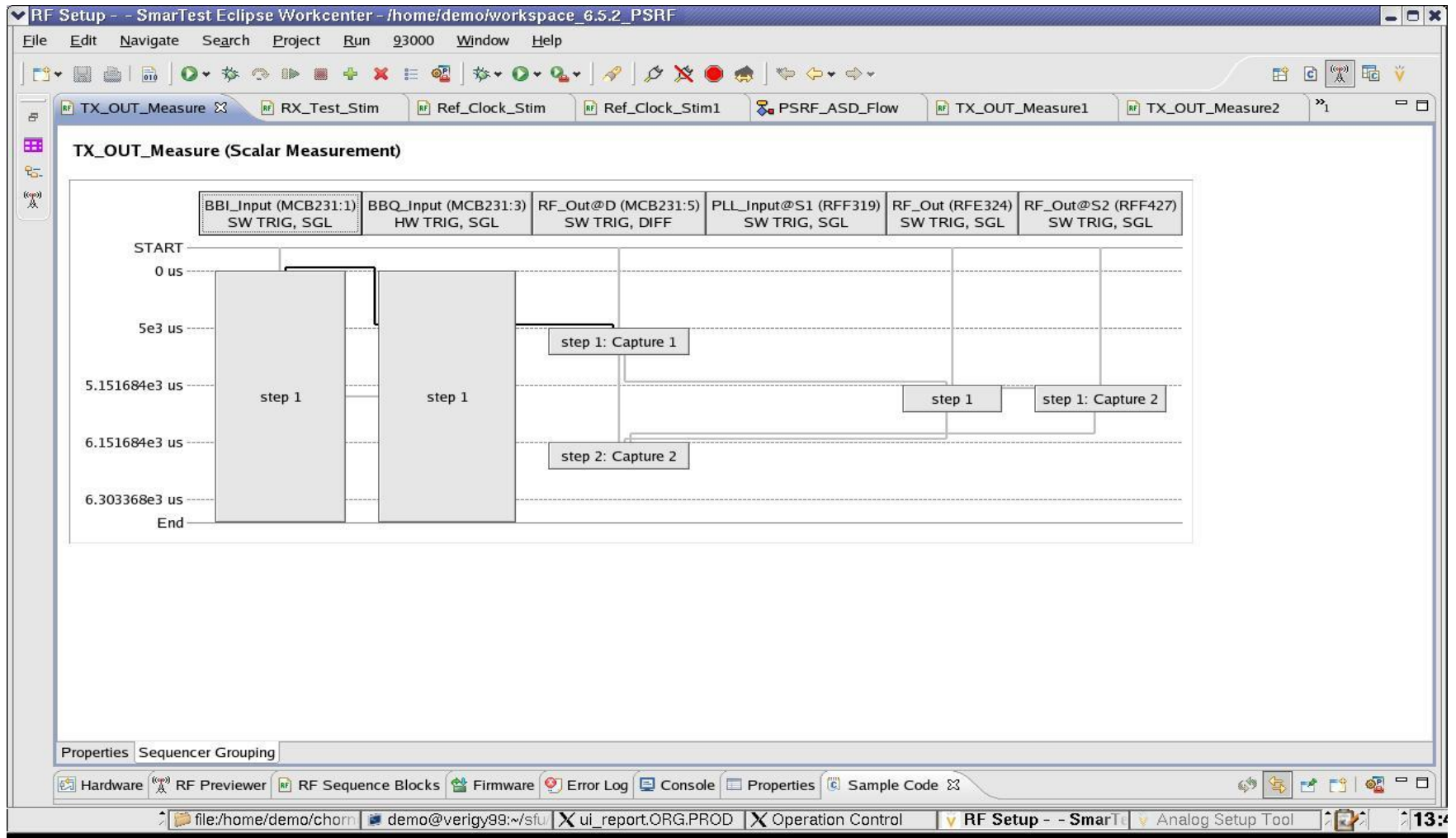
☒ Auto check

Instrument	Location	Clock Domain	Clock Mode	Clock Value	Fs	N	Rule	Actual Fs	Remark
MCB231_U1	CardCage 4 Slot 08	Analog	Fixed	480 MHz	160 MHz	3	Fixed Fs Value		200Msps IQ A...
MCB231_U3	CardCage 4 Slot 08	Analog	Fixed	480 MHz	160 MHz	3	Fixed Fs Value		200Msps IQ A...
MCB231_U5	CardCage 4 Slot 08	Analog	Fixed	480 MHz	2 MHz	240	Fixed N Value	96 MHz	RF DGT

Test Program Development & Debugging

Modulator (Baseband to RF) Test

Final Sequencer Grouping & Code for Test Method



Test Program Development & Debugging

Modulator (Baseband to RF) Test

Final Sequencer Grouping & Code for Test Method

```
DOUBLE Carrier_Suppression, Image_Rejection;
const STRING measName = "TX_OUT_Measure1";
ON_FIRST_INVOCATION_BEGIN();
    Analog.primary(measName);           //set the primary
    MEAS_DEF(measName).disableAll().connectAll(); // SW trigger the instruments in the Group and connect the pins
    EXECUTE_GROUP(measName);           //Then Execute the definition's "sequence group" in the 1st invocation
ON_FIRST_INVOCATION_END();
// Fetch the DSP parameters (and cal data) from the MEAS_DEF object.
ARRAY_D measParams = MEAS_DEF(measName).getParameters(1,0);
INT sizeOfOne = measParams.size();
INT numCaptures = 1;
MEAS_DEF(measName).get("NumCaptures", numCaptures);
ARRAY_D packedMeasParams(sizeOfOne*numCaptures);
DSP_EXTRACT(measParams, packedMeasParams, 0, 0, sizeOfOne);
for(INT capNum=1; capNum < numCaptures; capNum++)
{
    measParams = MEAS_DEF(measName).getParameters(capNum+1, 0);
    DSP_EXTRACT(measParams, packedMeasParams, 0, capNum*sizeOfOne, sizeOfOne);
}
// Run the DSP on the captured data by executing the static DSP function
// - the DSP_ROUTINES_BEGIN block cleanly handles multisite for you.
ARRAY_D measuredPowers(numCaptures);
DSP_ROUTINES_BEGIN();
    TX_OUT_Measure1Dsp(measName, packedMeasParams, measParams, measuredPowers);
DSP_ROUTINES_END();
// Print results to ui.Report window
cout << "*****Testsuite: BB_RF_SideBand_Suppression*****"<<endl;
for(INT capNum=0; capNum < numCaptures; capNum++)
cout << "\t Capture Num = " << capNum + 1<< ", Measured Power = " << measuredPowers[capNum]<<" dBm "<< endl;
Carrier_Suppression = measuredPowers[0] - measuredPowers[1];
Image_Rejection = measuredPowers[0] - measuredPowers[2];
cout << "\t Carrier_Suppression = " << Carrier_Suppression <<" dB "<< endl;
cout << "\t Image_Rejection = " << Image_Rejection <<" dB "<< endl;
TEST( "RF_Out", "Carrier_Suppression", Carrier_Suppression );
TEST( "RF_Out", "Image_Rejection", Image_Rejection );
// To prevent warnings and errors you should disconnect DGTs and AWGs that will no longer be in use.
ON_FIRST_INVOCATION_BEGIN();
    MEAS_DEF(measName).disconnectAll();
ON_FIRST_INVOCATION_END();
```

Test Program Development & Debugging

Datalog and Waveform Analysis for Modulator

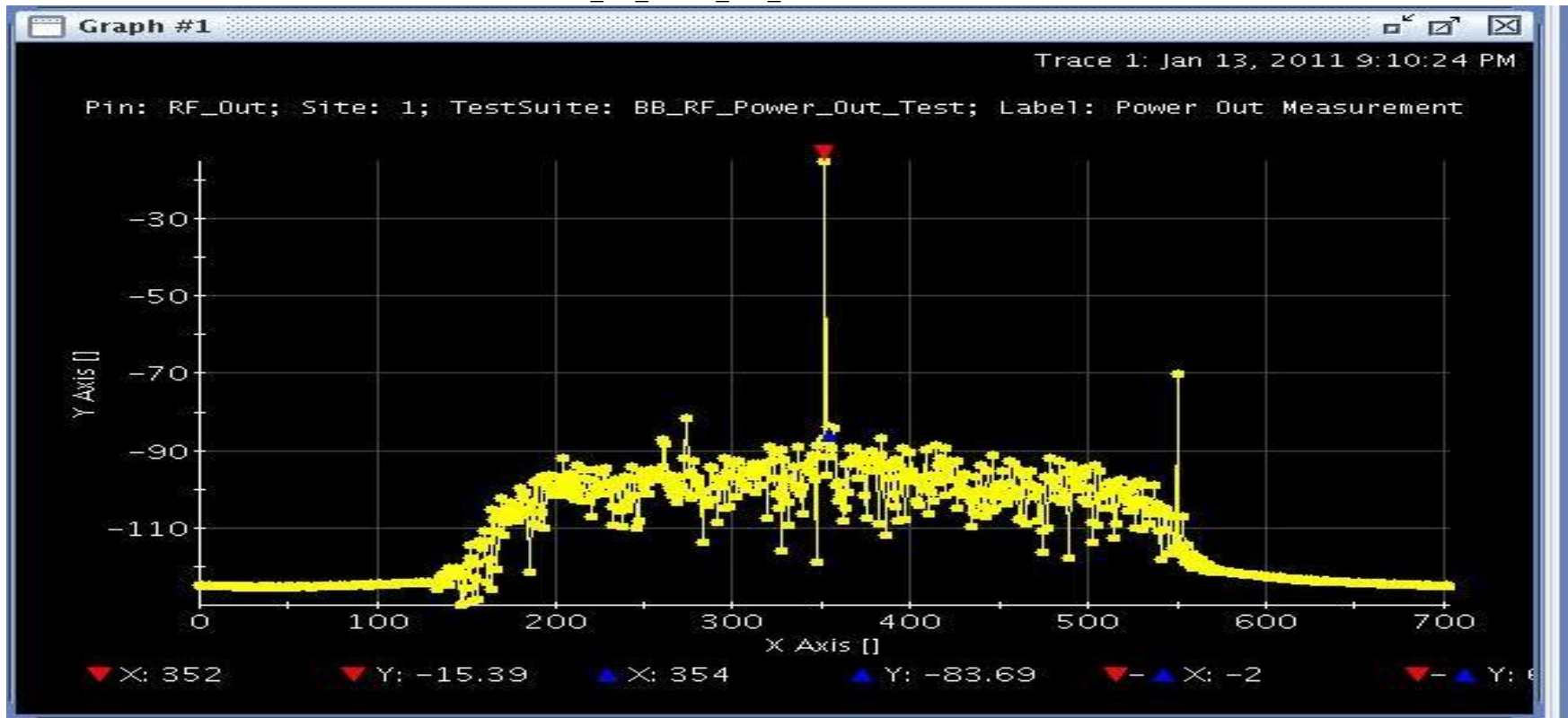
Datalog for Modulator



Datalog_for_BBtoR
F

Power Capture for Modulator

Testsuite: BB_RF_Power_Out_Test



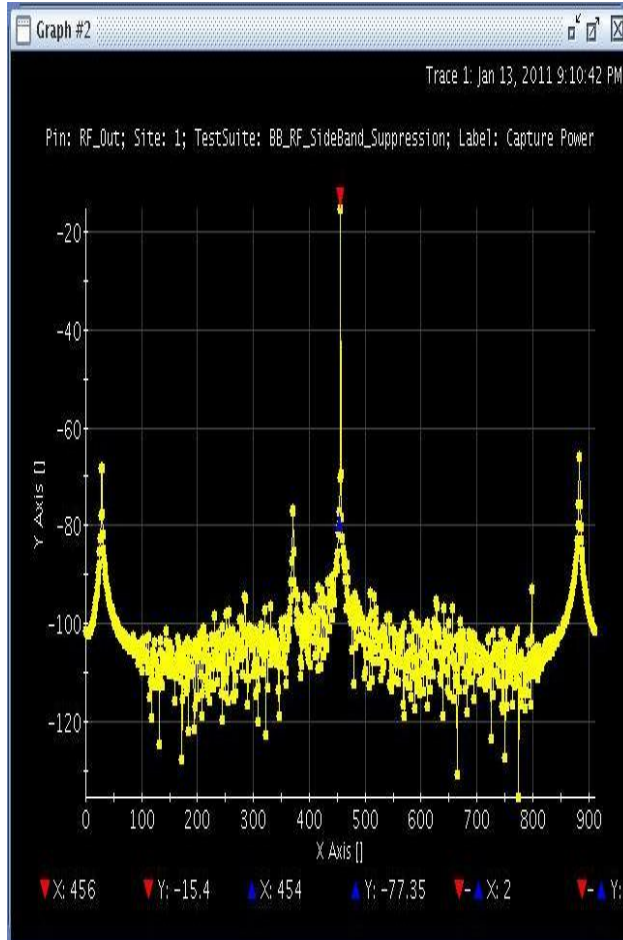
Measured Power : -30dBm < -15.386 dBm < 0dBm

Test Program Development & Debugging

Datalog and Waveform Analysis for Modulator

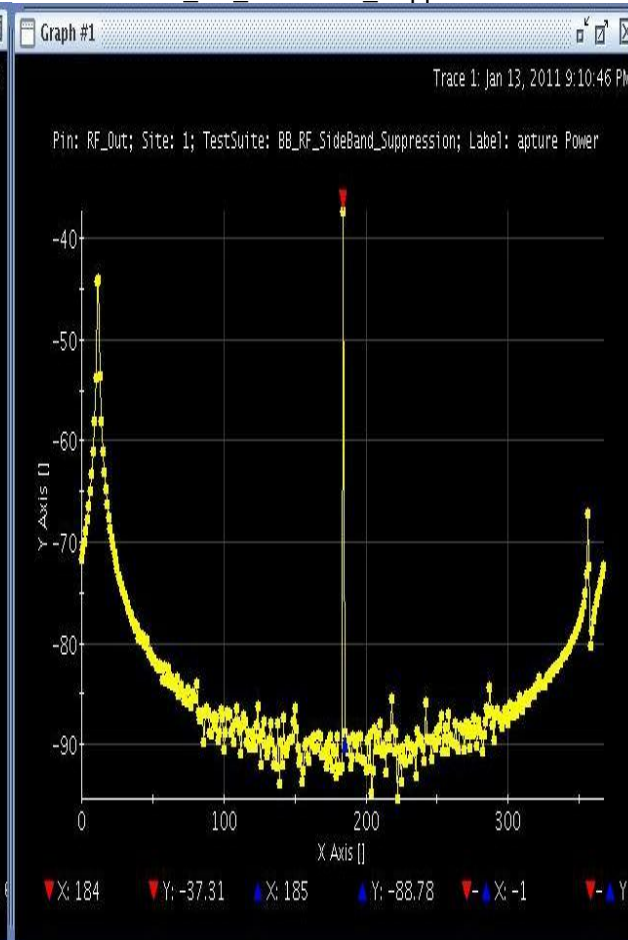
Power Capture for Modulator

Testsuite: BB_RF_SideBand_Suppression



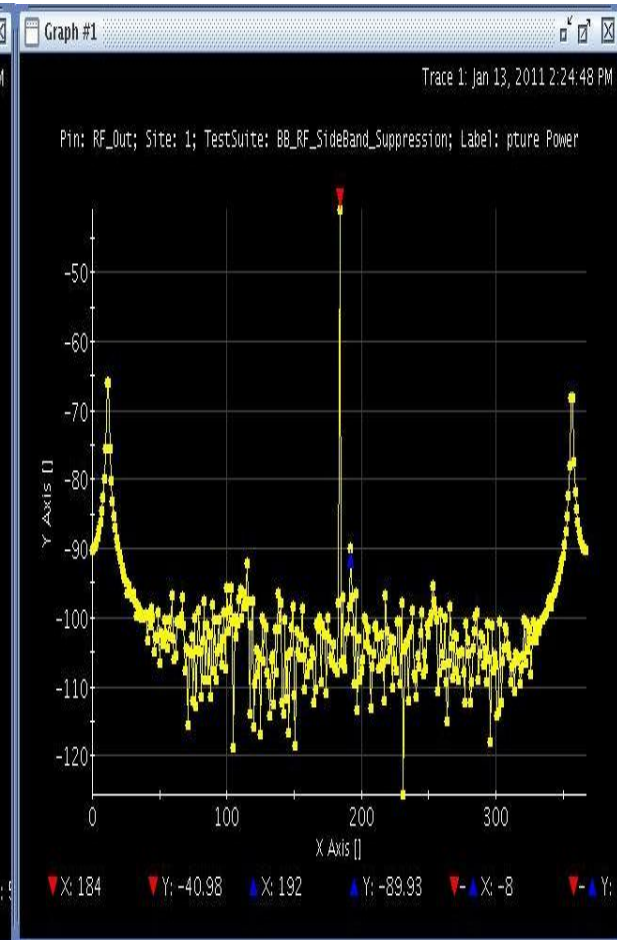
LSB = -15.396 dBm

Carrier_Suppression : 20dB < 21.8979 dB < 60dB



LO = -37.295 dBm

Image_Rejection : 20dB < 25.5781 dB < 60dB



USB = -40.975 dBm



10/11/2016
Verigy Fundamentals

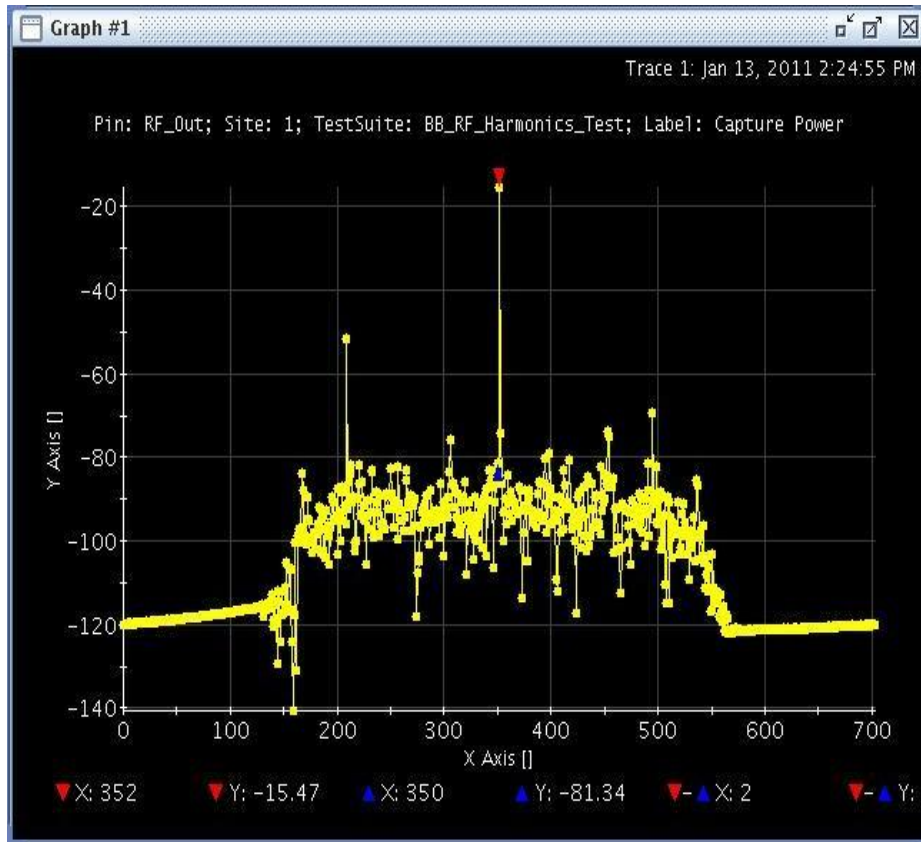
Verigy Restricted

Test Program Development & Debugging

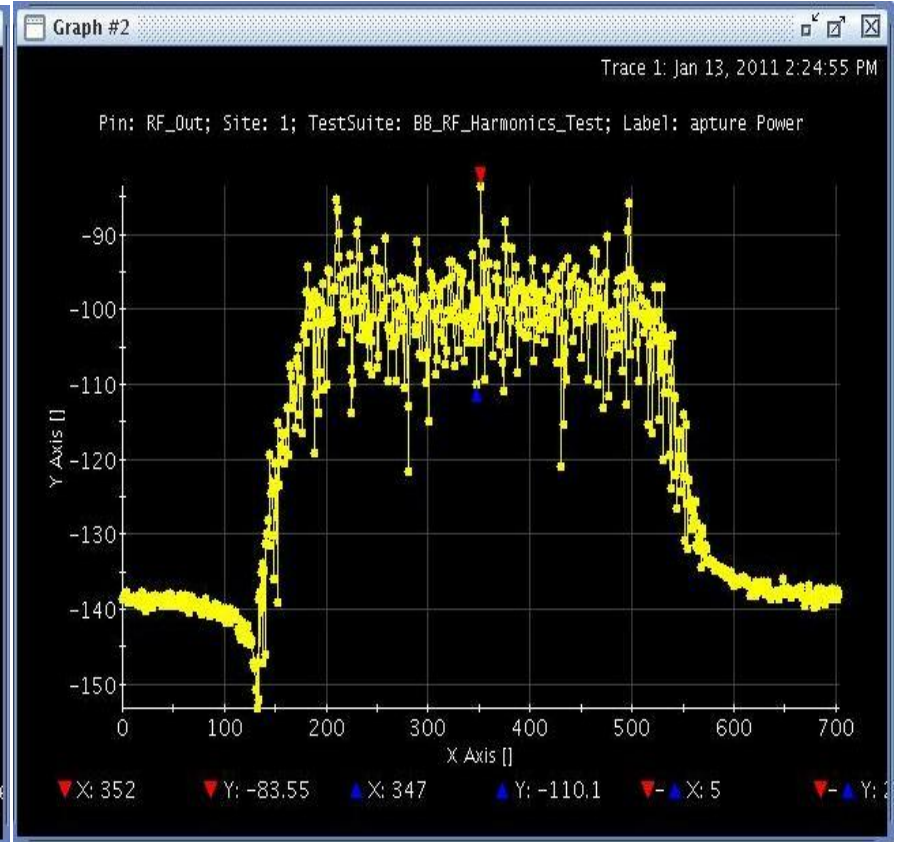
Datalog and Waveform Analysis for Modulator

Power Capture for Modulator

Testsuite: BB_RF_Harmonics_Test



Fundamental Signal Power = -15.4653 dBm



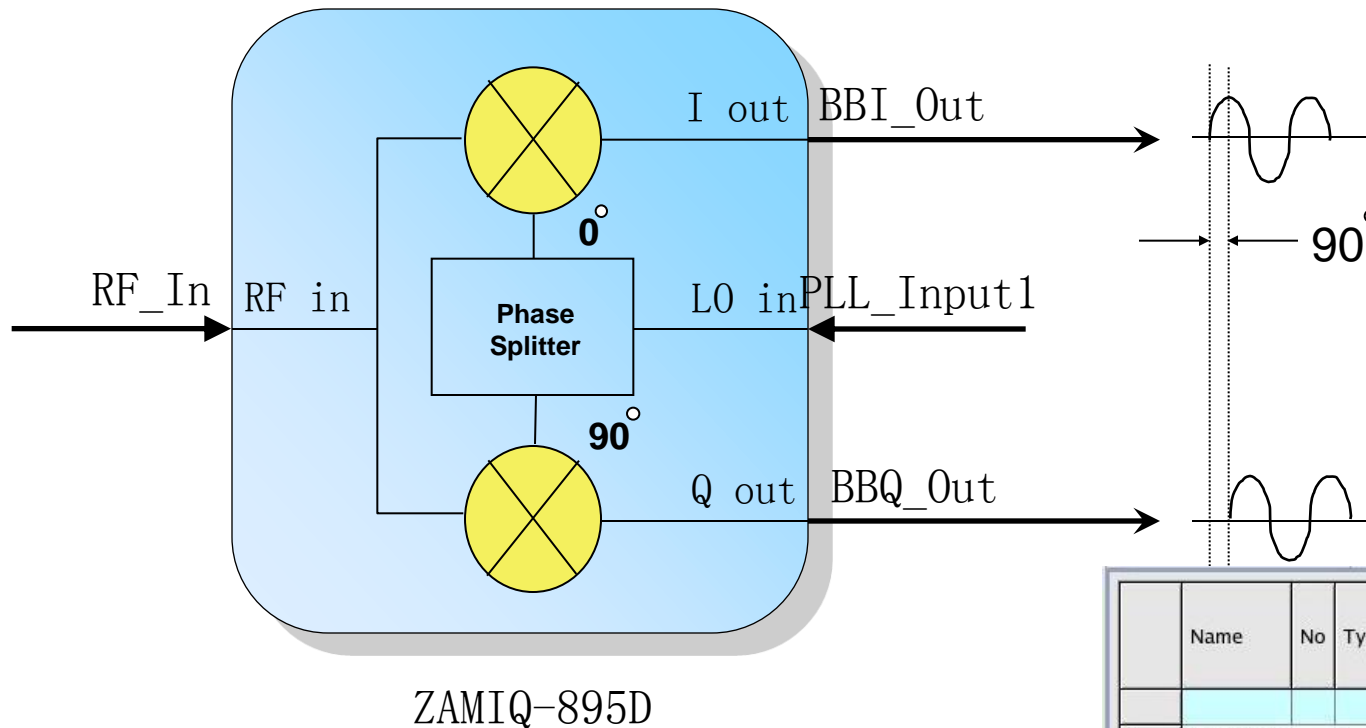
2nd Harmonics Power = -75.7937 dBm

2nd harmonics: 30 dB < 60.3283 dB

Test Program Development & Debugging

Demodulator (RF to Baseband) Test

Device Connections & Pin Names



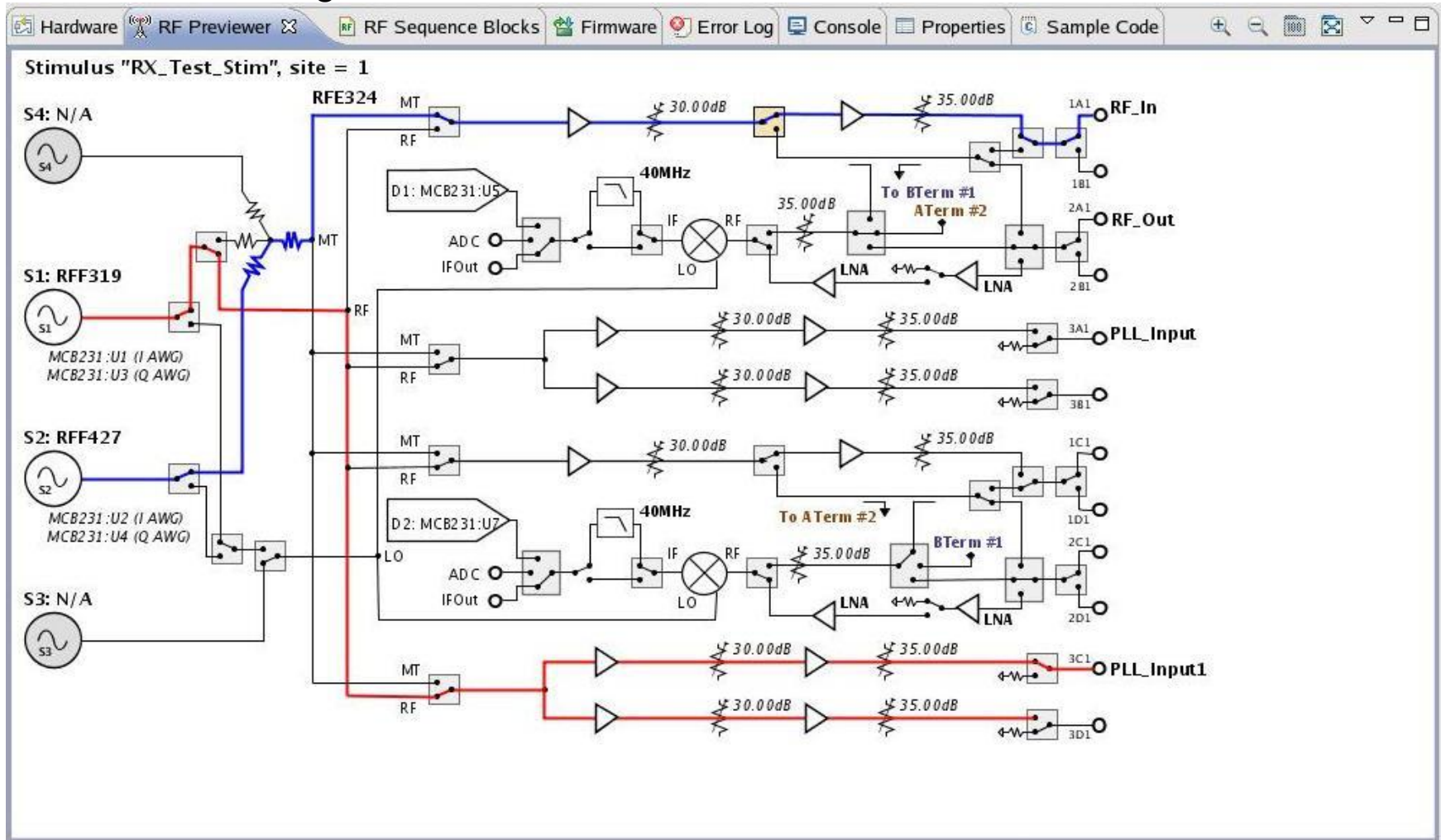
Pin Configuration for Digitizer access

	Name	No	Type	Inst...	Co...	Tester Channel	
						Site 1	
						Pogo	Pad
1	PLL_Input	i	RFE		324		3A1
2	RF_Out	o	RFE		324		2A1
3	BBI_Input	i	MCB		23116		S2
4	BBQ_Input	i	MCB		23112		S2
5	RF_In	i	RFE		324		1A1
6	BBI_Out	o	MCB		23116		S1
7	BBQ_Out	o	MCB		23112		S1
8	PLL_Input1	i	RFE		324		3C1

Test Program Development & Debugging

Demodulator (RF to Baseband) Test

RF Port Block Diagram



Test Program Development & Debugging

Demodulator (RF to Baseband) Test

Create Ref Clock Stim1.

The screenshot displays the Verigy test program development environment. The top window, titled 'Ref_Clock_Stim1 (Stimulus)', shows the configuration for a stimulus. It is divided into two main sections: 'Stimulus Configuration' and 'Resource Allocation'.

Stimulus Configuration:

- Pin Name: PLL_Input1
- Stimulus Type: CW
- Cal State: Off
- Multi-Pin Stimulus: FALSE
- Export To Analog Sets: (empty)
- RF Blanking: FALSE

Resource Allocation:

- Used with Definition: (empty)
- Minimum Power (dBm): -20
- Maximum Power (dBm): -20
- Frequency List: Ref_Clock_Freq
- Stimulus MUX: Direct
- Stim Instrument: S1: RFF319

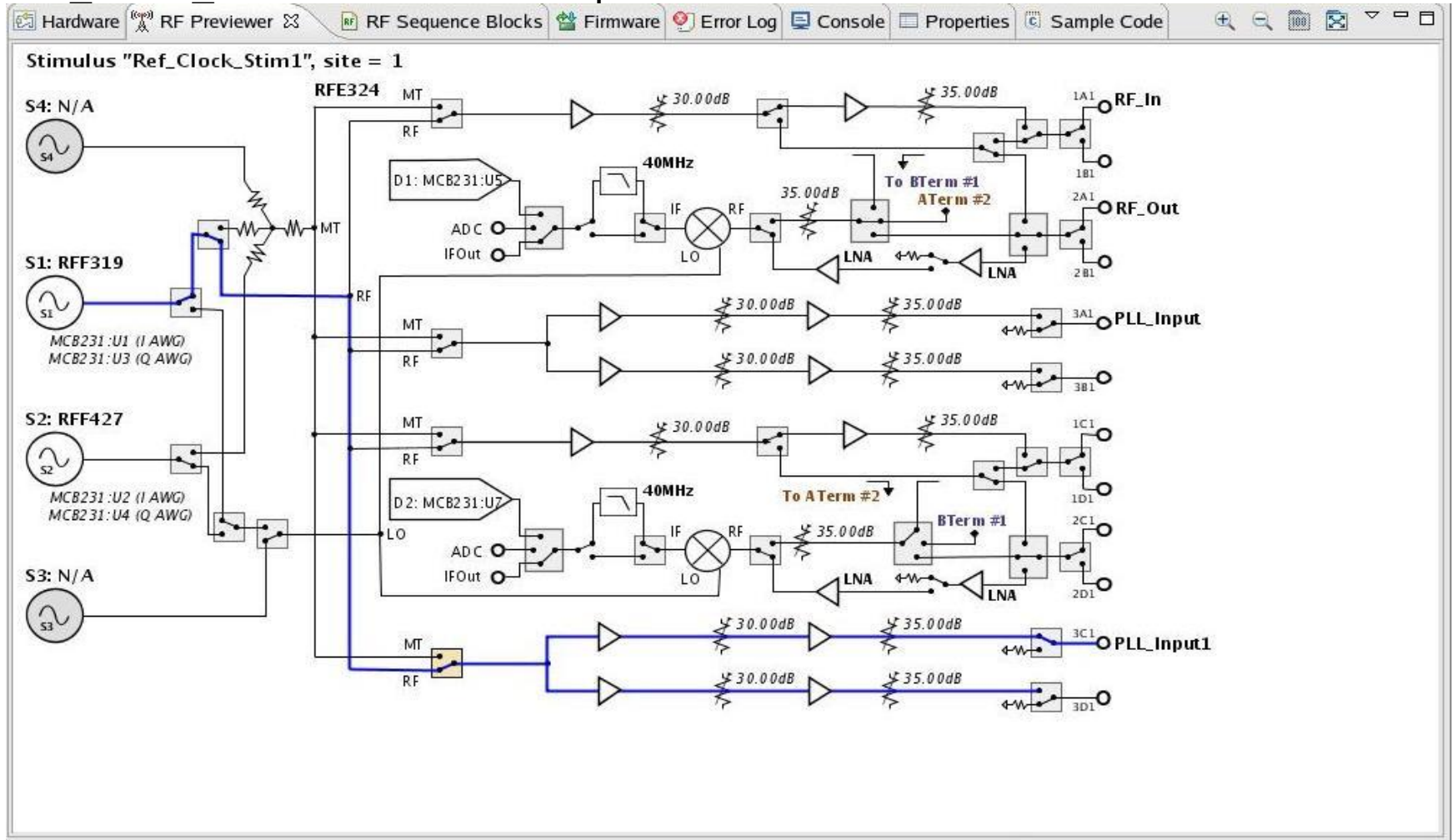
The bottom window, titled 'Sequence Setting of "Ref_Clock_Stim1"', shows the initial settings for the stimulus. It contains a 'Functional Block 1' section with the following settings:

- Comment: (empty)
- Stimulus State: On
- Frequency List Index: 0
- Output Power (dBm): 5

Test Program Development & Debugging

Demodulator (RF to Baseband) Test

Ref_Clock_Stim1 Hardware Setup



Test Program Development & Debugging

Demodulator (RF to Baseband) Test

Create RX_Test_Stim

RX_Test_Stim (Stimulus)

Stimulus Configuration		Resource Allocation	
Pin Name	RF_In	Used with Definition	Ref_Clock_Stim1
Stimulus Type	CW	Minimum Power (dBm)	-20
Cal State	Off	Maximum Power (dBm)	-20
Multi-Pin Stimulus	FALSE	Frequency List	RX_Stim_Freq
		Stimulus Path	Amplifier

Properties Sequencer Grouping

Hardware RF Previewer RF Sequence Blocks Firmware Error Log Console Properties

Sequence Setting of "RX_Test_Stim"

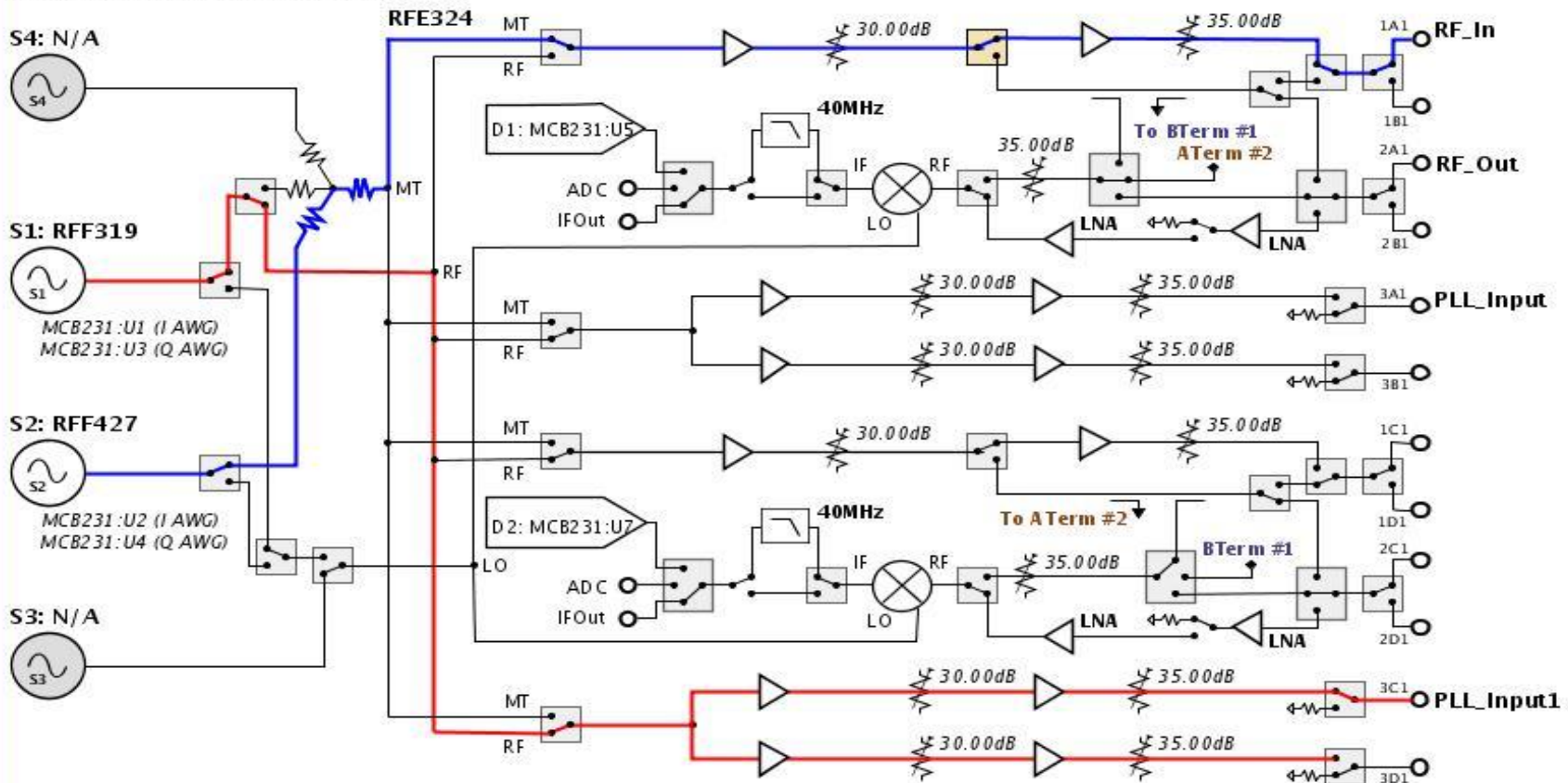
Functional Block 1	
RX_Test_Stim: Initial Settings	
Comment	
Stimulus State	On
Frequency List Index	0
Output Power (dBm)	PowerValue
Ref_Clock_Stim1: Initial Settings	
Comment	
Stimulus State	On

Test Program Development & Debugging

Demodulator (RF to Baseband) Test

RX_Test_Stim Hardware Setup

Stimulus "RX_Test_Stim", site = 1



Test Program Development & Debugging

Demodulator (RF to Baseband) Test

Calculate F_s for Digitizer

RF to Baseband Test: Baseband Signal $F_t = 3\text{MHz}$

Number of Points $N = 512$

Frequency Bin $M = 25$

Sampling Frequency $F_s = 61.44\text{ MHz}$

Master Clock on the RF Measurement can be set to $F_s * 8 = 491.52\text{MHz}$

RF Sequencer Block View

The screenshot displays the 'Sequence Setting of "RX_Test_Stim"' window. It features a tabbed interface with 'Hardware', 'RF Previewer', 'RF Sequence Blocks', and 'Firmware'. The 'RF Sequence Blocks' tab is active, showing a tree view with 'Functional Block 1' expanded. Under 'Functional Block 1', there are two sections: 'RX_Test_Stim: Initial Settings' and 'Ref_Clock_Stim1: Initial Settings'. Each section contains fields for 'Comment', 'Stimulus State' (set to 'On'), 'Frequency List Index' (set to '0'), and 'Output Power (dBm)'. The 'Output Power (dBm)' field for 'RX_Test_Stim' is set to 'PowerValue', and for 'Ref_Clock_Stim1' it is set to '5'.

Block	Comment	Stimulus State	Frequency List Index	Output Power (dBm)
RX_Test_Stim: Initial Settings		On	0	PowerValue
Ref_Clock_Stim1: Initial Settings		On	0	5

Test Program Development & Debugging

Demodulator (RF to Baseband) Test

Digitizer Setups to RX_Test_Stim Analog Control Set

Analog Setup Tool

File Help

Analog Set Explorer Save Setup File Reset Config Snapshot

Setup Clock domain Setup Setup Focus: 0 Query Focus: 1

Clock Domain Setup

Analog clock source INT Append Set Name Set:RX_Test_Stim Add

Timing Equation Set Waveform Set 1 Timing Set 1

Instrument MCB231_U5 Location CardCage 4 Slot 08 Change Delete

Clock Domain Analog Check domain Check All

Clock Value 491.5 MHz Clock Mode Auto

Fs 61.44 MHz N 8

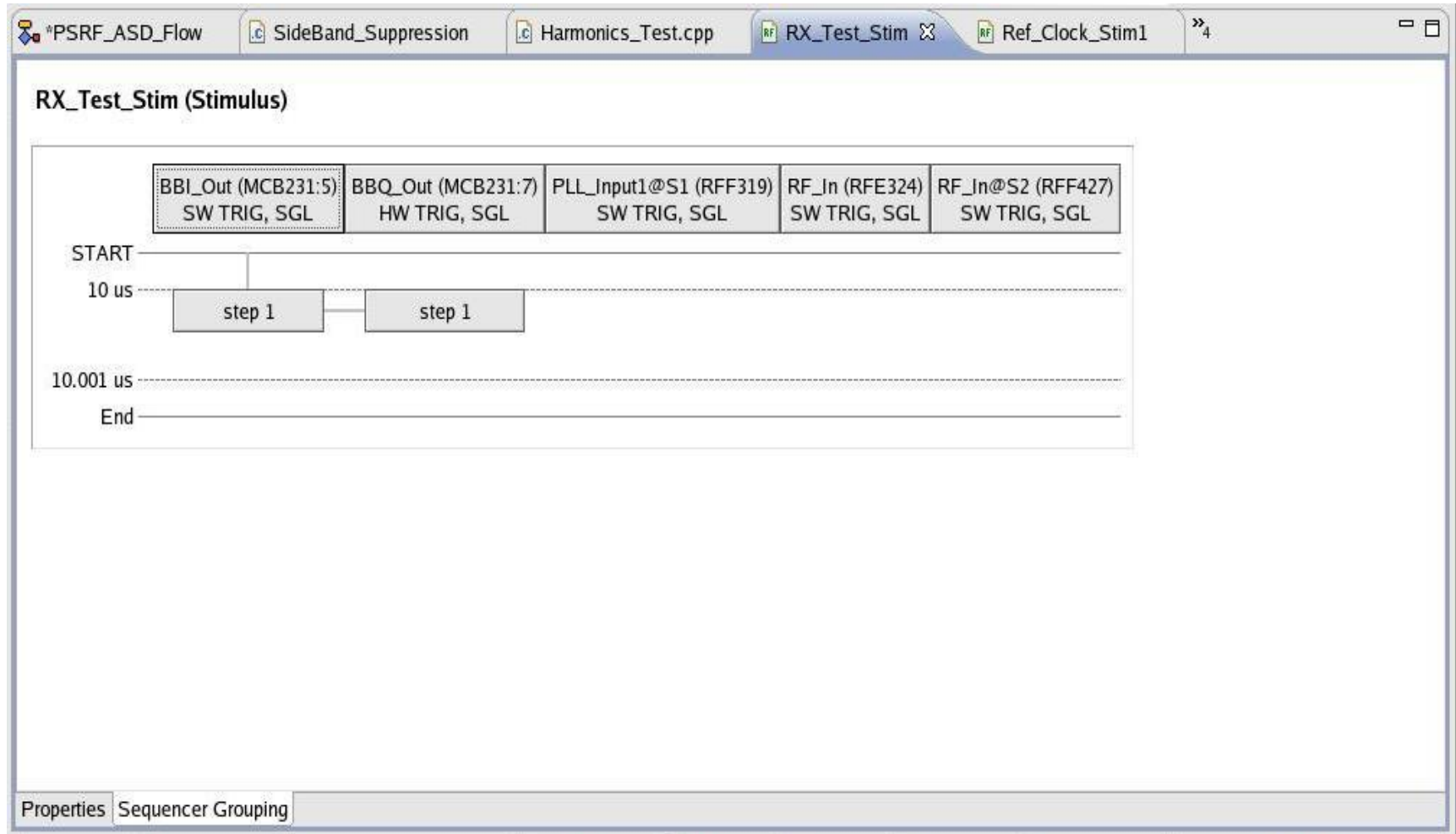
Rule Auto (Fs) ☒ Auto check

Instrument	Location	Clock Domain	Clock Mode	Clock Value	Fs	N	Rule	Actual Fs	Remark
MCB231_U5	CardCage 4 S...	Analog	Auto	491.52 MHz	61.44 MHz	8	Auto (Fs)	61.44 MHz	110Msps IQ ...
MCB231_U7	CardCage 4 S...	Analog	Auto	491.52 MHz	61.44 MHz	8	Auto (Fs)	61.44 MHz	110Msps IQ ...

Test Program Development & Debugging

Demodulator (RF to Baseband) Test

Final Sequencer Grouping & Code for Test Method



Test Program Development & Debugging

Demodulator (RF to Baseband) Test

Final Sequencer Grouping & Code for Test Method

```
ARRAY_D freqArrayI, freqArrayQ, timeArrayI, timeArrayQ;
ARRAY_COMPLEX iqArray, ifreq, qfreq;
DOUBLE i_real, q_real, i_image, q_image, i_phase, q_phase, i_mag, q_mag;
DOUBLE RX_Amp_Imbalance, RX_Phase_Imbalance, pwr;
Analog.primary("RX_Test_Stim");
pwr = DATA_DEF("Power_Sweep").getValue(0);
DATA_DEF("PowerValue").set(pwr);
ON_FIRST_INVOCATION_BEGIN();
    STIM_DEF().disableAll().connectAll();
    EXECUTE_GROUP(); // SW Triggers the sequence
ON_FIRST_INVOCATION_END();
iqArray = DGT("BBI_Out").getComplexWaveform();
timeArrayI = iqArray.getReal(); timeArrayQ = iqArray.getImag();
DSP_FFT(timeArrayI, ifreq, RECT); DSP_FFT(timeArrayQ, qfreq, RECT);
i_real = ifreq[25].real(); i_image = ifreq[25].imag();
i_mag = sqrt(i_real*i_real+i_image*i_image);
q_real = qfreq[25].real(); q_image = qfreq[25].imag();
q_mag = sqrt(q_real*q_real+q_image*q_image);
i_mag = 20*log10(i_mag*sqrt(500.0/50.0)); //convert to dBm
q_mag = 20*log10(q_mag*sqrt(500.0/50.0)); //convert to dBm
i_phase = 180*(atan2(i_image, i_real))/M_PI; q_phase = 180*(atan2(q_image, q_real))/M_PI;
cout << "*****Testsuite: RF_BB_IQ_Imbalance_Test*****"<<endl;
cout << "\t I mag = "<<i_mag<<" dBm "<<endl; cout << "\t Q mag = "<<q_mag<<" dBm "<<endl;
cout << "\t I phase = "<<i_phase<<" Degree "<<endl; cout << "\t Q phase = "<<q_phase<<" Degree "<<endl;
RX_Amp_Imbalance = q_mag - i_mag;
RX_Phase_Imbalance = 90 - abs(q_phase - i_phase);
if(RX_Phase_Imbalance > 180 )
{
    RX_Phase_Imbalance = RX_Phase_Imbalance -180;
}
else if (RX_Phase_Imbalance < -180 )
{
    RX_Phase_Imbalance = RX_Phase_Imbalance +180;
}
cout << "\t IQ Amplitude Imbalance = "<<RX_Amp_Imbalance<<" dB "<<endl;
cout << "\t IQ Phase Imbalance = "<<RX_Phase_Imbalance<<" Degree "<<endl;
TEST( "BBI_Out, BBQ_Out", "RX_Amp_Imbalance", RX_Amp_Imbalance );
TEST( "BBI_Out, BBQ_Out", "RX_Phase_Imbalance", RX_Phase_Imbalance );
```

Test Program Development & Debugging

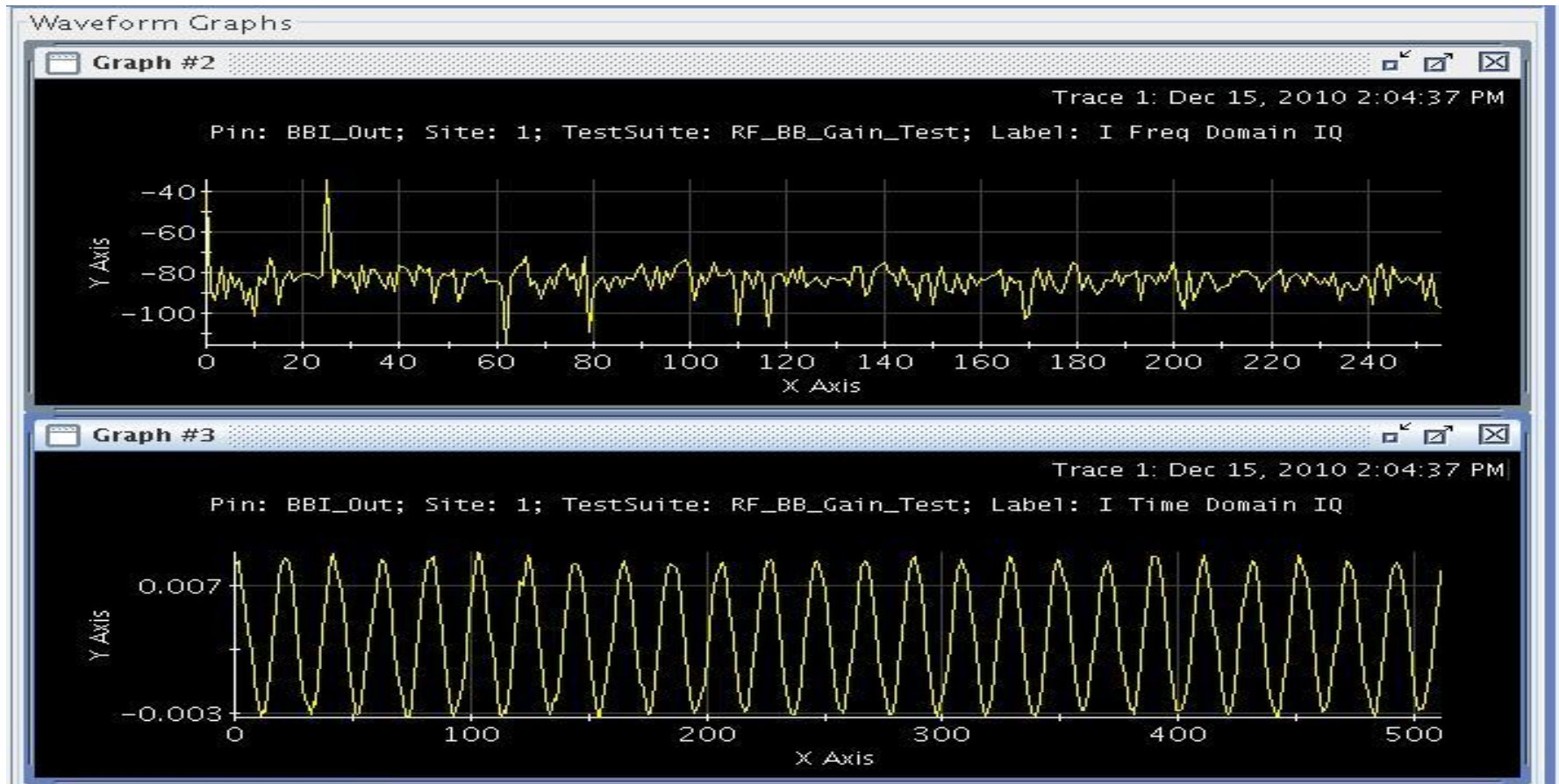
Datalog and Waveform Analysis for Demodulator

Datalog for Demodulator



Datalog for RFT0BB

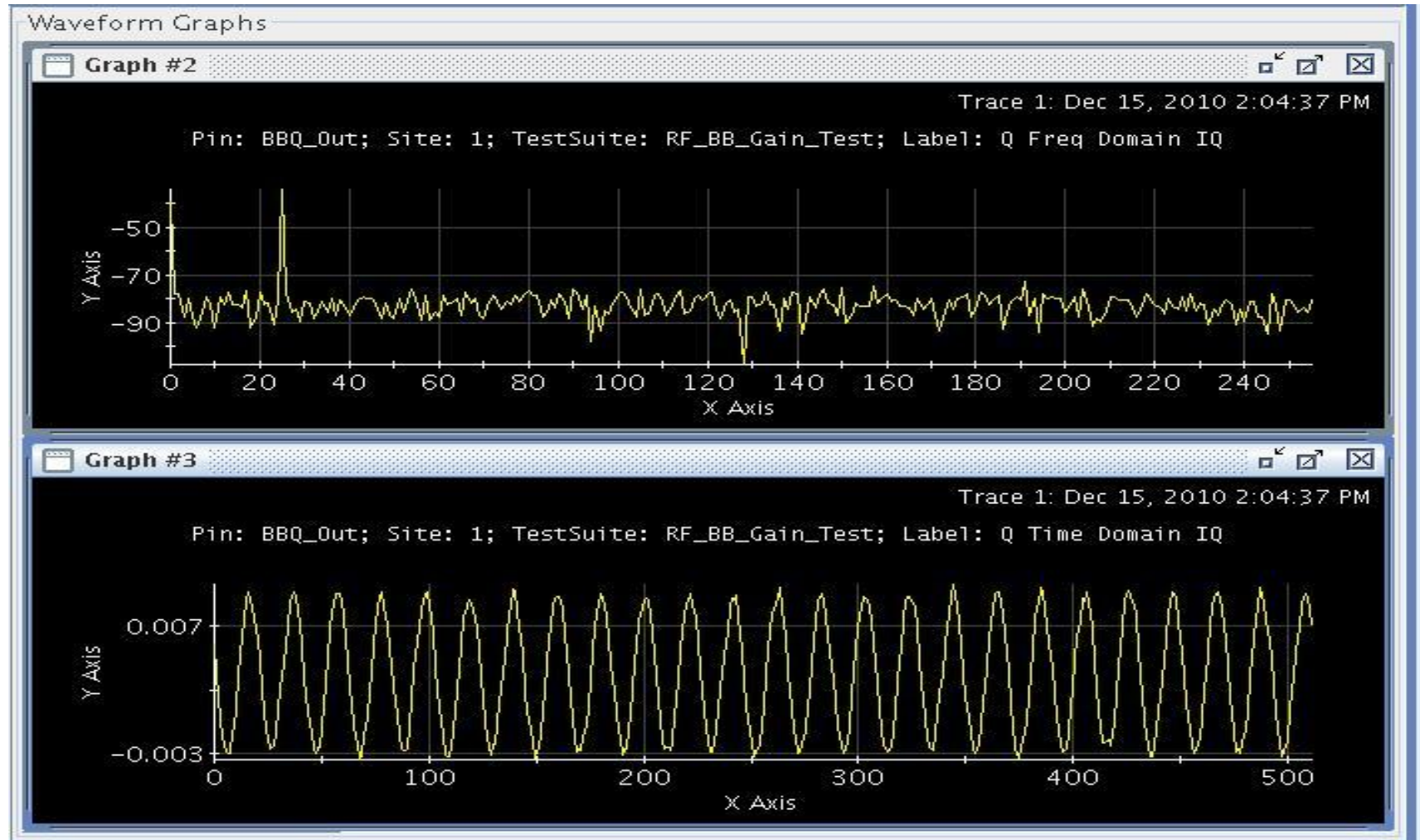
I Waveform Capture in Time & Frequency Domain



Test Program Development & Debugging

Datalog and Waveform Analysis for Demodulator

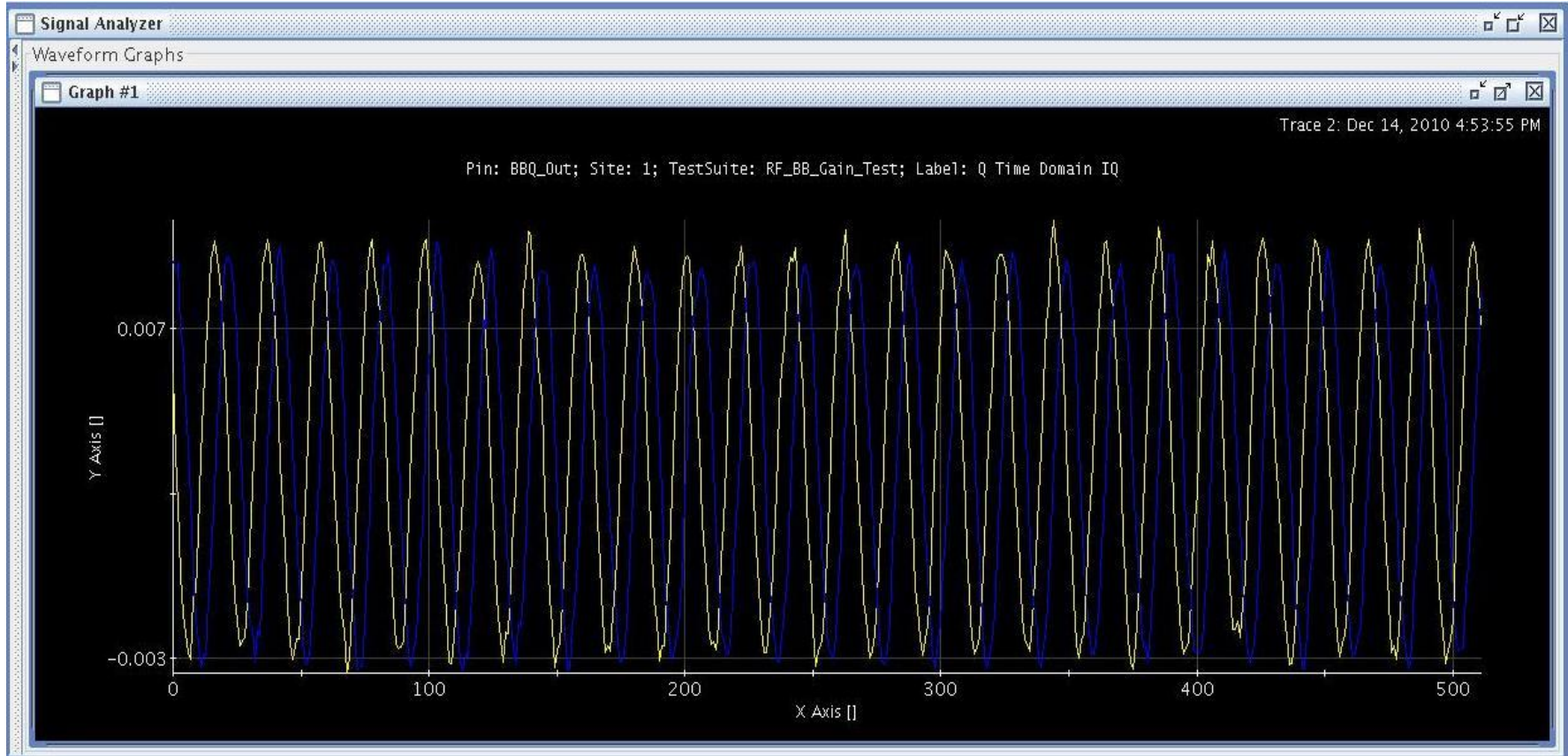
Q Waveform Capture in Time & Frequency Domain



Test Program Development & Debugging

Datalog and Waveform Analysis for Demodulator

I/Q Waveform Capture Overlap in Time Domain



IQ Amplitude Imbalance: $-0.5 \text{ dB} < 0.262095 \text{ dB} < 0.5 \text{ dB}$

IQ Phase Imbalance: $-5 \text{ Degree} < 0.875716 \text{ Degree} < 5 \text{ Degree}$

Summary

Achievement of Skill & Knowledge:

1. Basic Knowledge of RF testing and RF device.
2. Good Skill about basic RF test like IP3, S-parameter, Carrier Suppression.
3. Basic test development skill for RF chip, Create Frequency List, Stimulus and Power measurement .
4. How to use of Spectrum Analyzer to measure RF signal power.
5. How to debug RF testing with Sequencer Grouping.
6. Understanding of V93K Hardware for RF testing , RF source Card, RF Front End Card, MB Av8 Card.
7. Understanding and application of flowing API function: DATA_DEF, STIM_DEF, EXECUTE_GROUP, DSP_FFT, DSP_RF_CW_POWER, MEAS_DEF
8. Basic Calculation of power for sine signal.

Q/A

Thanks !