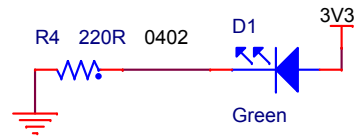
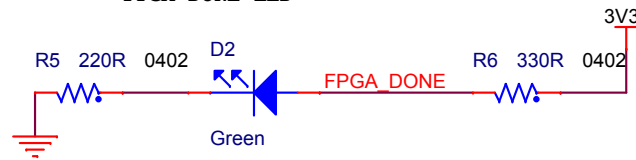




POWER LED



FPGA DONE LED



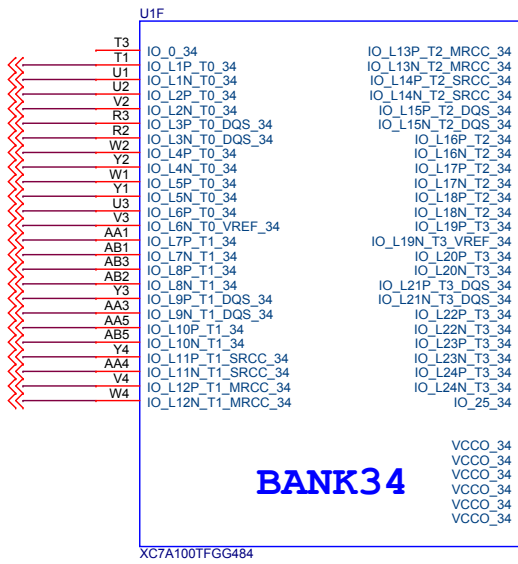


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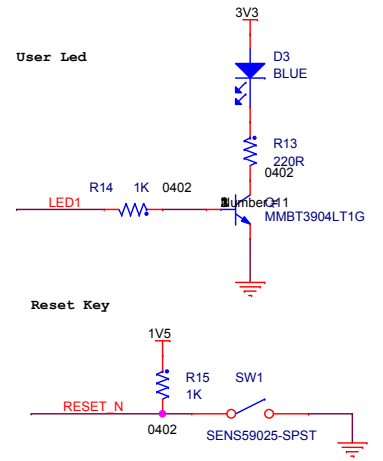
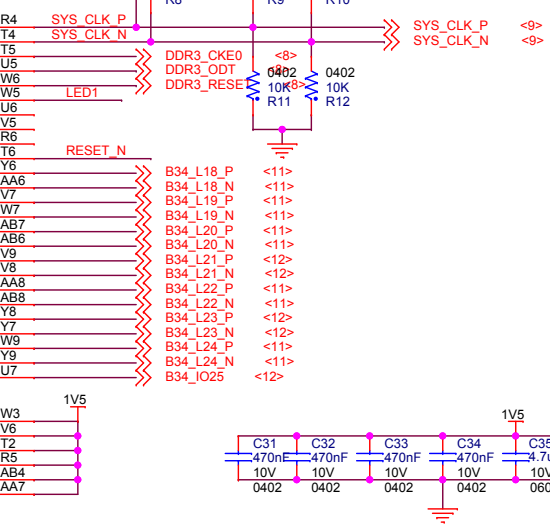
WU SYSTEM

ICAP Classification: FCP: FIUO: PUBI:		
Drawing Title: A7-AC7100T-Main		
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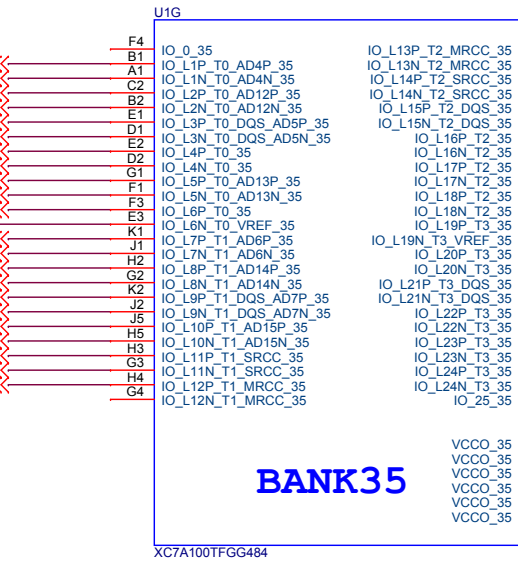
<8> DDR3_A7
<8> DDR3_A13
<8> DDR3_A9
<8> DDR3_A8
<8> DDR3_CLK0_P
<8> DDR3_CLK0_N
<8> DDR3_A11
<8> DDR3_A12
<8> DDR3_A6
<8> DDR3_A10
<8> DDR3_A5
<8> DDR3_A14
<8> DDR3_VE
<8> DDR3_A4
<8> DDR3_S0
<8> DDR3_A1
<8> DDR3_BA1
<8> DDR3_BA0
<8> DDR3_A2
<8> DDR3_A3
<8> DDR3_BA2
<8> DDR3_A0
<8> DDR3_RAS
<8> DDR3_CAS



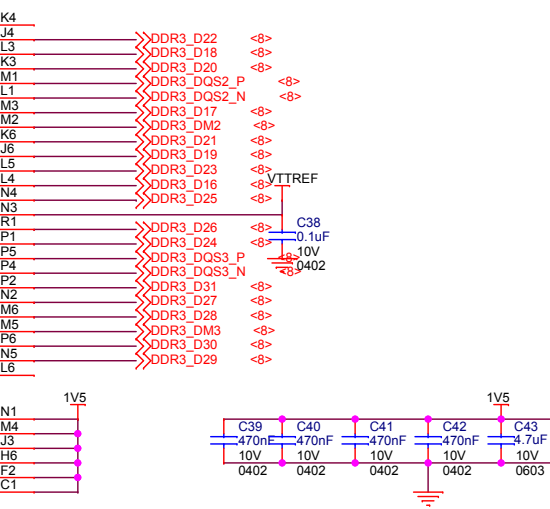
BANK34





<8> DDR3_D6
<8> DDR3_D2
<8> DDR3_D0
<8> DDR3_D4
<8> DDR3_DQS0_P
<8> DDR3_DQS0_N
<8> DDR3_D7
<8> DDR3_DM0
<8> DDR3_D1
<8> DDR3_D5
<8> DDR3_D3
<8> DDR3_D14
<8> DDR3_D12
<8> DDR3_D10
<8> DDR3_DM1
<8> DDR3_DQS1_P
<8> DDR3_DQS1_N
<8> DDR3_D13
<8> DDR3_D11
<8> DDR3_D8
<8> DDR3_D9
<8> DDR3_D15



BANK35



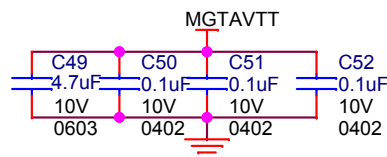
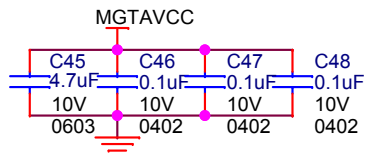
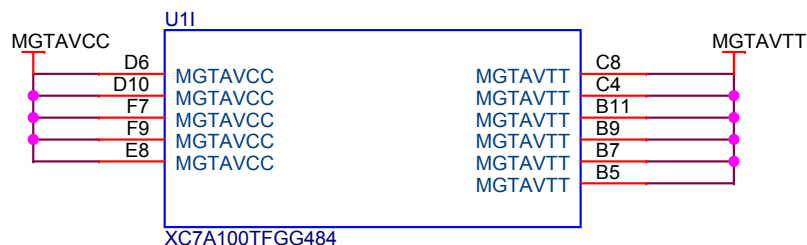
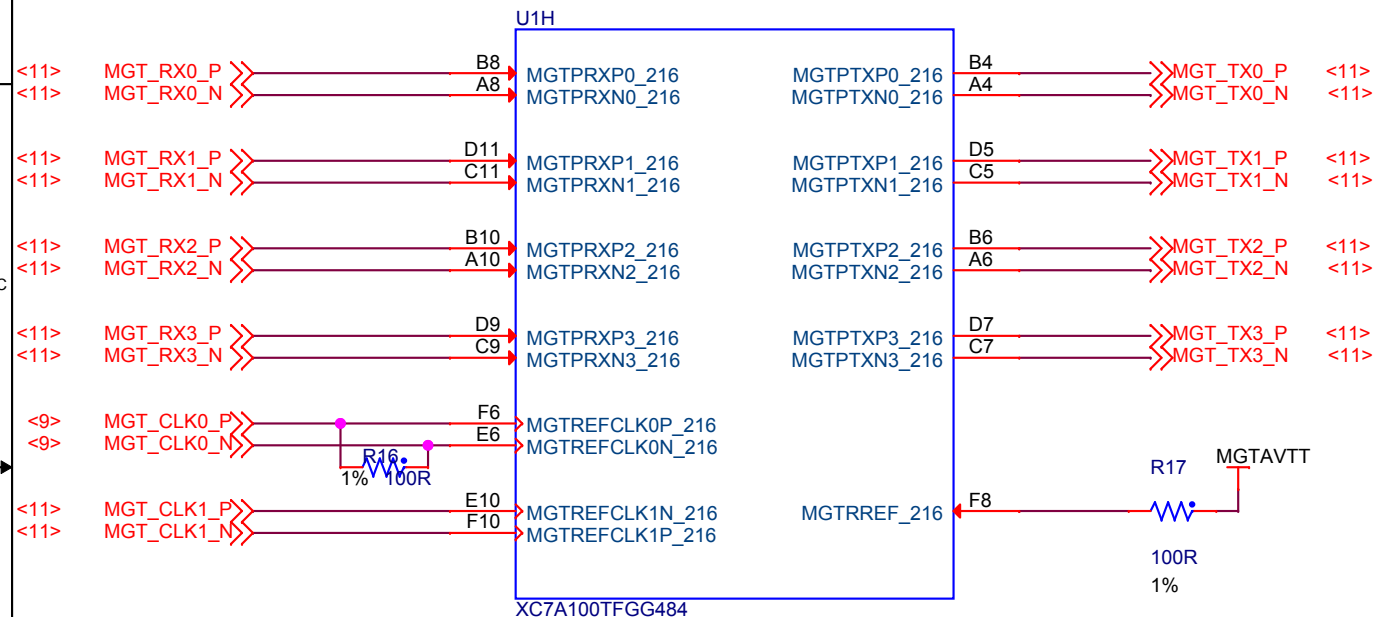




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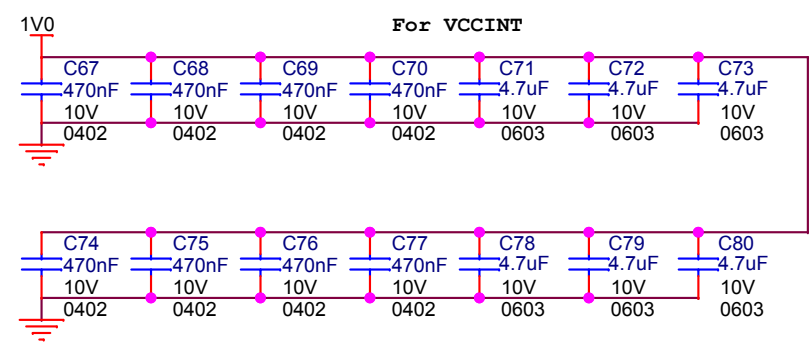
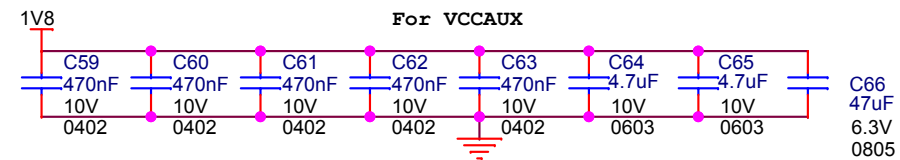
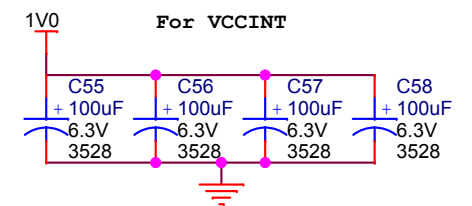
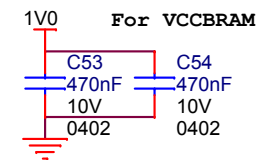
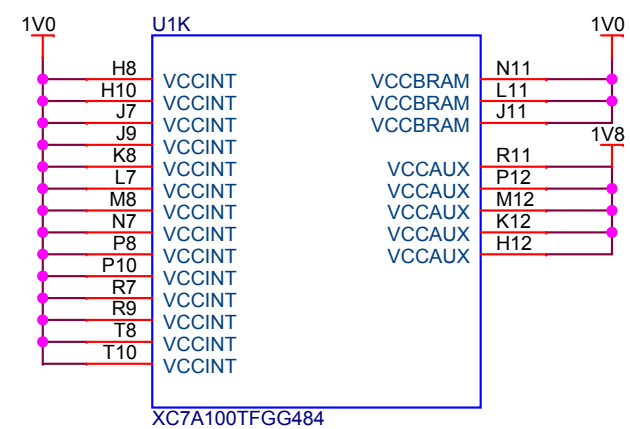
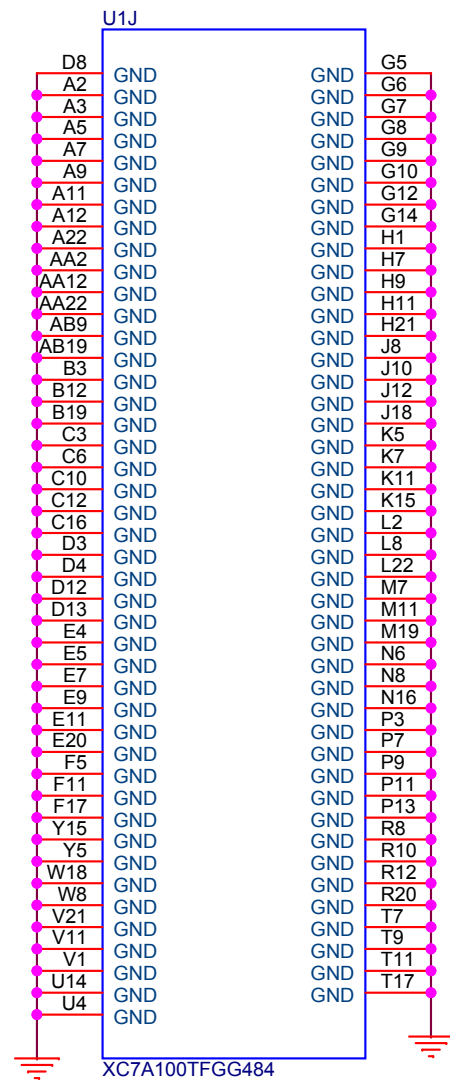
WU SYSTEM



ICAP Classification:	FCP:	FIUC:	PUBI:
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BANK216



  WU SYSTEM	
ICAP Classification: FCP: FIUO: PUBI:	
Drawing Title: A7-AC7100T-Main	
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WU SYSTEM

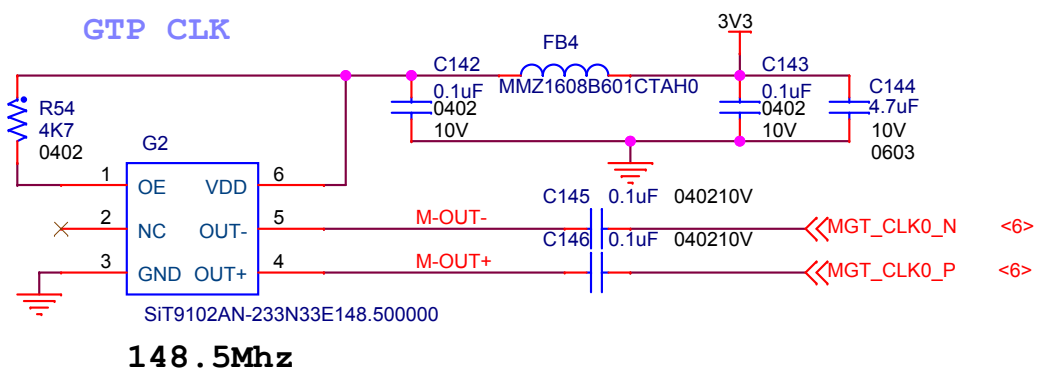
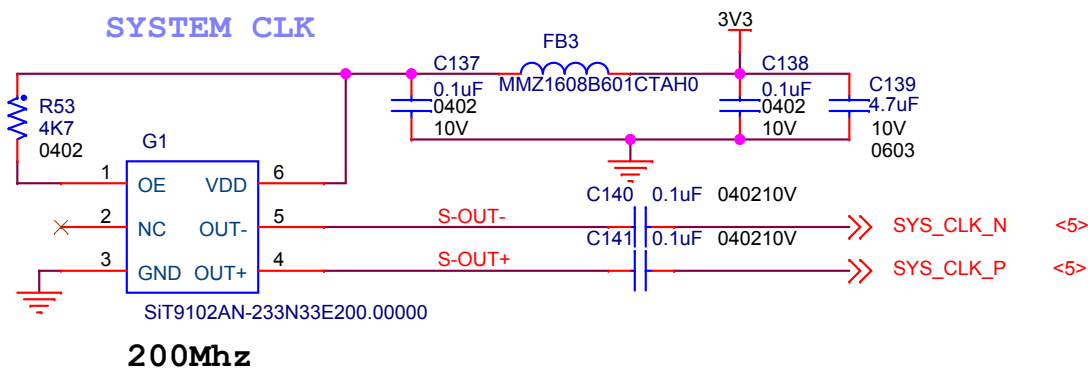
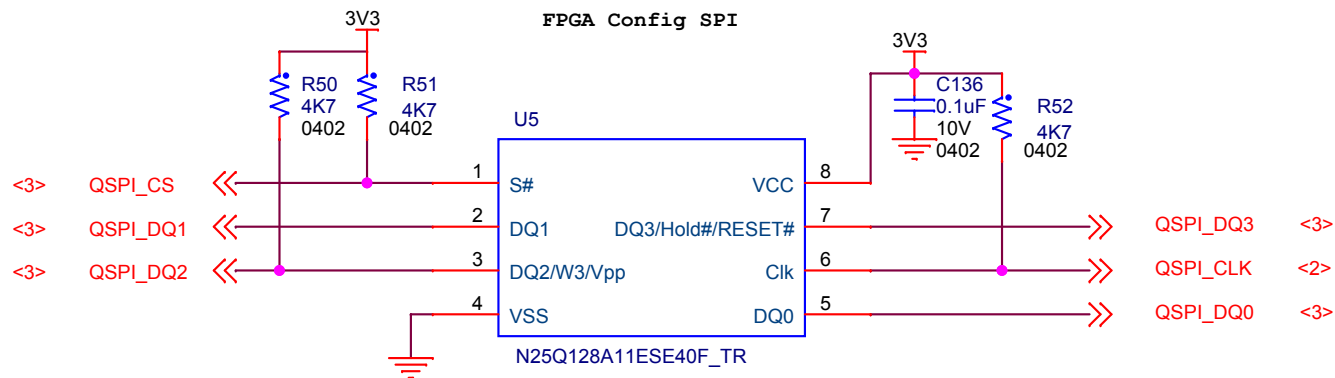
ICAP Classification: FCP: FIUO: PUBI:

Drawing Title: **A7-AC7100T-Main**

Page Title: **FPGA PWR**

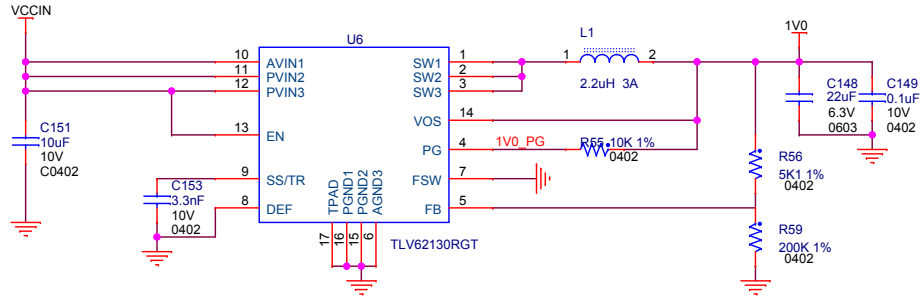
Size A	Document Number <Doc>	Rev A
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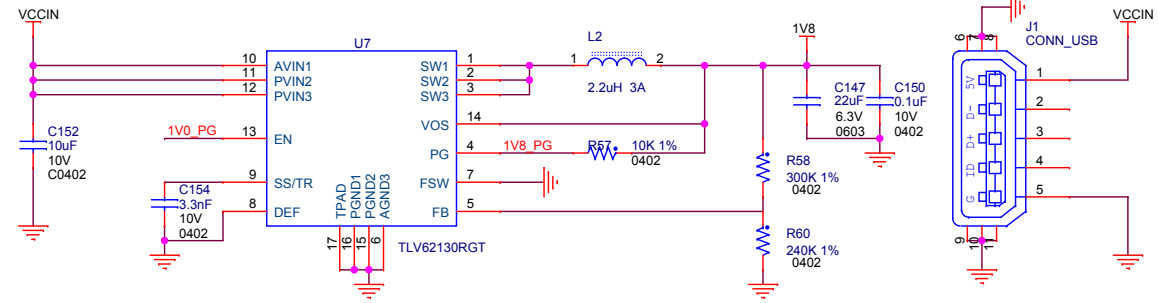


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WU SYSTEM	
ICAP Classification: _____ FCP: _____ FIUO: _____ PUBI: _____	
Drawing Title: A7-AC7100T-Main	
Page Title: FLASH & CLK	
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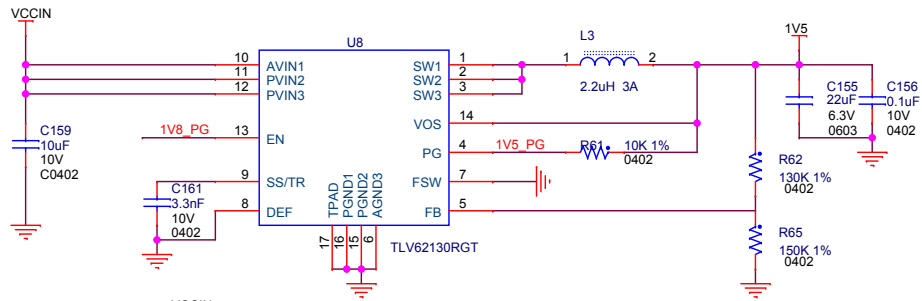
1.0V POWER



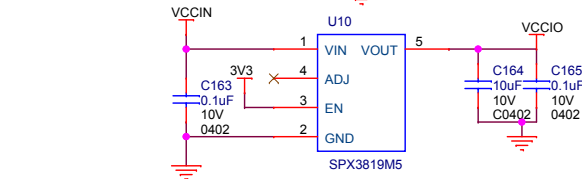
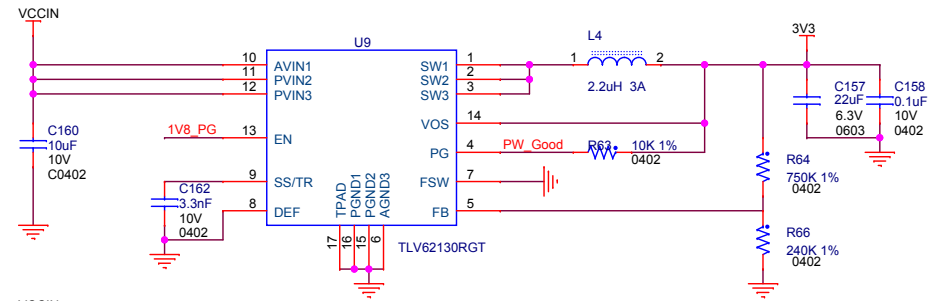
1.8V POWER



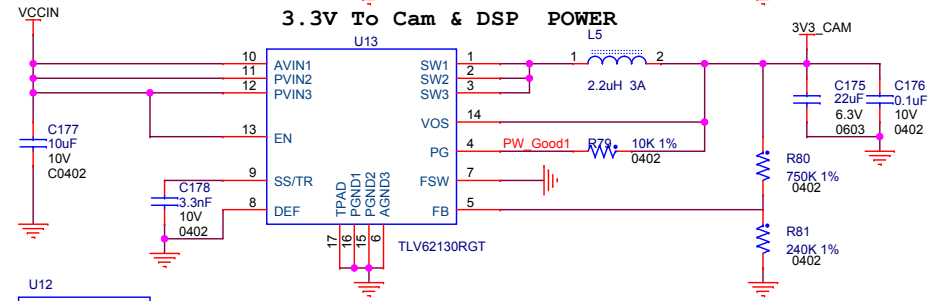
1.5V POWER



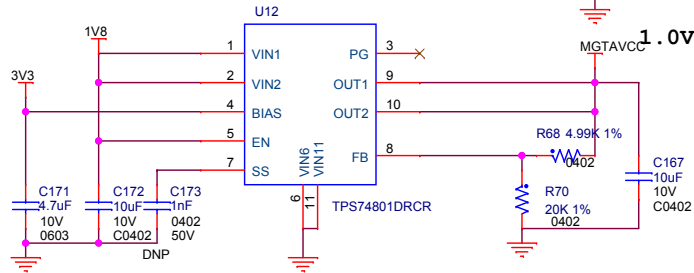
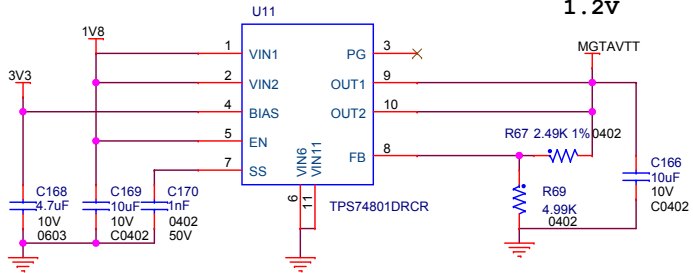
3.3V POWER





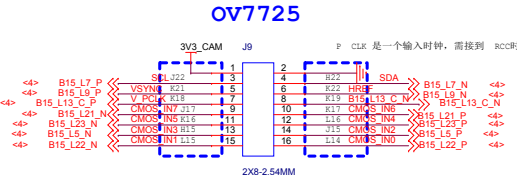
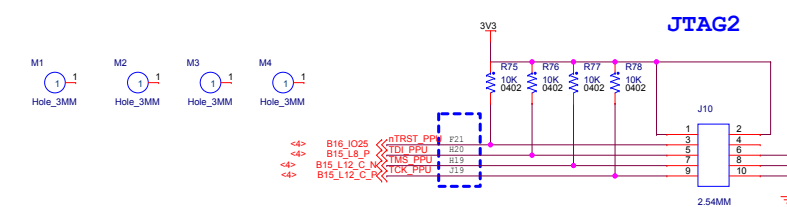
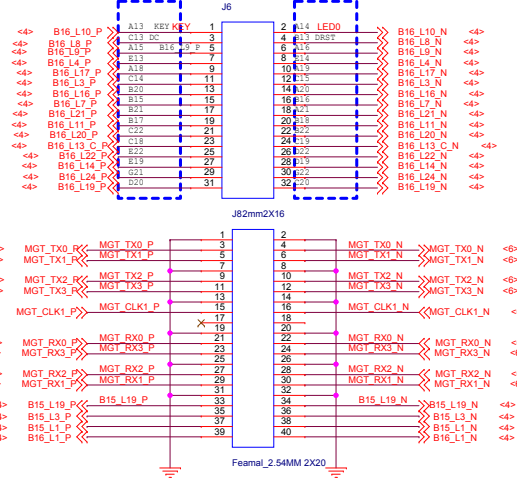
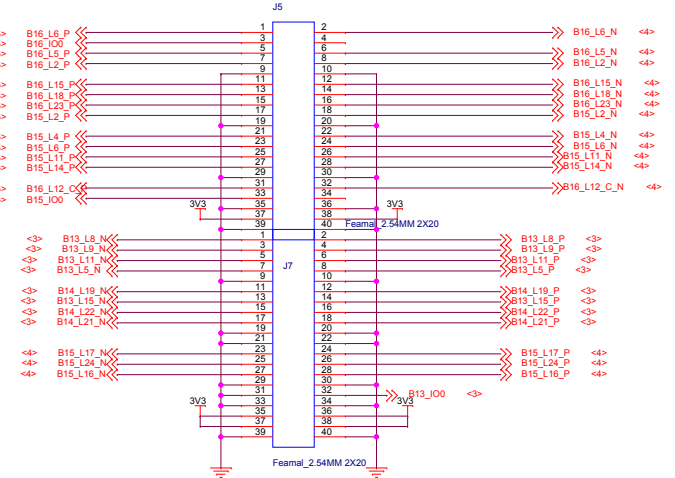
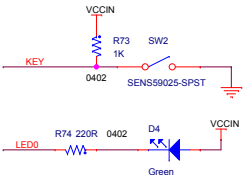
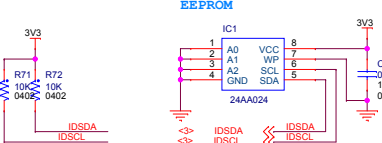
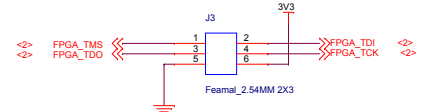
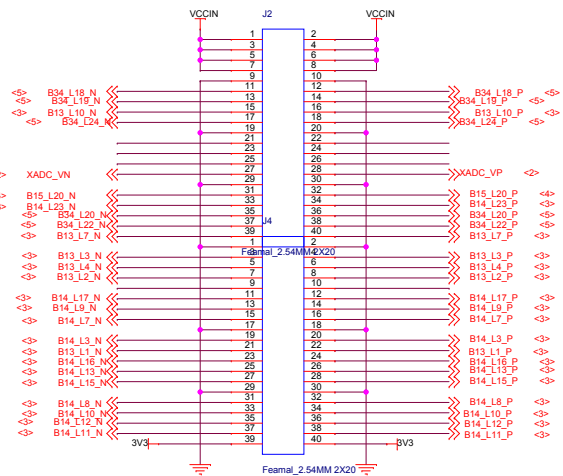
POWER ON: VCCINT (1.0V) -> VMGTAVCC (1.0V) -> VMGTAVTT (1.2V)



1.2V



 	
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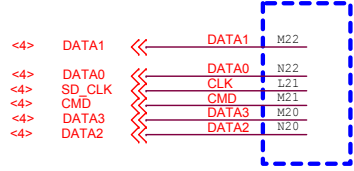
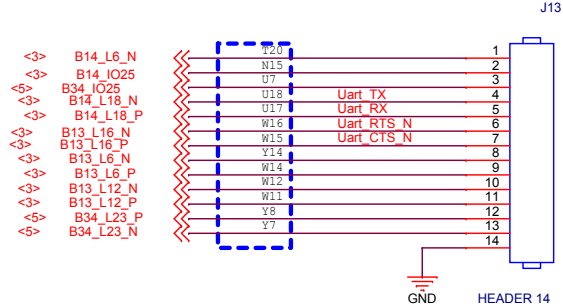
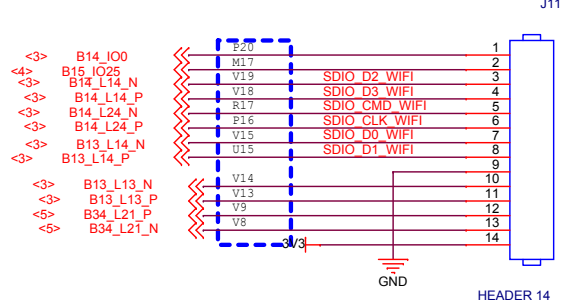
OV7725

P CLK 是一个输入时钟，需接到 RCC时钟管脚上。

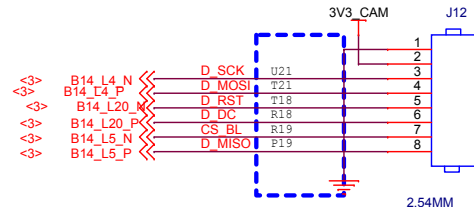
 	
ICAP Classification: FCP: _____ FIUC: _____ PUB: _____	
Drawing Title: A7-AC7100T-Main	
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输入时钟必须接到MRCC或者SRCC 管脚上
输出时钟可以随意配置。

WIFI



Display



TF Card

