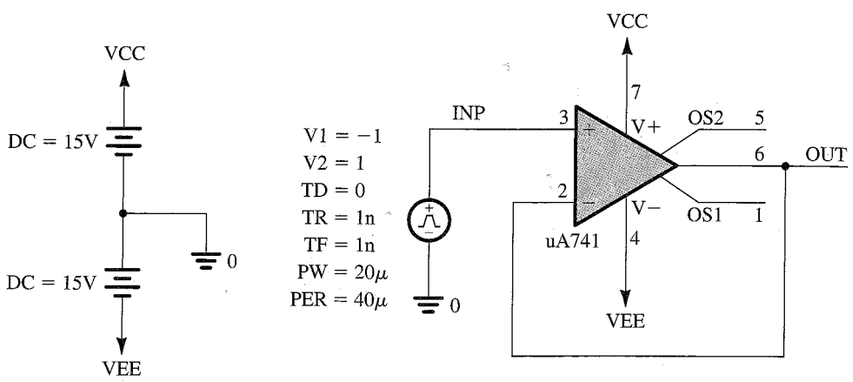



**FIGURE 2.51** Circuit for determining the slew rate of the $\mu$A741 op amp in Example 2.9.

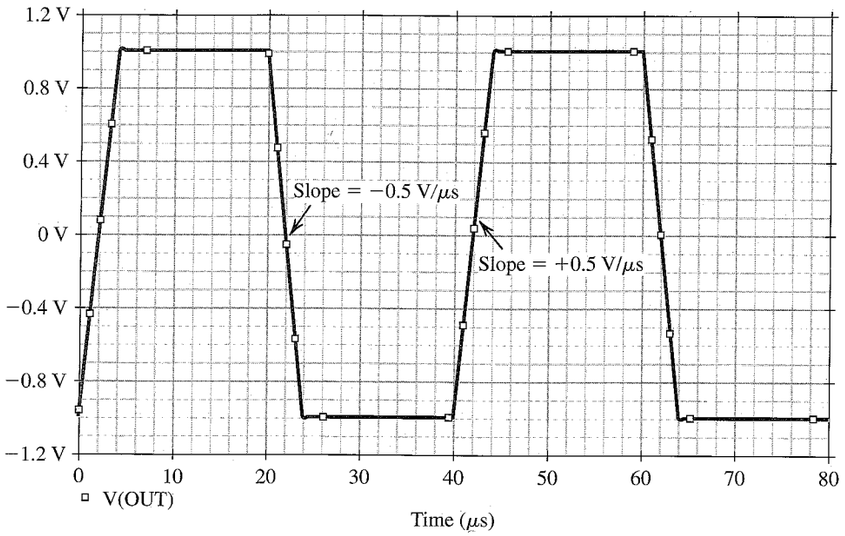



**FIGURE 2.52** Square-wave response of the $\mu$A741 op amp connected in the unity-gain configuration shown in Fig. 2.51.

## SUMMARY

- The IC op amp is a versatile circuit building block. It is easy to apply, and the performance of op-amp circuits closely matches theoretical predictions.
- The op-amp terminals are the inverting input terminal (1), the noninverting input terminal (2), the output terminal (3), the positive-supply terminal ($V^+$) to be connected to the positive power supply, and the negative-supply terminal ($V^-$) to be connected to the negative supply. The common terminal of the two supplies is the circuit ground.
- The ideal op amp responds only to the difference input signal, that is, $(v_2 - v_1)$; provides at the output, between terminal 3 and ground, a signal $A(v_2 - v_1)$, where $A$, the open-loop gain, is very large ($10^4$ to $10^6$) and ideally infinite; and has an infinite input resistance and a zero output resistance.
- Negative feedback is applied to an op amp by connecting a passive component between its output terminal and its inverting (negative) input terminal. Negative feedback causes the voltage between the two input terminals to become very small and ideally zero. Correspondingly, a virtual short circuit is said to exist between the two input terminals. If the positive input terminal is connected to ground, a virtual ground appears on the negative input terminal.
- The two most important assumptions in the analysis of op-amp circuits, presuming negative feedback exists and the op amps are ideal, are: the two input terminals of the op amp are at the same voltage, and zero current flows into the op-amp input terminals.
- With negative feedback applied and the loop closed, the closed-loop gain is almost entirely determined by external components: For the inverting configuration, $V_o/V_i = -R_2/R_1$; and for the noninverting configuration, $V_o/V_i = 1 + R_2/R_1$.
- The noninverting closed-loop configuration features a very high input resistance. A special case is the unity-gain follower, frequently employed as a buffer amplifier to connect a high-resistance source to a low-resistance load.
- For most internally compensated op amps, the open-loop gain falls off with frequency at a rate of −20 dB/decade, reaching unity at a frequency $f_t$ (the unity-gain bandwidth). Frequency $f_t$ is also known as the gain–bandwidth product of the op amp: $f_t = A_0 f_b$, where $A_0$ is the dc gain, and $f_b$ is the 3-dB frequency of the open-loop gain. At any frequency $f (f \gg f_b)$, the op-amp gain $|A| \simeq f_t/f$.



- For both the inverting and the noninverting closed-loop configurations, the 3-dB frequency is equal to $f_t/(1 + R_2/R_1)$.
- The maximum rate at which the op-amp output voltage can change is called the slew rate. The slew rate, SR, is usually specified in V/$\mu$s. Op-amp slewing can result in nonlinear distortion of output signal waveforms.
- The full-power bandwidth, $f_M$, is the maximum frequency at which an output sinusoid with an amplitude equal to the op-amp rated output voltage ($V_{omax}$) can be produced without distortion: $f_M = \text{SR}/2\pi V_{omax}$.
- The input offset voltage, $V_{OS}$, is the magnitude of dc voltage that when applied between the op amp input terminals, with appropriate polarity, reduces the dc offset voltage at the output to zero.
- The effect of $V_{OS}$ on performance can be evaluated by including in the analysis a dc source $V_{OS}$ in series with the op-amp positive input lead. For both the inverting and the noninverting configurations, $V_{OS}$ results in a dc offset voltage at the output of $V_{OS}(1 + R_2/R_1)$.
- Capacitively coupling an op amp reduces the dc offset voltage at the output considerably.
- The average of the two dc currents, $I_{B1}$ and $I_{B2}$, that flow in the input terminals of the op amp, is called the input bias current, $I_B$. In a closed-loop amplifier, $I_B$ gives rise to a dc offset voltage at the output of magnitude $I_B R_2$. This voltage can be reduced to $I_{OS} R_2$ by connecting a resistance in series with the positive input terminal equal to the total dc resistance seen by the negative input terminal. $I_{OS}$ is the input offset current; that is, $I_{OS} = |I_{B1} - I_{B2}|$.
- Connecting a large resistance in parallel with the capacitor of an op-amp inverting integrator prevents op-amp saturation (due to the effect of $V_{OS}$ and $I_B$).

# PROBLEMS

### SECTION 2.1: THE IDEAL OP AMP

**2.1** What is the minimum number of pins required for a so-called dual-op-amp IC package, one containing two op amps? What is the number of pins required for a so-called quad-op-amp package, one containing four op amps?

**2.2** The circuit of Fig. P2.2 uses an op amp that is ideal except for having a finite gain $A$. Measurements indicate $v_O = 4.0$ V when $v_I = 4.0$ V. What is the op amp gain $A$?

**2.3** Measurement of a circuit incorporating what is thought to be an ideal op amp shows the voltage at the op amp output to be

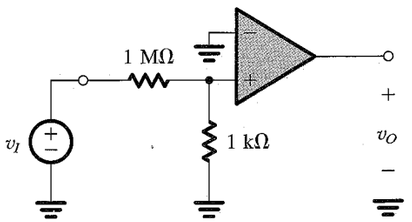



**FIGURE P2.2**

−2.000 V and that at the negative input to be −3.000 V. For the amplifier to be ideal, what would you expect the voltage at the positive input to be? If the measured voltage at the positive input is −3.020 V, what is likely to be the actual gain of the amplifier?

**2.4** A set of experiments are run on an op amp that is ideal except for having a finite gain $A$. The results are tabulated below. Are the results consistent? If not, are they reasonable, in view of the possibility of experimental error? What do they show the gain to be? Using this value, predict values of the measurements that were accidentally omitted (the blank entries).

| Experiment # | $v_1$ | $v_2$ | $v_O$ |
|---|---|---|---|
| 1 | 0.00 | 0.00 | 0.00 |
| 2 | 1.00 | 1.00 | 0.00 |
| 3 | | 1.00 | 1.00 |
| 4 | 1.00 | 1.10 | 10.1 |
| 5 | 2.01 | 2.00 | −0.99 |
| 6 | 1.99 | 2.00 | 1.00 |
| 7 | 5.10 | | −5.10 |

**2.5** Refer to Exercise 2.3. This problem explores an alternative internal structure for the op amp. In particular, we wish to model the internal structure of a particular op amp using two transconductance amplifiers and one transresistance amplifier. Suggest an appropriate topology. For equal transconductances $G_m$ and a transresistance $R_m$, find an expression for the open-loop gain $A$. For $G_m = 100$ mA/V and $R_m = 10^6\ \Omega$, what value of $A$ results?

**2.6** The two wires leading from the output terminals of a transducer pick up an interference signal that is a 60-Hz, 1-V sinusoid. The output signal of the transducer is sinusoidal of 10-mV amplitude and 1000-Hz frequency. Give expressions for $v_{cm}$, $v_d$, and the total signal between each wire and the system ground.

**2.7** Nonideal (i.e., real) operational amplifiers respond to both the differential and common-mode components of their input signals (refer to Fig. 2.4 for signal representation). Thus the output voltage of the op amp can be expressed as

$$v_O = A_d v_{Id} + A_{cm} v_{Icm}$$

where $A_d$ is the differential gain (referred to simply as $A$ in the text) and $A_{cm}$ is the common-mode gain (assumed to be zero in the text). The op amp's effectiveness in rejecting common-mode signals is measured by its CMRR, defined as

$$\text{CMRR} = 20 \log \left| \frac{A_d}{A_{cm}} \right|$$

Consider an op amp whose internal structure is of the type shown in Fig. E2.3 except for a mismatch $\Delta G_m$ between the transconductances of the two channels; that is,

$$G_{m1} = G_m - \tfrac{1}{2}\Delta G_m$$

$$G_{m2} = G_m + \tfrac{1}{2}\Delta G_m$$

Find expressions for $A_d$, $A_{cm}$, and CMRR. If $A_d$ is 80 dB and the two transconductances are matched to within 0.1% of each other, calculate $A_{cm}$ and CMRR.

## SECTION 2.2: THE INVERTING CONFIGURATION

**2.8** Assuming ideal op amps, find the voltage gain $v_o/v_i$ and input resistance $R_{in}$ of each of the circuits in Fig. P2.8.

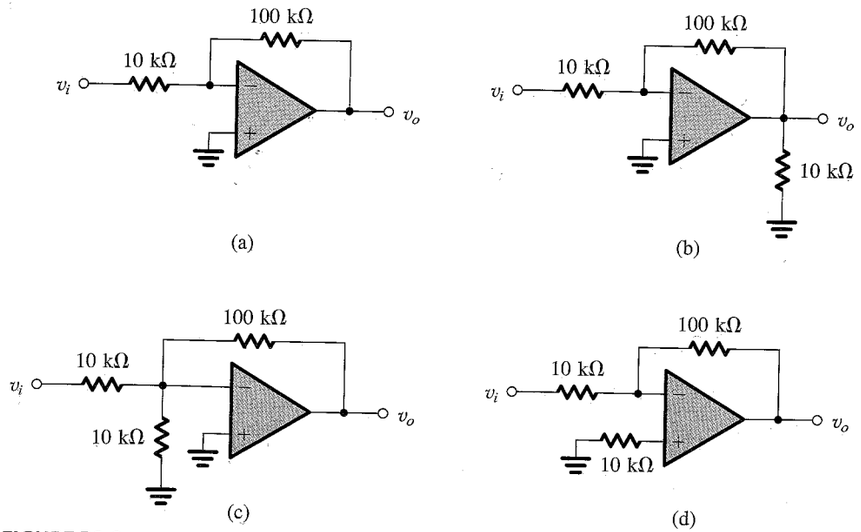



**FIGURE P2.8**



**2.9** A particular inverting circuit uses an ideal op amp and two 10-kΩ resistors. What closed-loop gain would you expect? If a dc voltage of +5.00 V is applied at the input, what output result? If the 10-kΩ resistors are said to be "5% resistors," having values somewhere in the range $(1 \pm 0.05)$ times the nominal value, what range of outputs would you expect to actually measure for an input of precisely 5.00 V?

**2.10** You are provided with an ideal op amp and three 10-kΩ resistors. Using series and parallel resistor combinations, how many different inverting-amplifier circuit topologies are possible? What is the largest (noninfinite) available voltage gain? What is the smallest (nonzero) available gain? What are the input resistances in these two cases?

**2.11** For ideal op amps operating with the following feedback networks in the inverting configuration, what closed-loop gain results?

(a) $R_1 = 10$ kΩ, $R_2 = 10$ kΩ
(b) $R_1 = 10$ kΩ, $R_2 = 100$ kΩ
(c) $R_1 = 10$ kΩ, $R_2 = 1$ kΩ
(d) $R_1 = 100$ kΩ, $R_2 = 10$ MΩ
(e) $R_1 = 100$ kΩ, $R_2 = 1$ MΩ

**D2.12** Using an ideal op amp, what are the values of the resistors $R_1$ and $R_2$ to be used to design amplifiers with the closed-loop gains listed below? In your designs, use at least one 10-kΩ resistor and another larger resistor.

(a) −1 V/V
(b) −2 V/V
(c) −0.5 V/V
(d) −100 V/V

**D2.13** Design an inverting op-amp circuit for which the gain is −5 V/V and the total resistance used is 120 kΩ.

**D2.14** Using the circuit of Fig. 2.5 and assuming an ideal op amp, design an inverting amplifier with a gain of 26 dB having the largest possible input resistance under the constraint of having to use resistors no larger than 10 MΩ. What is the input resistance of your design?

**2.15** An ideal op amp connected as shown in Fig. 2.5 of the text with $R_1 = 10$ kΩ and $R_2 = 100$ kΩ. A symmetrical square-wave signal with levels of 0 V and 1 V is applied at the input. Sketch and clearly label the waveform of the resulting output voltage. What is its average value? What is its highest value? What is its lowest value?

**2.16** For the circuit in Fig. P2.16, find the currents through all branches and the voltages at all nodes. Since the current supplied by the op amp is greater than the current drawn from the input signal source, where does the additional current come from?

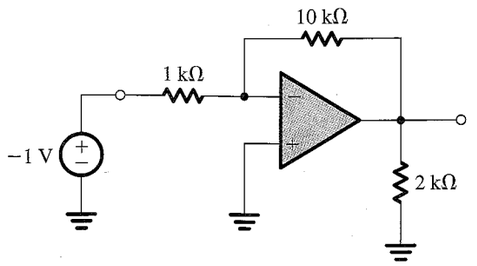



**FIGURE P2.16**

**2.17** An inverting op amp circuit is fabricated with the resistors $R_1$ and $R_2$ having $x$% tolerance (i.e., the value of each resistance can deviate from the nominal value by as much as $\pm x$%). What is the tolerance on the realized closed-loop gain? Assume the op amp to be ideal. If the nominal closed-loop gain is −100 V/V and $x = 5$, what is the range of gain values expected from such a circuit?

**2.18** An ideal op amp with 5-kΩ and 15-kΩ resistors is used to create a +5-V supply from a −15-V reference. Sketch the circuit. What are the voltages at the ends of the 5-kΩ resistor? If these resistors are so-called 1% resistors, whose actual values are the range bounded by the nominal value ±1%, what are the limits of the output voltage produced? If the −15-V supply can also vary by ±1%, what is the range of the output voltages that might be found?

**2.19** An inverting op-amp circuit for which the required gain is −50 V/V uses an op amp whose open-loop gain is only 200 V/V. If the larger resistor used is 100 kΩ, to what must the smaller be adjusted? With what resistor must a 2-kΩ resistor connected to the input be shunted to achieved this goal? (Note that a resistor $R_a$ is said to be shunted by resistor $R_b$ when $R_b$ is placed in parallel with $R_a$.)

**D2.20** (a) Design an inverting amplifier with a closed-loop gain of −100 V/V and an input resistance of 1 kΩ.
(b) If the op amp is known to have an open-loop gain of 1000 V/V, what do you expect the closed-loop gain of your circuit to be (assuming the resistors have precise values)?
(c) Give the value of a resistor you can place in parallel (shunt) with $R_1$ to restore the closed-loop gain to its nominal value. Use the closest standard 1% resistor value (see Appendix G).

**2.21** An op amp with an open-loop gain of 1000 V/V is used in the inverting configuration. If in this application the output voltage ranges from −10 V to +10 V, what is the maximum voltage by which the "virtual ground node" departs from its ideal value?

**2.22** The circuit in Fig. P2.22 is frequently used to provide an output voltage $v_o$ proportional to an input signal current $i_i$. Derive expressions for the transresistance $R_m \equiv v_o/i_i$ and the input resistance $R_i \equiv v_i/i_i$ for the following cases:

(a) $A$ is infinite.
(b) $A$ is finite.

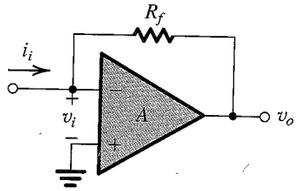



**FIGURE P2.22**

**2.23** Derive an expression for the input resistance of the inverting amplifier of Fig. 2.5 taking into account the finite open-loop gain $A$ of the op amp.

***2.24** For an inverting op amp with open-loop gain $A$ and nominal closed-loop gain $R_2/R_1$, find the minimum value the gain $A$ must have (in terms of $R_2/R_1$) for a gain error of 0.1%, 1%, and 10%. In each case, what value of resistor $R_{1a}$ can be used to shunt $R_1$ to achieve the nominal result?

***2.25** Figure P2.25 shows an op amp that is ideal except for having a finite open-loop gain and is used to realize an inverting amplifier whose gain has a nominal magnitude $G = R_2/R_1$. To compensate for the gain reduction due to the finite $A$, a resistor $R_c$ is shunted across $R_1$. Show that perfect compensation is achieved when $R_c$ is selected according to

$$\frac{R_c}{R_1} = \frac{A-G}{1+G}$$

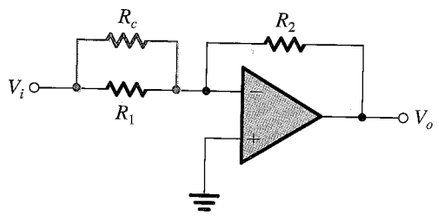



**FIGURE P2.25**

***2.26** Rearrange Eq. (2.5) to give the amplifier open-loop gain $A$ required to realize a specified closed-loop gain ($G_{\text{nominal}} = -R_2/R_1$) within a specified gain error $\varepsilon$,

$$\varepsilon \equiv \left|\frac{G - G_{\text{nominal}}}{G_{\text{nominal}}}\right|$$

For a closed-loop gain of −100 and a gain error of ≤10%, what is the minimum $A$ required?

***2.27** Using Eq. (2.5), determine the value of $A$ for which a reduction of $A$ by $x$% results in a reduction in $|G|$ by $(x/k)$%. Find the value of $A$ required for the case in which the nominal closed-loop gain is 100, $x$ is 50, and $k$ is 100.

**2.28** Consider the circuit in Fig. 2.8 with $R_1 = R_2 = R_4 = 1$ MΩ, and assume the op amp to be ideal. Find values for $R_3$ to obtain the following gains:

(a) −10 V/V
(b) −100 V/V
(c) −2 V/V

**D2.29** An inverting op-amp circuit using an ideal op amp must be designed to have a gain of −1000 V/V using resistors no larger than 100 kΩ.

(a) For the simple two-resistor circuit, what input resistance would result?
(b) If the circuit in Fig. 2.8 is used with three resistors of maximum value, what input resistance results? What is the value of the smallest resistor needed?

**2.30** The inverting circuit with the T network in the feedback is redrawn in Fig. P2.30 in a way that emphasizes the observation that $R_2$ and $R_3$ in effect are in parallel (because the ideal op amp forces a virtual ground at the inverting input terminal). Use this observation to derive an expression for the gain $(v_O/v_I)$ by first finding $(v_X/v_I)$ and $(v_O/v_X)$.

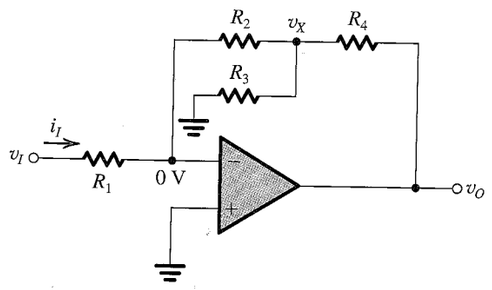



**FIGURE P2.30**

***2.31** The circuit in Fig. P2.31 can be considered an extension of the circuit in Fig. 2.8.

(a) Find the resistances looking into node 1, $R_1$; node 2, $R_2$; node 3, $R_3$; and node 4, $R_4$.
(b) Find the currents $I_1$, $I_2$, $I_3$, and $I_4$ in terms of the input current $I$.



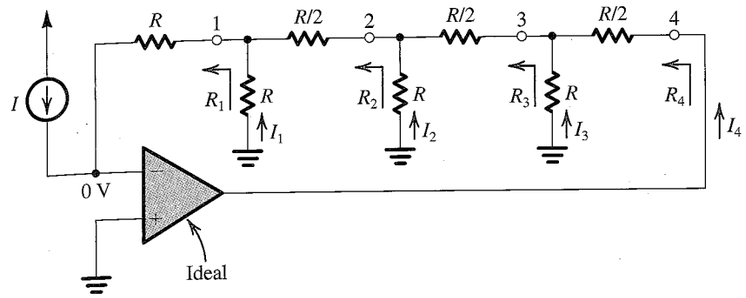



**FIGURE P2.31**

(c) Find the voltages at nodes 1, 2, 3, and 4, that is, $V_1$, $V_2$, $V_3$, and $V_4$ in terms of $(IR)$.

**2.32** The circuit in Fig. P2.32 utilizes an ideal op amp.

(a) Find $I_1$, $I_2$, $I_3$, and $V_x$.
(b) If $V_O$ is not to be lower than −13 V, find the maximum allowed value for $R_L$.
(c) If $R_L$ is varied in the range 100 Ω to 1 kΩ, what is the corresponding change in $I_L$ and in $V_O$?

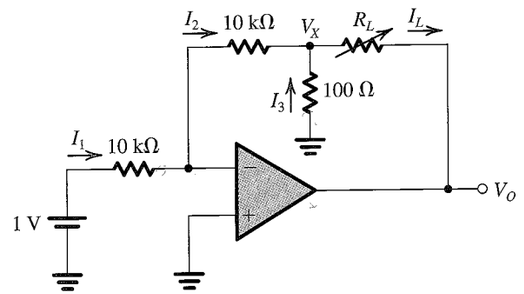



**FIGURE P2.32**

**D2.33** Assuming the op amp to be ideal, it is required to design the circuit shown in Fig. P2.33 to implement a current amplifier with gain $i_L/i_I = 20$ A/A.

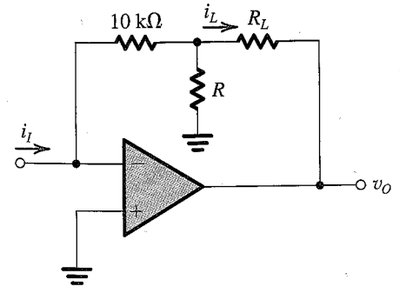



**FIGURE P2.33**

(a) Find the required value for $R$.
(b) If $R_L = 1$ kΩ and the op amp operates in an ideal manner so long as $v_O$ is in the range ±12 V. What range of $i_I$ is possible?
(c) What is the input resistance of the current amplifier? If the amplifier is fed with a current source having a current of 1 mA and a source resistance of 10 kΩ, find $i_L$.

**2.34** Figure P2.34 shows the inverting amplifier circuit of Fig. 2.8 redrawn to emphasize the fact that $R_3$ and $R_4$ can be thought of as a voltage divider connected across the output $v_O$ and from which a fraction of the output voltage (that available at node A) is fed back through $R_2$. Assuming $R_2 \gg R_3$ and thus that the loading of the feedback network can be ignored, express $v_A$ as a function of $v_O$. Now express $v_A$ as a function of $v_I$. Use these two relationships to find the (approximate) relationship between $v_O$ and $v_I$. With appropriate manipulation, compare it with the result obtained in Example 2.2. Show that the exact result can be obtained by noting that $R_2$ appears in effect across $R_3$ and, thus, that the voltage divider is composed of $R_4$ and $(R_3 \parallel R_2)$.

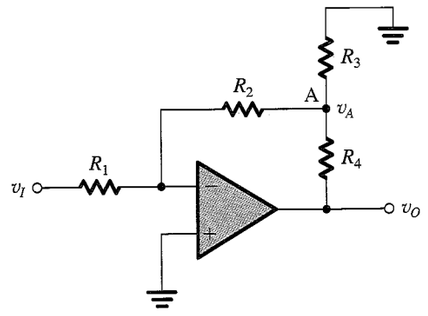



**FIGURE P2.34**

**D2.35** Design the circuit shown in Fig. P2.35 to have an input resistance of 100 kΩ and a gain that can be varied from −1 V/V to −10 V/V using the 10-kΩ potentiometer $R_4$. What

voltage gain results when the potentiometer is set exactly at its middle value?

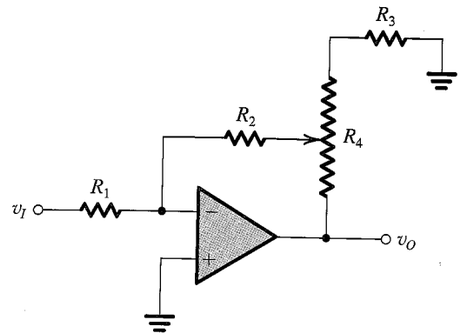



**FIGURE P2.35**

**2.36** A weighted summer circuit using an ideal op amp has three inputs using 100-kΩ resistors and a feedback resistor of 50 kΩ. A signal $v_1$ is connected to two of the inputs while a signal $v_2$ is connected to the third. Express $v_O$ in terms of $v_1$ and $v_2$. If $v_1 = 3$ V and $v_2 = -3$ V, what is $v_O$?

**D2.37** Design an op amp circuit to provide an output $v_O = -[4v_1 + (v_2/3)]$. Choose relatively low values of resistors but ones for which the input current (from each input signal source) does not exceed 0.1 mA for 1-V input signals.

**D2.38** Using the scheme illustrated in Fig. 2.10, design an op-amp circuit with inputs $v_1$, $v_2$, and $v_3$ whose output is $v_O = -(2v_1 + 4v_2 + 8v_3)$ using small resistors but no smaller than 10 kΩ.

**D2.39** An ideal op amp is connected in the weighted summer configuration of Fig. 2.10. The feedback resistor $R_f$ = 10 kΩ, and six 10-kΩ resistors are connected to the inverting input terminal of the op amp. Show, by sketching the various circuit configurations, how this basic circuit can be used to implement the following functions:

(a) $v_O = -(v_1 + 2v_2 + 3v_3)$
(b) $v_O = -(v_1 + v_2 + 2v_3 + 2v_4)$
(c) $v_O = -(v_1 + 5v_2)$
(d) $v_O = -6v_1$

In each case find the input resistance seen by each of the signal sources supplying $v_1$, $v_2$, $v_3$, and $v_4$. Suggest at least two additional summing functions that you can realize with this circuit. How would you realize a summing coefficient that is 0.5?

**D2.40** Give a circuit, complete with component values, for a weighted summer that shifts the dc level of a sine-wave signal of 5 sin($\omega t$) V from zero to −5 V. Assume that in addition to the sine-wave signal you have a dc reference voltage of 2 V available. Sketch the output signal waveform.

**D2.41** Use two ideal op amps and resistors to implement the summing function.

$$v_O = v_1 + 2v_2 - 3v_3 - 4v_4$$

**D*2.42** In an instrumentation system, there is a need to take the difference between two signals, one of $v_1 = 3\sin(2\pi \times 60t) + 0.01\sin(2\pi \times 1000t)$, volts and another of $v_2 = 3\sin(2\pi \times 60t) - 0.01\sin(2\pi \times 1000t)$ volts. Draw a circuit that finds the required difference using two op amps and mainly 10-kΩ resistors. Since it is desirable to amplify the 1000-Hz component in the process, arrange to provide an overall gain of 10 as well. The op amps available are ideal except that their output voltage swing is limited to ±10 V.

***2.43** Figure P2.43 shows a circuit for a digital-to-analog converter (DAC). The circuit accepts a 4-bit input binary word $a_3a_2a_1a_0$, where $a_0$, $a_1$, $a_2$, and $a_3$ take the values of 0 or 1, and it provides an analog output voltage $v_O$ proportional to the value of the digital input. Each of the bits of the input word controls the correspondingly numbered switch. For instance, if $a_2$ is 0 then switch $S_2$ connects the 20-kΩ resistor to ground, while if $a_2$ is 1 then $S_2$ connects the 20-kΩ resistor to the +5-V power supply. Show that $v_O$ is given by

$$v_O = -\frac{R_f}{16}[2^0a_0 + 2^1a_1 + 2^2a_2 + 2^3a_3]$$

where $R_f$ is in kΩ. Find the value of $R_f$ so that $v_O$ ranges from 0 to −12 volts.

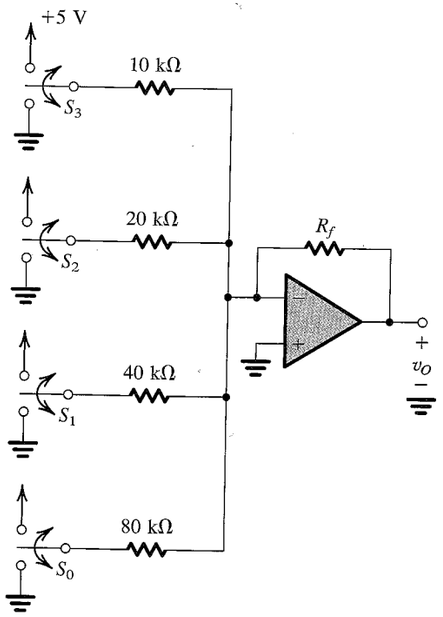



**FIGURE P2.43**



## SECTION 2.3: THE NONINVERTING CONFIGURATION

**D2.44** Using an ideal op amp to implement designs for the following closed-loop gains, what values of resistors ($R_1$, $R_2$) should be used? Where possible, use at least one 10-kΩ resistor as the smallest resistor in your design.

(a) +1 V/V
(b) +2 V/V
(c) +101 V/V
(d) +100 V/V

**D2.45** Design a circuit based on the topology of the noninverting amplifier to obtain a gain of +1.5 V/V, using only 10-kΩ resistors. Note that there are two possibilities. Which of these can be easily converted to have a gain of either +1.0 V/V or +2.0 V/V simply by short-circuiting a single resistor in each case?

**D2.46** Figure P2.46 shows a circuit for an analog voltmeter of very high input resistance that uses an inexpensive moving-coil meter. The voltmeter measures the voltage $V$ applied between the op amp's positive-input terminal and ground. Assuming that the moving coil produces full-scale deflection when the current passing through it is 100 μA, find the value of $R$ such that full-scale reading is obtained when $V$ is +10 V. Does the meter resistance shown affect the voltmeter calibration?

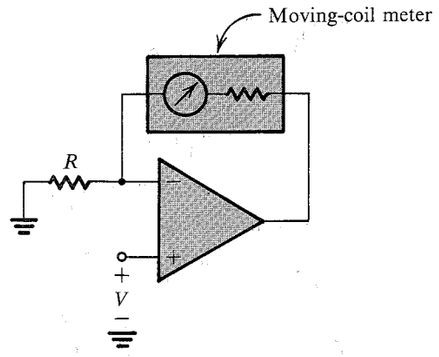



**FIGURE P2.46**

**D*2.47** (a) Use superposition to show that the output of the circuit in Fig. P2.47 is given by

$$v_O = -\left[\frac{R_f}{R_{N1}}v_{N1} + \frac{R_f}{R_{N2}}v_{N2} + \cdots + \frac{R_f}{R_{Nn}}v_{Nn}\right] + \left[1 + \frac{R_f}{R_N}\right]\left[\frac{R_P}{R_{P1}}v_{P1} + \frac{R_P}{R_{P2}}v_{P2} + \cdots + \frac{R_P}{R_{Pn}}v_{Pn}\right]$$

where $R_N = R_{N1}//R_{N2}// \cdots //R_{Nn}$ and
$R_P = R_{P1}//R_{P2}// \cdots //R_{Pn}//R_{P0}$

(b) Design a circuit to obtain

$$v_O = -2v_{N1} + v_{P1} + 2v_{P2}$$

The smallest resistor used should be 10 kΩ.

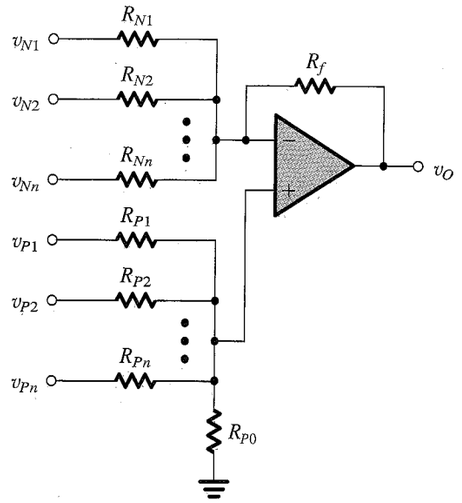



**FIGURE P2.47**

**D2.48** Design a circuit, using one ideal op amp, whose output is $v_O = v_{I1} + 3v_{I2} - 2(v_{I3} + 3v_{I4})$. (*Hint:* Use a structure similar to that shown in general form in Fig. P2.47.)

**2.49** Derive an expression for the voltage gain, $v_O/v_I$, of the circuit in Fig. P2.49.

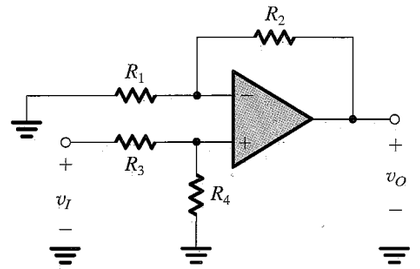



**FIGURE P2.49**

**2.50** For the circuit in Fig. P2.50, use superposition to find $v_O$ in terms of the input voltages $v_1$ and $v_2$. Assume an ideal op amp. For

$v_1 = 10\sin(2\pi \times 60t) - 0.1\sin(2\pi \times 1000t)$, volts
$v_2 = 10\sin(2\pi \times 60t) + 0.1\sin(2\pi \times 1000t)$, volts

find $v_O$.

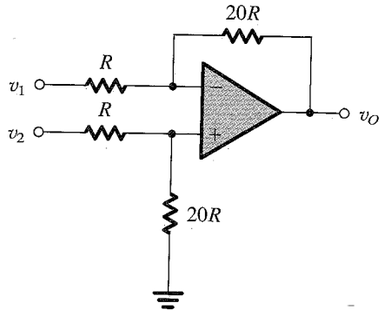



**FIGURE P2.50**

**D2.51** The circuit shown in Fig. P2.51 utilizes a 10-kΩ potentiometer to realize an adjustable-gain amplifier. Derive an expression for the gain as a function of the potentiometer setting $x$. Assume the op amp to be ideal. What is the range of gains obtained? Show how to add a fixed resistor so that the gain range can be 1 to 21 V/V. What should the resistor value be?

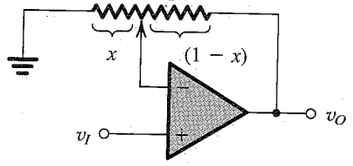



**FIGURE P2.51**

**D2.52** Given the availability of resistors of value 1 kΩ and 10 kΩ only, design a circuit based on the noninverting configuration to realize a gain of +10 V/V.

**2.53** It is required to connect a 10-V source with a source resistance of 100 kΩ to a 1-kΩ load. Find the voltage that will appear across the load if:

(a) The source is connected directly to the load.
(b) A unity-gain op-amp buffer is inserted between the source and the load.

In each case find the load current and the current supplied by the source. Where does the load current come from in case (b)?

**2.54** Derive an expression for the gain of the voltage follower of Fig. 2.14 assuming the op amp to be ideal except for having a finite gain $A$. Calculate the value of the closed-loop gain for $A = 1000$, 100, and 10. In each case find the percentage error in gain magnitude from the nominal value of unity.

**2.55** Complete the following table for feedback amplifiers created using one ideal op amp. Note that $R_{in}$ signifies input resistance and $R_1$ and $R_2$ are feedback-network resistors as labelled in the inverting and noninverting configurations.

| Case | Gain | $R_{in}$ | $R_1$ | $R_2$ |
|---|---|---|---|---|
| a | −10 V/V | 10 kΩ | | |
| b | −1 V/V | | 100 kΩ | |
| c | −2 V/V | | | 100 kΩ |
| d | +1 V/V | ∞ | | |
| e | +2 V/V | | 10 kΩ | |
| f | +11 V/V | | | 100 kΩ |
| g | −0.5 V/V | 10 kΩ | | |

**D2.56** A noninverting op-amp circuit with nominal gain of 10 V/V uses an op amp with open-loop gain of 50 V/V and a lowest-value resistor of 10 kΩ. What closed-loop gain actually results? With what value resistor can which resistor be shunted to achieve the nominal gain? If in the manufacturing process, an op amp of gain 100 V/V were used, what closed-loop gain would result in each case (the uncompensated one, and the compensated one)?

**2.57** Using Eq. (2.11), show that if the reduction in the closed-loop gain $G$ from the nominal value $G_0 = 1 + R_2/R_1$ is to be kept less than $x\%$ of $G_0$, then the open-loop gain of the op amp must exceed $G_0$ by at least a factor $F = (100/x) - 1 \simeq 100/x$. Find the required $F$ for $x = 0.01$, 0.1, 1, and 10. Utilize these results to find for each value of $x$ the minimum required open-loop gain to obtain closed-loop gains of 1, 10, $10^2$, $10^3$, and $10^4$ V/V.

**2.58** For each of the following combinations of op-amp open-loop gain $A$ and nominal closed-loop gain $G_0$, calculate the actual closed-loop gain $G$ that is achieved. Also, calculate the percentage by which $|G|$ falls short of the nominal gain magnitude $|G_0|$.

| Case | $G_0$ (V/V) | $A$ (V/V) |
|---|---|---|
| a | −1 | 10 |
| b | +1 | 10 |
| c | −1 | 100 |
| d | +10 | 10 |
| e | −10 | 100 |
| f | −10 | 1000 |
| g | +1 | 2 |

**2.59** Figure P2.59 shows a circuit that provides an output voltage $v_O$ whose value can be varied by turning the wiper of the 100-kΩ potentiometer. Find the range over which $v_O$ can be varied. If the potentiometer is a "20-turn" device, find the change in $v_O$ corresponding to each turn of the pot.



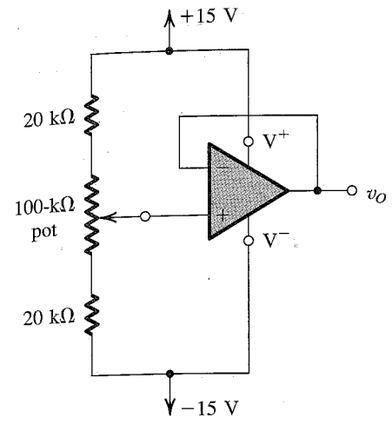



**FIGURE P2.59**

## SECTION 2.4: DIFFERENCE AMPLIFIERS

**2.60** Find the voltage gain $v_O/v_{Id}$ for the difference amplifier of Fig. 2.16 for the case $R_1 = R_3 = 10$ kΩ and $R_2 = R_4 = 100$ kΩ. What is the differential input resistance $R_{id}$? If the two key resistance ratios $(R_2/R_1)$ and $(R_4/R_3)$ are different from each other by 1%, what do you expect the common-mode gain $A_{cm}$ to be? Also, find the CMRR in this case.

**D2.61** Using the difference amplifier configuration of Fig. 2.16 and assuming an ideal op-amp, design the circuit to provide the following differential gains. In each case the differential input resistance should be 20 kΩ.

(a) 1 V/V
(b) 2 V/V
(c) 100 V/V
(d) 0.5 V/V

**2.62** For the circuit shown in Fig. P2.62, express $v_O$ as a function of $v_1$ and $v_2$. What is the input resistance seen by $v_1$ alone? By $v_2$ alone? By a source connected between the two input terminals? By a source connected to both input terminals simultaneously?

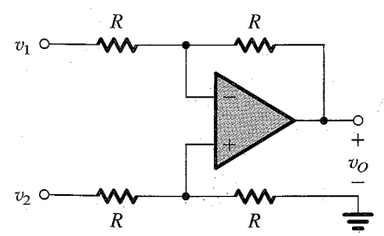



**FIGURE P2.62**

**2.63** Consider the difference amplifier of Fig. 2.16 with the two input terminals connected together to an input common-mode signal source. For $R_2/R_1 = R_4/R_3$, show that the input common-mode resistance is $(R_3 + R_4) \| (R_1 + R_2)$.

**2.64** Consider the circuit of Fig. 2.16, and let each of the $v_{I1}$ and $v_{I2}$ signal sources have a series resistance $R_s$. What condition must apply in addition to the condition in Eq. (2.15) in order for the amplifier to function as an ideal difference amplifier?

***2.65** For the difference amplifier shown in Fig. P2.62, let all the resistors be 100 kΩ ± $x$%. Find an expression for the worst-case common-mode gain that results. Evaluate this for $x$ = 0.1, 1, and 5. Also, evaluate the resulting CMRR in each case.

**2.66** For the difference amplifier of Fig. 2.16, show that if each resistor has a tolerance of ±100 $\varepsilon$% (i.e., for, say, a 5% resistor, $\varepsilon = 0.05$) then the worst-case CMRR is given approximately by

$$\text{CMRR} \cong 20 \log\left[\frac{K+1}{4\varepsilon}\right]$$

where $K$ is the nominal (ideal) value of the ratios $(R_2/R_1)$ and $(R_4/R_3)$. Calculate the value of worst-case CMRR for an amplifier designed to have a differential gain of ideally 100 V/V, assuming that the op amp is ideal and that 1% resistors are used.

**D*2.67** Design the difference amplifier circuit of Fig. 2.16 to realize a differential gain of 100, a differential input resistance of 20 kΩ, and a minimum CMRR of 80 dB. Assume the op amp to be ideal. Specify both the resistor values and their required tolerance (e.g., better than $x$%).

***2.68** (a) Find $A_d$ and $A_{cm}$ for the difference amplifier circuit shown in Fig. P2.68.
(b) If the op amp is specified to operate properly so long as the common-mode voltage at its positive and negative inputs falls in the range ±2.5 V, what is the corresponding limitation on the range of the input common-mode signal $v_{Icm}$? (This is known as the **common-mode range** of the differential amplifier).
(c) The circuit is modified by connecting a 10-kΩ resistor between node A and ground and another 10-kΩ resistor between node B and ground. What will now be the values of $A_d$, $A_{cm}$, and the input common-mode range?

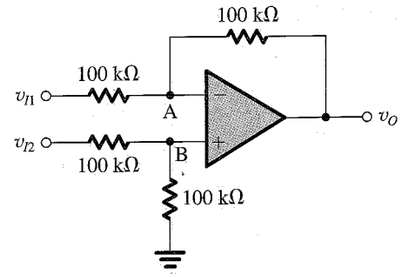



**FIGURE P2.68**

****2.69** To obtain a high-gain, high-input-resistance difference amplifier the circuit in Fig. P2.69 employs positive feedback, in addition to the negative feedback provided by the resistor $R$ connected from the output to the negative input of the op amp. Specifically, a voltage divider ($R_5$, $R_6$) connected across the output feeds a fraction $\beta$ of the output, that is, a voltage $\beta v_O$, back to the positive-input terminal of the op amp through a resistor $R$. Assume that $R_5$ and $R_6$ are much smaller than $R$ so that the current through $R$ is much lower than the current in the voltage divider, with the result that $\beta \cong R_6/(R_5 + R_6)$. Show that the differential gain is given by

$$A_d \equiv \frac{v_O}{v_{Id}} = \frac{1}{1-\beta}$$

Design the circuit to obtain a differential gain of 10 V/V and differential input resistance of 2 MΩ. Select values for $R$, $R_5$, and $R_6$ such that $(R_5 + R_6) \le R/100$.

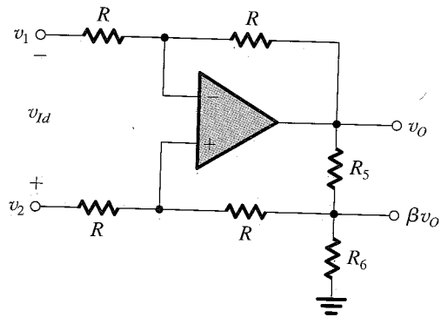



**FIGURE P2.69**

***2.70** Figure P2.70 shows a modified version of the difference amplifier. The modified circuit includes a resistor $R_G$, which can be used to vary the gain. Show that the differential voltage gain is given by

$$\frac{v_O}{v_{Id}} = -2\frac{R_2}{R_1}\left[1 + \frac{R_2}{R_G}\right]$$

(*Hint:* The virtual short circuit at the op amp input causes the current through the $R_1$ resistors to be $v_{Id}/2R_1$.)

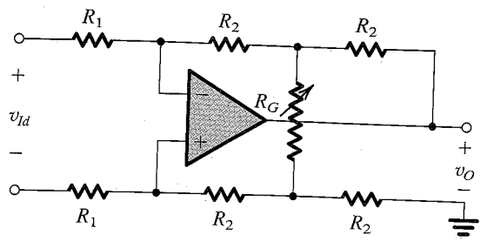



**FIGURE P2.70**

**D*2.71** The circuit shown in Fig. P2.71 is a representation of a versatile, commercially available IC, the INA105, manufactured by Burr-Brown and known as a differential amplifier module. It consists of an op amp and precision, laser-trimmed, metal-film resistors. The circuit can be configured for a variety of applications by the appropriate connection of terminals A, B, C, D, and O.

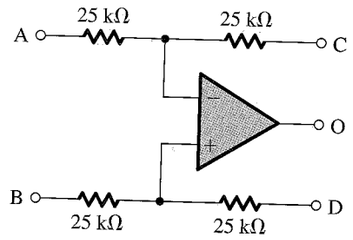



**FIGURE P2.71**

(a) Show how the circuit can be used to implement a difference amplifier of unity gain.
(b) Show how the circuit can be used to implement single-ended amplifiers with gains:

(i) −1 V/V
(ii) +1 V/V
(iii) +2 V/V
(iv) +1/2 V/V

Avoid leaving a terminal open-circuited, for such a terminal may act as an "antenna," picking up interference and noise through capacitive coupling. Rather, find a convenient node to connect such a terminal in a redundant way. When more than one circuit implementation is possible, comment on the relative merits of each, taking into account such considerations as dependence on component matching and input resistance.

**2.72** Consider the instrumentation amplifier of Fig. 2.20(b) with a common-mode input voltage of +3 V (dc) and a differential input signal of 80-mV peak sine wave. Let $2R_1 = 1$ kΩ, $R_2 = 50$ kΩ, $R_3 = R_4 = 10$ kΩ. Find the voltage at every node in the circuit.

**2.73** (a) Consider the instrumentation amplifier circuit of Fig. 2.20(a). If the op amps are ideal except that their outputs saturate at ±14 V, in the manner shown in Fig. 1.13, find the maximum allowed input common-mode signal for the case $R_1 = 1$ kΩ and $R_2 = 100$ kΩ.
(b) Repeat (a) for the circuit in Fig. 2.20(b), and comment on the difference between the two circuits.

**2.74** (a) Expressing $v_{I1}$ and $v_{I2}$ in terms of differential and common-mode components, find $v_{O1}$ and $v_{O2}$ in the circuit in Fig. 2.20(a) and hence find their differential component $v_{O2} - v_{O1}$ and their common-mode component $\frac{1}{2}(v_{O1} + v_{O2})$. Now find the differential gain and the common-mode gain of the first stage of this instrumentation amplifier and hence the CMRR.
(b) Repeat for the circuit in Fig. 2.20(b), and comment on the difference between the two circuits.



****2.75** For an instrumentation amplifier of the type shown in Fig. 2.20(b), a designer proposes to make $R_2 = R_3 = R_4 = 100$ kΩ, and $2R_1 = 10$ kΩ. For ideal components, what difference-mode gain, common-mode gain, and CMRR result? Reevaluate the worst-case values for these for the situation in which all resistors are specified as ±1% units. Repeat the latter analysis for the case in which $2R_1$ is reduced to 1 kΩ. What do you conclude about the importance of the relative difference gains of the first and second stages?

**D2.76** Design the instrumentation-amplifier circuit of Fig. 2.20(b) to realize a differential gain, variable in the range 1 to 100, utilizing a 100-kΩ pot as variable resistor. (*Hint:* Design the second stage for a gain of 0.5.)

***2.77** The circuit shown in Fig. P2.77 is intended to supply a voltage to floating loads (those for which both terminals are ungrounded) while making greatest possible use of the available power supply.

(a) Assuming ideal op amps, sketch the voltage waveforms at nodes B and C for a 1-V peak-to-peak sine wave applied at A. Also sketch $v_O$.
(b) What is the voltage gain $v_O/v_I$?
(c) Assuming that the op amps operate from ±15-V power supplies and that their output saturates at ±14 V (in the manner shown in Fig. 1.13), what is the largest sine wave output that can be accommodated? Specify both its peak-to-peak and rms values.

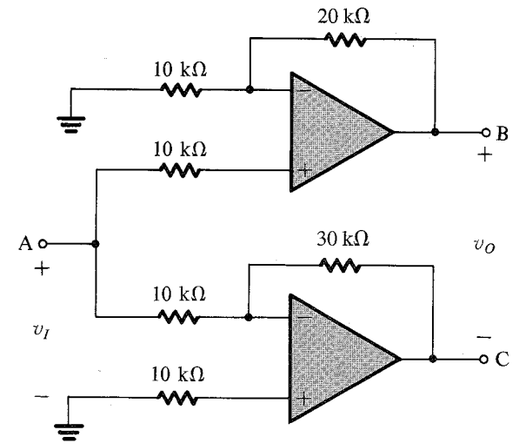



**FIGURE P2.77**

***2.78** The two circuits in Fig. P2.78 are intended to function as voltage-to-current converters; that is, they supply the load impedance $Z_L$ with a current proportional to $v_I$ and independent of the value of $Z_L$. Show that this is indeed the case, and find for each circuit $i_O$ as a function of $v_I$. Comment on the differences between the two circuits.

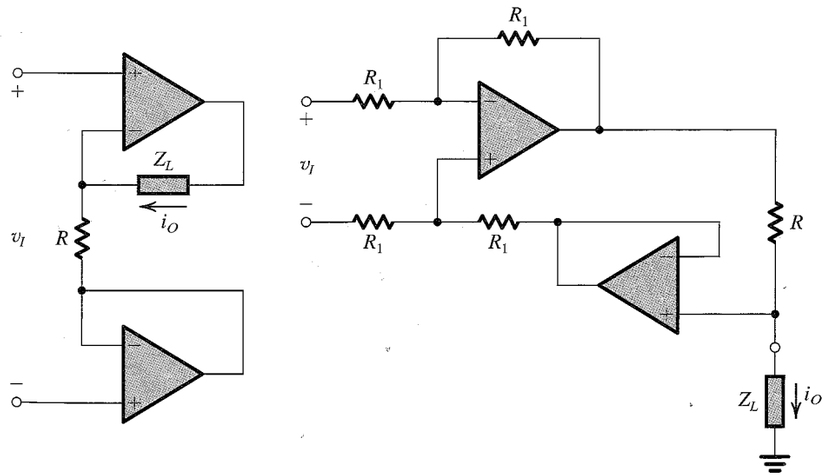



**FIGURE P2.78**

## SECTION 2.5: EFFECT OF FINITE OPEN-LOOP GAIN AND BANDWIDTH ON CIRCUIT PERFORMANCE

**2.79** The data in the following table apply to internally compensated op amps. Fill in the blank entries.

| $A_0$ | $f_b$ (Hz) | $f_t$ (Hz) |
|---|---|---|
| $10^5$ | $10^2$ | |
| $10^6$ | | $10^6$ |
| | $10^3$ | $10^8$ |
| | $10^{-1}$ | $10^6$ |
| $2 \times 10^5$ | 10 | |

**2.80** A measurement of the open-loop gain of an internally compensated op amp at very low frequencies shows it to be 86 dB; at 100 kHz, this shows it is 40 dB. Estimate values for $A_0$, $f_b$, and $f_t$.

**2.81** Measurements of the open-loop gain of a compensated op amp intended for high-frequency operation indicate that the gain is $5.1 \times 10^3$ at 100 kHz and $8.3 \times 10^3$ at 10 kHz. Estimate its 3-dB frequency, its unity-gain frequency, and its dc gain.

**2.82** Measurements made on the internally compensated amplifiers listed below provide the dc gain and the frequency at which the gain has dropped by 20 dB. For each, what are the 3 dB and unity-gain frequencies?

(a) $3 \times 10^5$ V/V and $6 \times 10^2$ Hz
(b) $50 \times 10^5$ V/V and 10 Hz
(c) 1500 V/V and 0.1 MHz
(d) 100 V/V and 0.1 GHz
(e) 25 V/mV and 25 kHz

**2.83** An inverting amplifier with nominal gain of −20 V/V employs an op amp having a dc gain of $10^4$ and a unity-gain frequency of $10^6$ Hz. What is the 3-dB frequency $f_{3dB}$ of the closed-loop amplifier? What is its gain at $0.1 f_{3dB}$ and at $10 f_{3dB}$?

**2.84** A particular op amp, characterized by a gain–bandwidth product of 20 MHz, is operated with a closed-loop gain of +100 V/V. What 3-dB bandwidth results? At what frequency does the closed-loop amplifier exhibit a −6° phase shift? A −84° phase shift?

**2.85** Find the $f_t$ required for internally compensated op amps to be used in the implementation of closed-loop amplifiers with the following nominal dc gains and 3-dB bandwidths:

(a) −100 V/V; 100 kHz
(b) +100 V/V; 100 kHz
(c) +2 V/V; 10 MHz
(d) −2 V/V; 10 MHz
(e) −1000 V/V; 20 kHz
(f) +1 V/V; 1 MHz
(g) −1 V/V; 1 MHz

**2.86** A noninverting op-amp circuit with a gain of 100 V/V is found to have a 3-dB frequency of 8 kHz. For a particular system application, a bandwidth of 20 kHz is required. What is the highest gain available under these conditions?

**2.87** Consider a unity-gain follower utilizing an internally compensated op amp with $f_t = 1$ MHz. What is the 3-dB frequency of the follower? At what frequency is the gain of the follower 1% below its low-frequency magnitude? If the input to the follower is a 1-V step, find the 10% to 90% rise time of the output voltage. (*Note:* The step response of STC low-pass networks is discussed in Appendix D.)

**D*2.88** It is required to design a noninverting amplifier with a dc gain of 10. When a step voltage of 100 mV is applied at the input, it is required that the output be within 1% of its final value of 1 V in at most 100 ns. What must the $f_t$ of the op amp be? (*Note:* The step response of STC low-pass networks is discussed in Appendix D.)

**D*2.89** This problem illustrates the use of cascaded closed-loop amplifiers to obtain an overall bandwidth greater than can be achieved using a single-stage amplifier with the same overall gain.

(a) Show that cascading two identical amplifier stages, each having a low-pass STC frequency response with a 3-dB frequency $f_1$, results in an overall amplifier with a 3-dB frequency given by

$$f_{3dB} = \sqrt{\sqrt{2} - 1}\, f_1$$

(b) It is required to design a noninverting amplifier with a dc gain of 40 dB utilizing a single internally-compensated op amp with $f_t = 1$ MHz. What is the 3-dB frequency obtained?
(c) Redesign the amplifier of (b) by cascading two identical noninverting amplifiers each with a dc gain of 20 dB. What is the 3-dB frequency of the overall amplifier? Compare this to the value obtained in (b) above.

**D**2.90** A designer, wanting to achieve a stable gain of 100 V/V at 5 MHz, considers her choice of amplifier topologies. What unity-gain frequency would a single operational amplifier require to satisfy her need? Unfortunately, the best available amplifier has an $f_t$ of 40 MHz. How many such amplifiers connected in a cascade of identical noninverting stages would she need to achieve her goal? What is the 3-dB frequency of each stage she can use? What is the overall 3-dB frequency?

**2.91** Consider the use of an op amp with a unity-gain frequency $f_t$ in the realization of

(a) an inverting amplifier with dc gain of magnitude $K$.
(b) a noninverting amplifier with a dc gain of $K$.

In each case find the 3-dB frequency and the gain-bandwidth product (GBP ≡ |Gain| × $f_{3dB}$). Comment on the results.



***2.92** Consider an inverting summer with two inputs $V_1$ and $V_2$ and with $V_o = -(V_1 + V_2)$. Find the 3-dB frequency of each of the gain functions $V_o/V_1$ and $V_o/V_2$ in terms of the op amp $f_t$. (*Hint:* In each case, the other input to the summer can be set to zero—an application of superposition.)

## SECTION 2.6: LARGE-SIGNAL OPERATION OF OP AMPS

**2.93** A particular op amp using ±15-V supplies operates linearly for outputs in the range −12 V to +12 V. If used in an inverting amplifier configuration of gain −100, what is the rms value of the largest possible sine wave that can be applied at the input without output clipping?

**2.94** Consider an op amp connected in the inverting configuration to realize a closed-loop gain of −100 V/V utilizing resistors of 1 kΩ and 100 kΩ. A load resistance $R_L$ is connected from the output to ground, and a low-frequency sine-wave signal of peak amplitude $V_p$ is applied to the input. Let the op amp be ideal except that its output voltage saturates at ±10 V and its output current is limited to the range ±20 mA.

(a) For $R_L = 1$ kΩ, what is the maximum possible value of $V_p$ while an undistorted output sinusoid is obtained?
(b) Repeat (a) for $R_L = 100$ Ω.
(c) If it is desired to obtain an output sinusoid of 10-V peak amplitude, what minimum value of $R_L$ is allowed?

**2.95** An op amp having a slew rate of 20 V/μs is to be used in the unity-gain follower configuration, with input pulses that rise from 0 to 3 V. What is the shortest pulse that can be used while ensuring full-amplitude output? For such a pulse, describe the output resulting.

***2.96** For operation with 10-V output pulses with the requirement that the sum of the rise and fall times should represent only 20% of the pulse width (at half amplitude), what is the slew-rate requirement for an op amp to handle pulses 2 μs wide? (*Note:* The rise and fall times of a pulse signal are usually measured between the 10%- and 90%-height points.)

**2.97** What is the highest frequency of a triangle wave of 20-V peak-to-peak amplitude that can be reproduced by an op amp whose slew rate is 10 V/μs? For a sine wave of the same frequency, what is the maximum amplitude of output signal that remains undistorted?

**2.98** For an amplifier having a slew rate of 60 V/μs, what is the highest frequency at which a 20-V peak-to-peak sine wave can be produced at the output?

**D*2.99** In designing with op amps one has to check the limitations on the voltage and frequency ranges of operation of the closed-loop amplifier, imposed by the op amp finite bandwidth ($f_t$), slew rate (SR), and output saturation ($V_{omax}$). This problem illustrates the point by considering the use of an op amp with $f_t = 2$ MHz, SR = 1 V/μs, and $V_{omax} = 10$ V in the design of a noninverting amplifier with a nominal gain of 10. Assume a sine-wave input with peak amplitude $V_i$.

(a) If $V_i = 0.5$ V, what is the maximum frequency before the output distorts?
(b) If $f = 20$ kHz, what is the maximum value of $V_i$ before the output distorts?
(c) If $V_i = 50$ mV, what is the useful frequency range of operation?
(d) If $f = 5$ kHz, what is the useful input voltage range?

## SECTION 2.7: DC IMPERFECTIONS

**2.100** An op amp wired in the inverting configuration with the input grounded, having $R_2 = 100$ kΩ and $R_1 = 1$ kΩ, has an output dc voltage of −0.3 V. If the input bias current is known to be very small, find the input offset voltage.

**2.101** A noninverting amplifier with a gain of 200 uses an op amp having an input offset voltage of ±2 mV. Find the output when the input is 0.01 sin $\omega t$, volts.

**2.102** A noninverting amplifier with a closed-loop gain of 1000 is designed using an op amp having an input offset voltage of 3 mV and output saturation levels of ±13 V. What is the maximum amplitude of the sine wave that can be applied at the input without the output clipping? If the amplifier is capacitively coupled in the manner indicated in Fig. 2.36, what would the maximum possible amplitude be?

**2.103** An op amp connected in a closed-loop inverting configuration having a gain of 1000 V/V and using relatively small-valued resistors is measured with input grounded to have a dc output voltage of −1.4 V. What is its input offset voltage? Prepare an offset-voltage-source sketch resembling that in Fig. 2.28. Be careful of polarities.

**2.104** A particular inverting amplifier with nominal gain of −100 V/V uses an imperfect op amp in conjunction with 100-kΩ and 10-MΩ resistors. The output voltage is found to be +9.31 V when measured with the input open and +9.09 V with the input grounded.

(a) What is the bias current of this amplifier? In what direction does it flow?
(b) Estimate the value of the input offset voltage.
(c) A 10-MΩ resistor is connected between the positive-input terminal and ground. With the input left floating (disconnected), the output dc voltage is measured to be −0.8 V. Estimate the input offset current.

**D*2.105** A noninverting amplifier with a gain of +10 V/V using 100 kΩ as the feedback resistor operates from a 5-kΩ source. For an amplifier offset voltage of 0 mV, but with a

bias current of 1 $\mu$A and an offset current of 0.1 $\mu$A, what range of outputs would you expect? Indicate where you would add an additional resistor to compensate for the bias currents. What does the range of possible outputs then become? A designer wishes to use this amplifier with a 15-k$\Omega$ source. In order to compensate for the bias current in this case, what resistor would you use? And where?

**D2.106** The circuit of Fig. 2.36 is used to create an ac-coupled noninverting amplifier with a gain of 200 V/V using resistors no larger than 100 k$\Omega$. What values of $R_1$, $R_2$, and $R_3$ should be used? For a break frequency due to $C_1$ at 100 Hz, and that due to $C_2$ at 10 Hz, what values of $C_1$ and $C_2$ are needed?

***2.107** Consider the difference amplifier circuit in Fig. 2.16. Let $R_1 = R_3 = 10$ k$\Omega$ and $R_2 = R_4 = 1$ M$\Omega$. If the op amp has $V_{OS} = 4$ mV, $I_B = 0.3$ $\mu$A, and $I_{OS} = 50$ nA, find the worst-case (largest) dc offset voltage at the output.

***2.108** The circuit shown in Fig. P2.108 uses an op amp having a ±4-mV offset. What is its output offset voltage? What does the output offset become with the input ac coupled through a capacitor $C$? If, instead, the 1-k$\Omega$ resistor is capacitively coupled to ground, what does the output offset become?

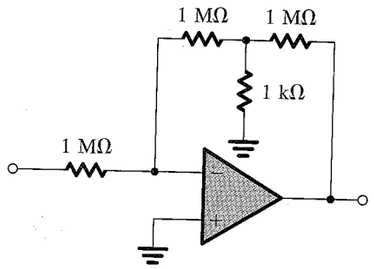



**FIGURE P2.108**

**2.109** Using offset-nulling facilities provided for the op amp, a closed-loop amplifier with gain of +1000 is adjusted at 25°C to produce zero output with the input grounded. If the input offset-voltage drift of the op amp is specified to be 10 $\mu$V/°C, what output would you expect at 0°C and at 75°C? While nothing can be said separately about the polarity of the output offset at either 0 or 75°C, what would you expect their relative polarities to be?

**2.110** An op amp is connected in a closed loop with gain of +100 utilizing a feedback resistor of 1 M$\Omega$.

(a) If the input bias current is 100 nA, what output voltage results with the input grounded?
(b) If the input offset voltage is ±1 mV and the input bias current as in (a), what is the largest possible output that can be observed with the input grounded?
(c) If bias-current compensation is used, what is the value of the required resistor? If the offset current is no more than one-tenth the bias current, what is the resulting output offset voltage (due to offset current alone)?
(d) With bias-current compensation as in (c) in place what is the largest dc voltage at the output due to the combined effect of offset voltage and offset current?

***2.111** An op amp intended for operation with a closed-loop gain of –100 V/V uses feedback resistors of 10 k$\Omega$ and 1 M$\Omega$ with a bias-current-compensation resistor $R_3$. What should the value of $R_3$ be? With input grounded, the output offset voltage is found to be +0.21 V. Estimate the input offset current assuming zero input offset voltage. If the input offset voltage can be as large as 1 mV of unknown polarity, what range of offset current is possible? What current injected into, or extracted from, the nongrounded end of $R_3$ would reduce the op amp output voltage to zero? For available ±15-V supplies, what resistor and supply voltage would you use?

## SECTION 2.8: INTEGRATORS AND DIFFERENTIATORS

**2.112** A Miller integrator incorporates an ideal op amp, a resistor $R$ of 100 k$\Omega$, and a capacitor $C$ of 10 nF. A sine-wave signal is applied to its input.

(a) At what frequency (in Hz) are the input and output signals equal in amplitude?
(b) At that frequency how does the phase of the output sine wave relate to that of the input?
(c) If the frequency is lowered by a factor of 10 from that found in (a), by what factor does the output voltage change, and in what direction (smaller or larger)?
(d) What is the phase relation between the input and output in situation (c)?

**D2.113** Design a Miller integrator with a time constant of one second and an input resistance of 100 k$\Omega$. For a dc voltage of –1 volt applied at the input at time 0, at which moment $v_O = -10$ V, how long does it take the output to reach 0 V? +10 V?

**2.114** An op-amp-based inverting integrator is measured at 1 kHz to have a voltage gain of –100 V/V. At what frequency is its gain reduced to –1 V/V? What is the integrator time constant?

**D2.115** Design a Miller integrator that has a unity-gain frequency of 1 krad/s and an input resistance of 100 k$\Omega$. Sketch the output you would expect for the situation in which, with output initially at 0 V, a 2-V 2-ms pulse is applied to the input. Characterize the output that results when a sine wave 2 sin 1000$t$ is applied to the input?



**D2.116** Design a Miller integrator whose input resistance is 20 k$\Omega$ and unity-gain frequency is 10 kHz. What components are needed? For long-term stability, a feedback resistor is introduced across the capacitor, which limits the dc gain to 40 dB. What is its value? What is the associated lower 3-dB frequency? Sketch and label the output which results with a 0.1-ms, 1-V positive-input pulse (initially at 0 V) with (a) no dc stabilization (but with the output initially at 0 V) and (b) the feedback resistor connected.

***2.117** A Miller integrator whose input and output voltages are initially zero and whose time constant is 1 ms is driven by the signal shown in Fig. P2.117. Sketch and label the output waveform that results. Indicate what happens if the input levels are ±2 V, with the time constant the same (1 ms) and with the time constant raised to 2 ms.

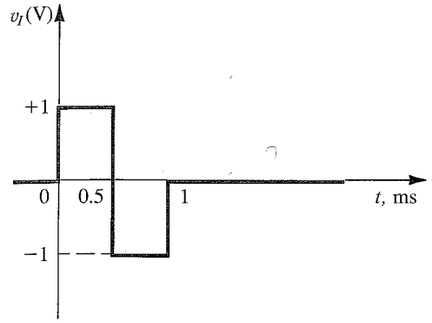



**FIGURE P2.117**

**2.118** Consider a Miller integrator having a time constant of 1 ms, and whose output is initially zero, when fed with a string of pulses of 10-$\mu$s duration and 1-V amplitude rising from 0 V (see Fig. P2.118). Sketch and label the output waveform resulting. How many pulses are required for an output voltage change of 1 V?

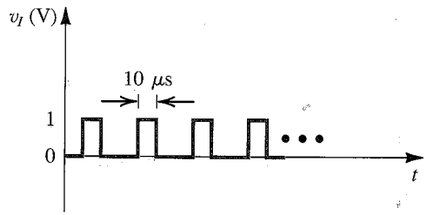



**FIGURE P2.118**

**D2.119** Figure P2.119 shows a circuit that performs a low-pass STC function. Such a circuit is known as a first-order low-pass active filter. Derive the transfer function and show that the dc gain is $(-R_2/R_1)$ and the 3-dB frequency $\omega_0 = 1/CR_2$. Design the circuit to obtain an input resistance of 1 k$\Omega$, a dc gain of 20 dB, and a 3-dB frequency of 4 kHz. At what frequency does the magnitude of the transfer function reduce to unity?

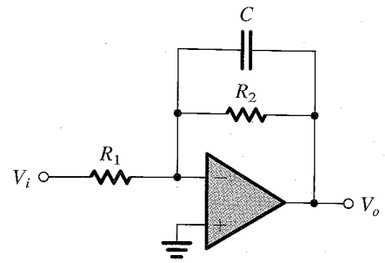



**FIGURE P2.119**

**2.120** A Miller integrator with $R = 10$ k$\Omega$ and $C = 10$ nF is implemented using an op amp with $V_{OS} = 3$ mV, $I_B = 0.1$ $\mu$A, and $I_{OS} = 10$ nA. To provide a finite dc gain, a 1-M$\Omega$ resistor is connected across the capacitor.

(a) To compensate for the effect of $I_B$, a resistor is connected in series with the positive-input terminal of the op amp. What should its value be?
(b) With the resistor of (a) in place, find the worst-case dc output voltage of the integrator when the input is grounded.

**2.121** A differentiator utilizes an ideal op amp, a 10-k$\Omega$ resistor, and a 0.01-$\mu$F capacitor. What is the frequency $f_0$ (in Hz) at which its input and output sine-wave signals have equal magnitude? What is the output signal for a 1-V peak-to-peak sine-wave input with frequency equal to $10f_0$?

**2.122** An op-amp differentiator with 1-ms time constant is driven by the rate-controlled step shown in Fig. P2.122. Assuming $v_O$ to be zero initially, sketch and label its waveform.

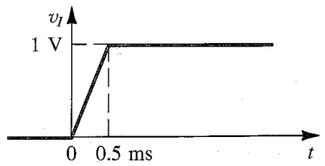



**FIGURE P2.122**

***2.123** An op-amp differentiator, employing the circuit shown in Fig. 2.44(a), has $R = 10$ k$\Omega$ and $C = 0.1$ $\mu$F. When a triangle wave of ±1-V peak amplitude at 1 kHz is applied to the input, what form of output results? What is its frequency? What is its peak amplitude? What is its average value? What value of $R$ is needed to cause the output to have a 10-V peak amplitude? When a 1-V peak sine wave at 1 kHz is applied to

the (original) circuit, what output waveform is produced? What is its peak amplitude? Calculate this three ways: First, use the second formula in Fig. 2.44(a) directly; second, use the third formula in Fig. 2.44(a); third, use the maximum slope of the input sine wave. In each case, establish a value for the peak output voltage and its location.

**2.124** Using an ideal op amp, design a differentiation circuit for which the time constant is $10^{-3}$ s using a 10-nF capacitor. What are the gains and phase shifts found for this circuit at one-tenth and 10 times the unity-gain frequency? A series input resistor is added to limit the gain magnitude at high frequencies to 100 V/V. What is the associated 3-dB frequency? What gain and phase shift result at 10 times the unity-gain frequency?

**D2.125** Figure P2.125 shows a circuit that performs the high-pass single-time-constant function. Such a circuit is known as a first-order high-pass active filter. Derive the transfer function and show that the high-frequency gain is $(-R_2/R_1)$ and the 3-dB frequency $\omega_0 = 1/CR_1$. Design the circuit to obtain a high-frequency input resistance of 10 kΩ, a high-frequency gain of 40 dB, and a 3-dB frequency of 1000 Hz. At what frequency does the magnitude of the transfer function reduce to unity?

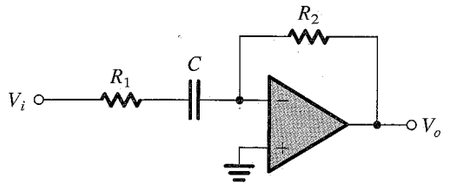



**FIGURE P2.125**

**D**2.126** Derive the transfer function of the circuit in Fig. P2.126 (for an ideal op amp) and show that it can be written in the form

$$\frac{V_o}{V_i} = \frac{-R_2/R_1}{[1+(\omega_1/j\omega)][1+j(\omega/\omega_2)]}$$

where $\omega_1 = 1/C_1R_1$ and $\omega_2 = 1/C_2R_2$. Assuming that the circuit is designed such that $\omega_2 \gg \omega_1$, find approximate expressions for the transfer function in the following frequency regions:

(a) $\omega \ll \omega_1$
(b) $\omega_1 \ll \omega \ll \omega_2$
(c) $\omega \gg \omega_2$

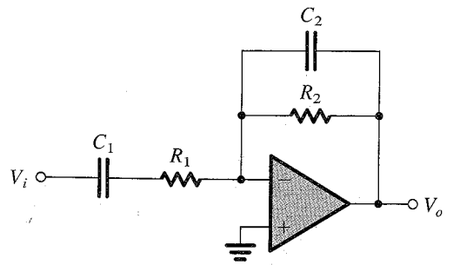
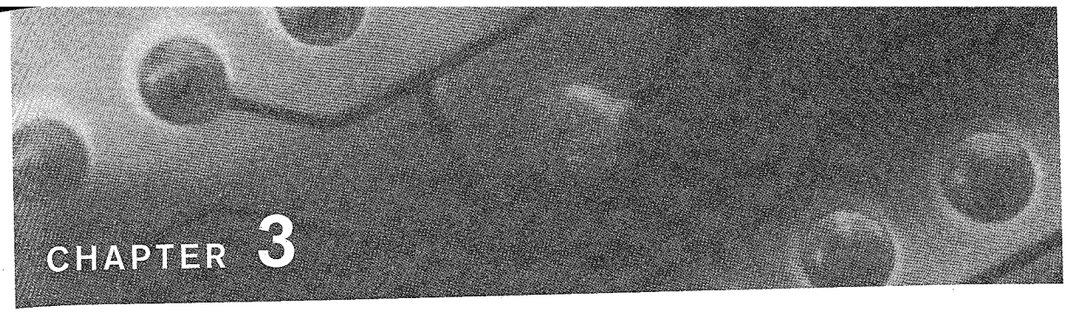



**FIGURE P2.126**

Use these approximations to sketch a Bode plot for the magnitude response. Observe that the circuit performs as an amplifier whose gain rolls off at the low-frequency end in the manner of a high-pass STC network, and at the high-frequency end in the manner of a low-pass STC network. Design the circuit to provide a gain of 60 dB in the "middle frequency range," a low-frequency 3-dB point at 100 Hz, a high-frequency 3-dB point at 10 kHz, and an input resistance (at $\omega \gg \omega_1$) of 1 kΩ.



CHAPTER 3

# Diodes

Introduction 139
3.1 The Ideal Diode 140
3.2 Terminal Characteristics of Junction Diodes 147
3.3 Modeling the Diode Forward Characteristic 153
3.4 Operation in the Reverse Breakdown Region—Zener Diodes 167
3.5 Rectifier Circuits 171
3.6 Limiting and Clamping Circuits 184
3.7 Physical Operation of Diodes 190
3.8 Special Diode Types 209
3.9 The SPICE Diode Model and Simulation Examples 212
Summary 217
Problems 218

## INTRODUCTION

In the previous chapter we dealt almost entirely with linear circuits; any nonlinearity, such as that introduced by amplifier output saturation, was considered a problem to be solved by the circuit designer. However, there are many other signal-processing functions that can be implemented only by nonlinear circuits. Examples include the generation of dc voltages from the ac power supply and the generation of signals of various waveforms (e.g., sinusoids, square waves, pulses, etc.). Also, digital logic and memory circuits constitute a special class of nonlinear circuits.

The simplest and most fundamental nonlinear circuit element is the diode. Just like a resistor, the diode has two terminals; but unlike the resistor, which has a linear (straight-line) relationship between the current flowing through it and the voltage appearing across it, the diode has a nonlinear $i$–$v$ characteristic.

This chapter is concerned with the study of diodes. In order to understand the essence of the diode function, we begin with a fictitious element, the ideal diode. We then introduce the silicon junction diode, explain its terminal characteristics, and provide techniques for the analysis of diode circuits. The latter task involves the important subject of device modeling.