Fu Yong Quah
fuyong.quah14@imperial.ac.uk | www.fyquah.me
Twitter, Github, Linkedin: fyquah95

Third-year Electronic and Information Engineering undergraduate at Imperial College London, United Kingdom. My academic interest is in hardware acceleration of machine learning models.

Skills

FPGA Design SystemVerilog, Maxcompiler, Vivado HLS, Quartus, Resource and Performance Modelling

Programming C++, Python, Java (Expert), Clojure (Intermediate)

Environment Developing and shell scripting in Unix-based environment

Education

2014 - 2018 **Imperial College London, London, UK**
MEng. Electronic and Information Engineering
First class, Dean's List
Computer Architecture, Control Engineering, Computer Vision, Simulation and Modelling, Operational Research, Mathematics, Language Processors

2013 – 2014 **INTI International College Penang, Penang, Malaysia**
Cambridge GCE A-Levels: 4A* in Mathematics, Further Mathematics, Physics and Chemistry.

Professional Experience

04/2017 – 09/2017 **Jane Street Capital - Software Engineering Intern**

07/2016 – 09/2016 **Google Inc - Software Engineering Intern**
- Deploy python static analysis tool (github.com/google/pytype) to code review tool.
- My work was used to run program analysis Borg, pytype and an internal tool.
- Worked with pytype and bazel, in python and java

06/2015 – 08/2015 **Netcraft Ltd – Internet Service Developer Intern**
- Worked primarily on a classification project of hosting companies
- Automated data collection and validation using Perl, Bash scripts and Cronjobs.
- Improve and maintain a web interface for manual data labelling (Perl/CGI/MySQL)

Projects

01/2017 - 03/2017 **fpgaConvNet on Maxeler**
- Map convolutional neural networks to FPGA using maxcompiler.
- Optimized design with logic units, BRAM, DSP and performance mathematical models.

01/2016 - 03/2016 **Self-Hosting C Compiler**
- Implement a turing complete portion of a C to MIPS compiler
- Written in C, flex and bison, extensively using classic C dynamic-dispatch techniques

05/2015 – 06/2015 **Real-time Autofocus for FPGA** *[link: https://youtu.be/UJXkHhFQPak]*
- Developed an algorithm to carry out autofocus with FPGA via edge detection.
- Written in C++ using High Level Synthesis with Verilog HDL.

Awards

2016 **NUS Data Science Challenge -** Grand Prize
PennApps – Grand Prize (http://technical.ly/philly/2016/01/25/scary-hardware-hack-won-pennapps-ramear/)

2015 **Head of Department Prize –** Top student in first year Electronic and Information Engineering
Won **Grand Prize** in the **Fishackathon,** sponsored to attend **World Mobile Congress 2016**
Won **Grand Prize** in the **Imperial Bitcoin Forum**

2014 **King's Scout** title (Eagle Scout equivalent)
Represented Malaysia in the **International Olympiad in Informatics (IOI)**

Languages

English, Chinese (Mandarin), Malay