brickout_game Project Status (06/26/2012 - 12:50:09)					
Project File:	brickout.xise	Parser Errors:	No Errors		
Module Name:	brickout_game	Implementation State:	Programming File Generated		
Target Device:	xc3s200-4ft256	• Errors:	No Errors		
Product Version:	ISE 13.2	• Warnings:	106 Warnings (106 new)		
Design Goal:	Balanced	• Routing Results:	All Signals Completely Routed		
Design Strategy:	Xilinx Default (unlocked)	Timing Constraints:	All Constraints Met		
Environment:	System Settings	Final Timing Score:	0 (Timing Report)		

Device Utilization Summary					[-]
Logic Utilization	Used	Available	Utilization	Note(s)	
Number of Slice Flip Flops	252	3,840	6%		
Number of 4 input LUTs	1,135	3,840	29%		
Number of occupied Slices	690	1,920	35%		
Number of Slices containing only related logic	690	690	100%		
Number of Slices containing unrelated logic	0	690	0%		
Total Number of 4 input LUTs	1,221	3,840	31%		
Number used as logic	1,135				
Number used as a route-thru	86				
Number of bonded <u>IOBs</u>	9	173	5%		
Number of BUFGMUXs	2	8	25%		
Average Fanout of Non-Clock Nets	3.65				

Performance Summary				
Final Timing Score:	0 (Setup: 0, Hold: 0, Component Switching Limit: 0)	Pinout Data:	Pinout Report	
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report	
Timing Constraints:	All Constraints Met			

Detailed Reports [-					
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Fri Jul 6 10:29:29 2012	0	106 Warnings (106 new)	8 Infos (8 new)
Translation Report	Current	Fri Jul 6 10:29:34 2012	0	0	0
Map Report	Current	Fri Jul 6 10:29:39 2012	0	0	2 Infos (2 new)

Place and Route Report	Current	Fri Jul 6 10:29:50 2012	0	0	0
Power Report					
Post-PAR Static Timing Report	Current	Fri Jul 6 10:29:52 2012	0	0	4 Infos (4 new)
Bitgen Report	Current	Fri Jul 6 10:29:57 2012	0	0	1 Info (1 new)

Secondary Reports			
Report Name	Status	Generated	
WebTalk Report	Current	Fri Jul 6 10:29:58 2012	
WebTalk Log File	Current	Fri Jul 6 10:30:00 2012	

Date Generated: 07/06/2012 - 10:30:40