brickout_game Project Status (06/26/2012 - 12:50:09)				
Project File:	brickout.xise	Parser Errors:	No Errors	
Module Name:	brickout_game	Implementation State:	Mapped	
Target Device:	xc3s200-4ft256	• Errors:	X 2 Errors (2 new)	
Product Version:	ISE 13.2	• Warnings:	103 Warnings (2 new)	
Design Goal:	Balanced	Routing Results:		
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:		
Environment:	System Settings	• Final Timing Score:		

Device Utilization Summary [-					
Logic Utilization	Used	Available	Utilization	Note(s)	
Number of Slice Flip Flops	302	3,840	7%		
Number of 4 input LUTs	3,081	3,840	80%		
Number of occupied Slices	2,061	1,920	107%	OVERMAPPED	
Number of Slices containing only related logic	2,061	2,061	100%		
Number of Slices containing unrelated logic	0	2,061	0%		
Total Number of 4 input LUTs	4,054	3,840	105%	OVERMAPPED	
Number used as logic	3,081				
Number used as a route-thru	973				
Number of bonded <u>IOBs</u>	9	173	5%		
Number of BUFGMUXs	2	8	25%		
Average Fanout of Non-Clock Nets	2.10				

Detailed Reports [-]						
Report Name	Status	Generated	Errors	Warnings	Infos	
Synthesis Report	Current	Fri Jul 6 10:21:37 2012	0	102 Warnings (2 new)	4 Infos (0 new)	
Translation Report	Current	Fri Jul 6 10:22:07 2012	0	0	0	
Map Report	Current	Fri Jul 6 10:22:18 2012	X 2 Errors (2 new)	1 Warning (0 new)	2 Infos (0 new)	
Place and Route Report	Out of Date	Fri Jul 6 10:20:13 2012	0	1 Warning (1 new)	0	
Power Report						
Post-PAR Static Timing Report	Out of Date	Fri Jul 6 10:20:16 2012	0	0	4 Infos (0 new)	
Bitgen Report	Out of Date	Fri Jul 6 10:20:23 2012	0	1 Warning (0 new)	1 Info (0 new)	

Secondary Reports			[-]
Report Name	Status	Generated	
WebTalk Report	Out of Date	Fri Jul 6 10:20:24 2012	
WebTalk Log File	Out of Date	Fri Jul 6 10:20:26 2012	

Date Generated: 07/06/2012 - 10:22:42