Rahul Guruprakash

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Education

North Carolina State University **Raleigh, NC**

Master of Science in Computer Engineering *Expected Fall 2027*

Relevant Coursework: Computer Architecture, Microarchitecture Security, Operating Systems

R.V College of Engineering **Bangalore, India**

Bachelor of Electrical and Electronics Engineering *GPA: 8.3/10*

Skillset

Programming: Adept in embedded software design with C and C++. Relevant experience with build systems (CMake, SCons), compilers (GNU, LLVM), scripting languages (shell, perl) and python.

Tools: Trace32, GDB, OpenOCD, QEMU, Arm FVP, Buildroot, Busybox, Yocto, GTest, PCB Layout tools - Altium, KiCAD.

Platforms: Experience and contributions in Trusted-Firmware, Linux Kernel Drivers, XEN, MCUBoot, Nuttx, FreeRTOS.

Professional Work Experience

Arm - Engineer, System Compliance - ATG, Bangalore **July '23 - August '25**

- Contributor and maintainer of the open-source arm Firmware Framework for A Profile Architecture (FF-A) architecture compliance suite (ACS) - https://github.com/ARM-software/ff-a-acs.
- Contributed compliance and testing strategy for FF-A Specification v1.1 and v1.2. Developed FF-A test suites for secure partition memory model, interrupt model and FF-A run time state machines.
- Developed bare metal drivers for aarch64 MMU, Generic Interrupt Controller, SMMU, DMA for Arm Base FVP Targets.
- Designed ACS Linux kernel driver for FF-A system compliance from user space and added platform support for NS-Hypervisor. This was a key deliverable for ACS adoption in Android - pKVM FF-A Compliance by Google.
- Contributed FF-A bug fixes for reference system platforms - Hafnium (SPMC), XEN (NS-Hypervisor) and TF-A.

Qualcomm - Engineer, RF-Link Manager Team, Hyderabad **October '21 - July '23**

- Developed RF front-end drivers for the NR-5G modem (SDX35) SoC, enabling transceiver boot and inter-RAT configuration via the RF coprocessor.
- Built and maintained a GTest framework for pre-silicon SoC bring-up, leveraging virtual platforms to model and surface bugs in pre-silicon RTL and early silicon.
- Designed a CRC scheme for AXI-based linked-list DMA in RF coprocessor firmware to detect bit flips in front-end programming traffic between the modem DSP and RF subsystem.
- Introduced a section-gapped ("holes") RF coprocessor image to mitigate an instruction-decoder hardware bug and drove compiler support effort with the tools team.

Log9 Materials - Engineer, Embedded Systems, Bangalore **January '21 – September '21**

- Developed the EV charging protocol stack and an OSI-layered implementation of GB/T 27930 and SAE J1939/21 CAN in the charging-controller firmware.
- Designed the EV charging controller front-end hardware on a low-power Cortex-M4 SoC, optimizing memory and power for seamless vehicle CAN integration; implemented a CAN-based bootloader for in-field firmware updates and diagnostics.
- Scaled and deployed EVCC hardware across 1,000+ three-wheeled electric autos, with a platform-flexible design supporting integration with standard battery-management hardware.

Academic Research

Graduate Research Assistant - North Carolina State University **August '25 - Present**

- Designing and delivering hardware platforms for AI systems used in biomass mapping and precision agriculture.
- Architecting a custom carrier board for the NVIDIA Orin NX compute module; evaluating signal-integrity requirements and designing high-speed layouts for PCIe Gen4, GbE, and USB 3.2 PHYs.