Rahul Guruprakash

rahulguruprakash@gmail.com | g-rahul.github.io

Education

Bachelor of Electrical and Electronics Engineering (Undergraduate) **Aug '17 – Jul '21**
R.V College of Engineering (RVCE), Bengaluru, India. **GPA: 8.3/10.0**

Research Interests

Computer Architecture, Platform Security and Trusted Computing, System Software Architecture, Operating Systems

Skills

Programming Languages: Three-year experience in firmware and device driver design with C and C++.
Tools: Altium, Matlab, Trace32, CMake, GDB and OpenOCD, Arm FVP Models, Git, Yocto, Buildroot, GTest.
Platform Software: Nuttx RTOS, MCUBoot, TF-A and SPMC- Hafnium, XEN, Linux Device Drivers, Mbed TLS.

Professional Work Experience

Arm Bangalore – Engineer, Architecture and Technology Group **Jul '23 - Present**
Platform Security Architecture Compliance

- Investigated Firmware Framework for A Profile Architecture (FFA) v1.2 specification and developed test strategies for FFA compliance. Maintainer of open-source FFA architecture compliance kit https://github.com/ARM-software/ff-a-acs.
- Developed and contributed Bare Metal software drivers for MMU, Generic Interrupt Controller, System MMU, DMA controller and Secure Partition Images.
- Investigated and devised strategies to enable FFA Architecture compliance stack as a Virtual Machine under Normal World Hypervisor XEN to test FFA Application Binary Interfaces.
- Examined strategies to integrate FFA test suite (ACS) for android pKVM FFA compliance; contributed target configurations to enable FFA ACS as part of Linux VM alongside upstream FFA kernel drivers.

Qualcomm Hyderabad - RFSW Engineer **Oct '21 - July '23**
Modem SoC Software Drivers

- RF Front End Driver development for NR-5G Modem (SDX35) SoC; contributed to firmware designing efforts for managing wireless transceiver boot up and Inter-Radio Access Technology configuration scripts by RF Coprocessor.
- Developed and maintained GTest unit-testing framework for SoC Pre Silicon bring up, leveraging virtual platforms to develop test models that effectively identify bugs in Pre-Silicon RTL and initial Silicon bring-up.
- Designed a CRC32 scheme for an AXI Bus based Linked List DMA in RF coprocessor firmware to detect bit flips in front-end programming traffic between the Modem DSP and the unified RF subsystem.
- Contributed a strategy for incorporating holes in the RF coprocessor image as a workaround to address a hardware instruction decoder logic bug; collaborated with the tools team to create a compiler feature that accommodates images with section gaps.

Log9 Materials Bangalore - Embedded System Design Intern **Jan '21 - Sep '21**
EV Battery Electronics and Rapid Charging Sub System

- Owned the development of EV charging Protocol Stack and contributed an OSI model design to implement GB/T-27930 and SAE-J1939/21 CAN logic in charging controller firmware.
- Designed and developed the EV Charging Controller front-end hardware based on a low-power Cortex-M4 SoC, with an optimized memory and power footprint to enable seamless integration into the existing standard vehicle CAN network.
- EVCC Hardware was scaled and deployed in a fleet of more than a thousand three-wheeled electric autos. The hardware design ensured flexible platform support for integration with standard Battery Management Hardware.
- Designed a CAN-based bootloader firmware state machine for the EV Charging Controller to support on-field device firmware upgrade and diagnostics via the standard vehicle CAN network.

Academic Research Projects

Research and development of Trapezoidal Controller for 3 Phase BLDC Motor **Aug '18 - Mar '19**

Dr. Dinesh MN, Professor - EEE, R.V College of Engineering

- Modeled and simulated a 3-phase trapezoidal motor control system in MATLAB; developed a software state machine and implemented the design on a Cortex-M4 SoC platform with a firmware footprint less than 32kB.
- Investigated and developed parallel MOSFET inverter stage with digital cycle-by-cycle current-limiting scheme for the trapezoidal controller and scaled the system to support concept EV power system of up to 1kW.
- Deployed the controller design as part of inhouse EV automobile developed by an interdisciplinary student club and supported the team in participating in the international event, Shell Eco-Marathon.

Design and development of PSFB converter for wireless charging **Sep '19 - Apr '20**

Ms. Raja Vidya, Associate Professor - EEE, R.V College of Engineering

- Developed a MATLAB model to simulate PSFB Power controller with parallel FET configuration and synthesized control logic from Simulink coder to test on SoC.
- Designed and taped out 4kW 400V Power Factor Correction stage for the PSFB converter, investigated and designed high power toroidal inductor for PFC filtering stage including an inhouse multipurpose Litz wire coil.

Profiling real time performance of freeRTOS and comparison with AUTOSAR **Sep '20 - Dec '20**

Dr. Anitha GS, Professor - EEE, R.V. College of Engineering

- Presented technical seminar on real time requirements of automotive operating system and carried out an investigation to evaluate its use case in automotive ECU firmware in line with AUTOSAR spec.
- Profiled and characterized freeRTOS's real time capabilities on an ARM Cortex-M4 SoC by deploying kernel monitors to analyze performance on SEGGER System View.

Design of stackable passive balancer for 48V Li-ion Battery Pack **Jan '20 - May '20**

Dr. Dinesh MN, Professor - EEE, R.V. College of Engineering

- Designed and taped out stackable passive battery balancer module for 48V li-ion battery based on Texas instrument battery monitor ASIC BQ764PL455 platform.
- Scaled up the battery monitor design to support 48V 20Ah battery pack for 1kW power loads. Developed custom drivers to enable battery monitoring with stackable configuration of up to 200V.

Leadership and Extracurricular Role

Team Garuda, RVCE EV Student Club **Sep '19 - Aug '21**

Team Captain | Electrical Sub System Lead

- Head of student innovative club, Team Garuda, between 2020 and 2021. I was the lead for electrical systems when the team took part in international efficiency challenge, the Shell Eco- Marathon, in Sepang, Malaysia. Team Garuda was the only team from India in 2019 edition to develop custom motor controller and participate in the urban concept electric vehicle category of the event.

Embedded Security Hackathon, ECE Dept, RVCE **Sep '24**

Speaker and organizer

- Organized an embedded security hackathon for the fourth semester students of the Electronics and Communication department of RVCE, as part of the academic credit requirement for the students.
- Presided over the event with an introductory talk on embedded security and threat models for edge devices. Framed a problem statement to implement quasi root of trust by leveraging Cortex-M7 memory protection unit and SoC specific AXI controlled executive only memory partitioning.