CMT2119A Programming Notes.

Serial data format.

Uses a simple 2 wire SPI type interface. No Chip Select. Data line is bidirectional.
Clock is Idle High. Latch Data on the negative going edge.
Data is sent MSB (bit 15) first.
16 bits per transfer.
Bit 15 is always a high.
Bit 14 is low for write and high for read.
Bits 13 to 8 are the register address.
Bits 7 to 0 are the data. Sourced by CPU for Writes and by the CMT2119 for reads.

Max clock rate is 1MHz. (500 ns high 500 ns low)

There are two types of register. The command type uses the above format and appears to configure the chip itself.
The synthesiser settings are programmed into secondary Feature registers which are loaded using a special command sequence.

Programming.

Normally the chip will self program from its built in EEPROM. No external programming is required. The EEPROM is programmed using the manufacturers RFPDK program and USB interface. The exact protocol for this is not documented and currently unknown.

The EEPROM programming can be overridden by a microcontroller using the following procedure, however the settings are not permanent and will be lost on the next power cycle.

The procedure is documented in the datasheet and needs to be followed exactly.

Step 1. Send the special TWI_RESET sequence. This activates the CPU control mode.

Send 32 clock cycles with the data line held low. Then send 0D00. 48 clock cycles in total.

Step 2. Send the Soft Reset Command.

Send 3D01. Then wait at least 1ms.

Step 3. Send an initialisation command (don't know what it does)

Send 2278.

Step 4. Send a fixed set of commands. (don't know what they do)

Send 2F80 35CA 36EB 3737 3882

Step 5. Send more commands (don't know what they do)

Send 1210 1200 2407 1D20

Step 6. Program the Secondary Feature registers. (loop round 21 times)

For each of the 21 Secondary Feature registers. Program the values calculated by the RFPDK program.

Send 18AA to set register address
Send 19LL to set register low 8 bits
Send 1AHH to set register high 8 bits
Send 2501 to program the register

Step 7. Send the TWI_OFF command to end the direct register access.

Send 0D02

RF output is now directly under control of the DATA pin. Low is RF Off. High is RF On.

Secondary registers.

The 21 Secondary register values are best calculated using the RFPDK program. The calculated values can be output to a text file using the Export function.

The register functions are not documented but the following has been found by reverse engineering and can be used for live tuning.

Register 0:- Normal Value = 5000 5400 enables a /2 output divider for lower output frequencies.
Register 6:- Normal Value = 0000 0001 enables a /1.5 output divider for lower frequencies

Register 7:- Holds the low 16 bits of the fractional N divider. Bit zero is always low so N must always be even.
Register 8:- Bits 15 to 8 hold the top 8 bits of the fractional N divider. Bit 7 is high for FSK mod low for OOK mod.
Register 9:- Bits 10 to 3 hold the deviation setting (FSK Shift) for FSK mode. (Zero for OOK)

Frequency Calculation.

Frequency 240 – 320 MHz Output divider = 3 (1.5 and 2.0)
Frequency 320 – 480 MHz Output Divider = 2
Frequency 480 – 640 MHz Output Divider = 1.5
Frequency 640 – 960 MHz Output Divider = 1

Reference frequency = 26 MHz.
Step size = 26000000 / 2^17 = 198.3642578125 Hz.

VCO Frequency = Output Frequency * Output Divider.

Divider setting = VCO Frequency / Step Size

Divider must be even. So step size is effectively doubled.

Examples.

250.0 MHz Output Divider = 3 VCO = 750.0 Divider = 3780922 = 39B13A Hex
435.0 MHz Output Divider = 2 VCO = 870.0 Divider = 4385870 = 42EC4E Hex
500.0 MHz Output Divider = 1.5 VCO = 750.0 Divider = 3780922 = 39B13A Hex
800.0 MHz Output Divider = 1 VCO = 800.0 Divider = 4032984 = 3D89D8 Hex

Programming the device EEPROM

Reverse engineered procedure for programming the device EEPROM.

Step 1. Send the special TWI_RESET sequence. This activates the CPU control mode.

Send 32 clock cycles with the data line held low. Then send 0D00. 48 clock cycles in total.

Step 2. Send the special power on sequence (don't know exactly what this does)

Send 023B 2F80 3F01 1631 35CA 36EB 3737 3882

Step 3. Erase each EEPROM Location and then write new value. (repeat for each location)

Send 17AA to set EEPROM address
Send 1639 to start the Erase

wait 1 ms then Read Register 1F until it returns with bit 3 =1

Send 1631 to end the Erase

Send 17AA to reset EEPROM address
Send 19LL to set the low 8 bits
Send 1AHH to set the high 8 bits
Send 1635 to start the EEPROM Write

wait 1 ms then Read Register 1F until it returns with bit 3 =1

Send 1631 to end the Write

Step 4. Send the Exit Sequence

Send 1630 3F00 0C27 2F00 027F 0C07 3D01

Optional EEPROM verify

The Factory Programmer also verifies the EEPROM values

Step 1. Send the special TWI_RESET sequence. This activates the CPU control mode.

Send 32 clock cycles with the data line held low. Then send 0D00. 48 clock cycles in total.

Step 2. Send the special power on sequence (don't know exactly what this does)

Send 023B 2F80 3F01 1631 35CA 36EB 3737 3882

Step 3. Read and verify each EEPROm Location (repeat for each location)

Send 17AA to set the EEPROM Address
Send 1633 to read the EEPROM

wait 1 ms then Read Register 1F until it returns with bit 3 =1

Read Register 1B for the EEPROM Low Byte
Read Register 1C for the EEPROM High Byte

Send 1631 to end the read

Step 4. Send the Exit Sequence

Send 1630 3F00 0C27 2F00 027F 0C07 3D01