An introduction to

Quantum Annealing Hardware

Gaelen Marsden
Processor Software

Copyright © D-Wave Systems Inc.

Outline

Technology

- Why and how
- Types of quantum computers
- Quantum annealing
- D-Wave implementation
  - Devices
  - Timing
  - Layout
- 2000Q & Advantage

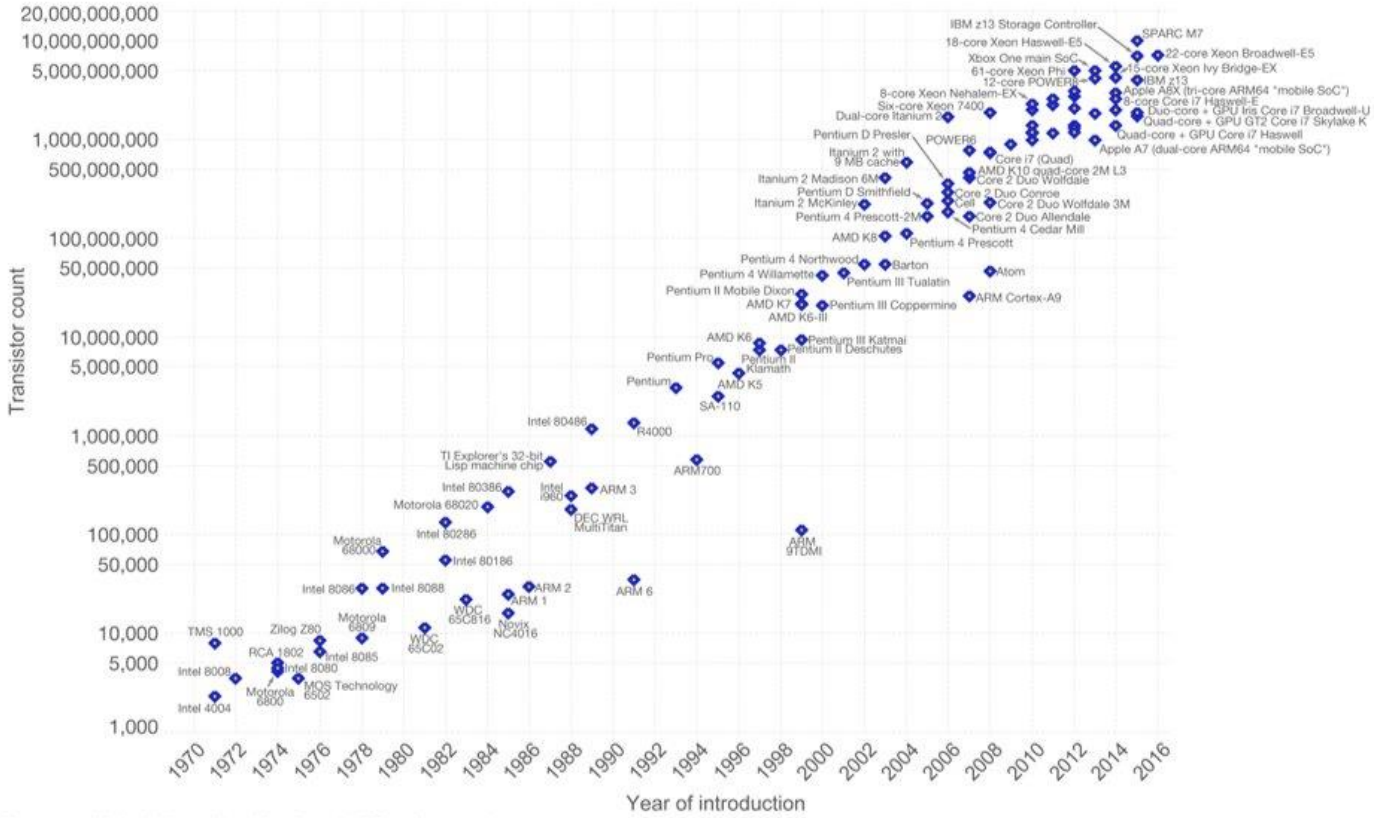
Copyright © D-Wave Systems Inc.

Why Quantum Computers?

- Classical computers will hit their max capability as predicted by the trend that transistor count doubles about every two years – Moore's Law

- We can use quantum physics to increase the power of computation

Moore's Law



Data source: Wikipedia (https://en.wikipedia.org/wiki/Transistor_count)
The data visualization is available at OurWorldinData.org. There you find more visualizations and research on this topic.

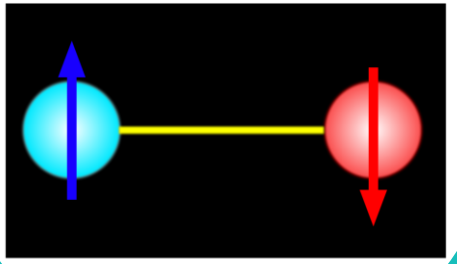
Licensed under CC-BY-SA by the author Max Roser.

Copyright © D-Wave Systems Inc.

Quantum Physics

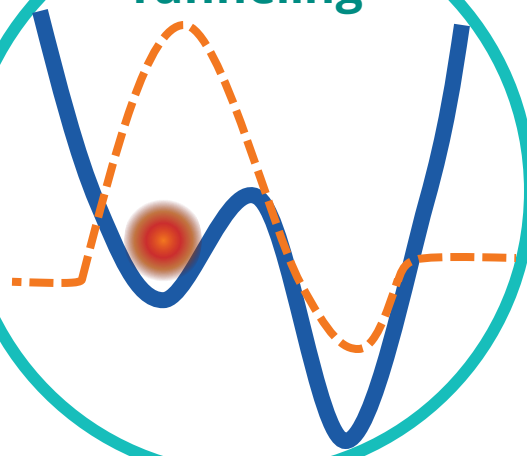
Exploit quantum effects to solve problems beyond the capabilities of classical computers

entanglement



superposition

Tunneling



Copyright © D-Wave Systems Inc.

Different ways of doing Quantum Computation

They all have advantages and disadvantages

What we considered:

- Feasibility of fabrication and operation
- Scaling to larger system sizes
- Tolerance to noise
- Current application to relevant problems

Quantum computer models

- Adiabatic quantum computer
- Quantum gate computer
- One-way quantum computer
- Topological quantum computer

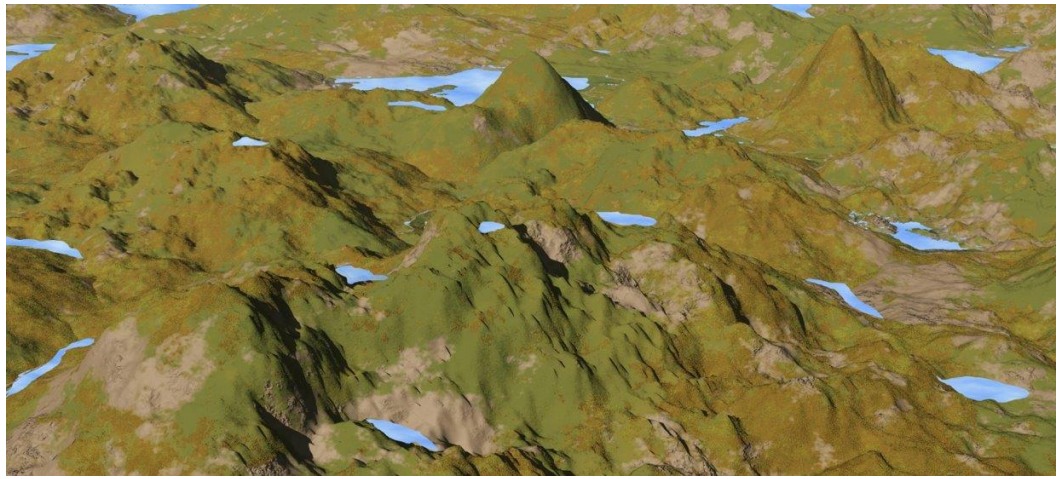
Types of qubits

Super-conducting loops | **Trapped ions** | **Silicon quantum dots** | **Topological qubits** | **Diamond vacancies**

(GRAPHIC) C. BICKEL/*SCIENCE*

Copyright © D-Wave Systems Inc.

Quantum Annealing



Adiabatic Theorem

- Start a quantum system in the ground-state of a Hamiltonian (energy landscape)
- If that Hamiltonian changes slowly enough in time, the system will end up in the ground state of the final Hamiltonian

Ground state computation

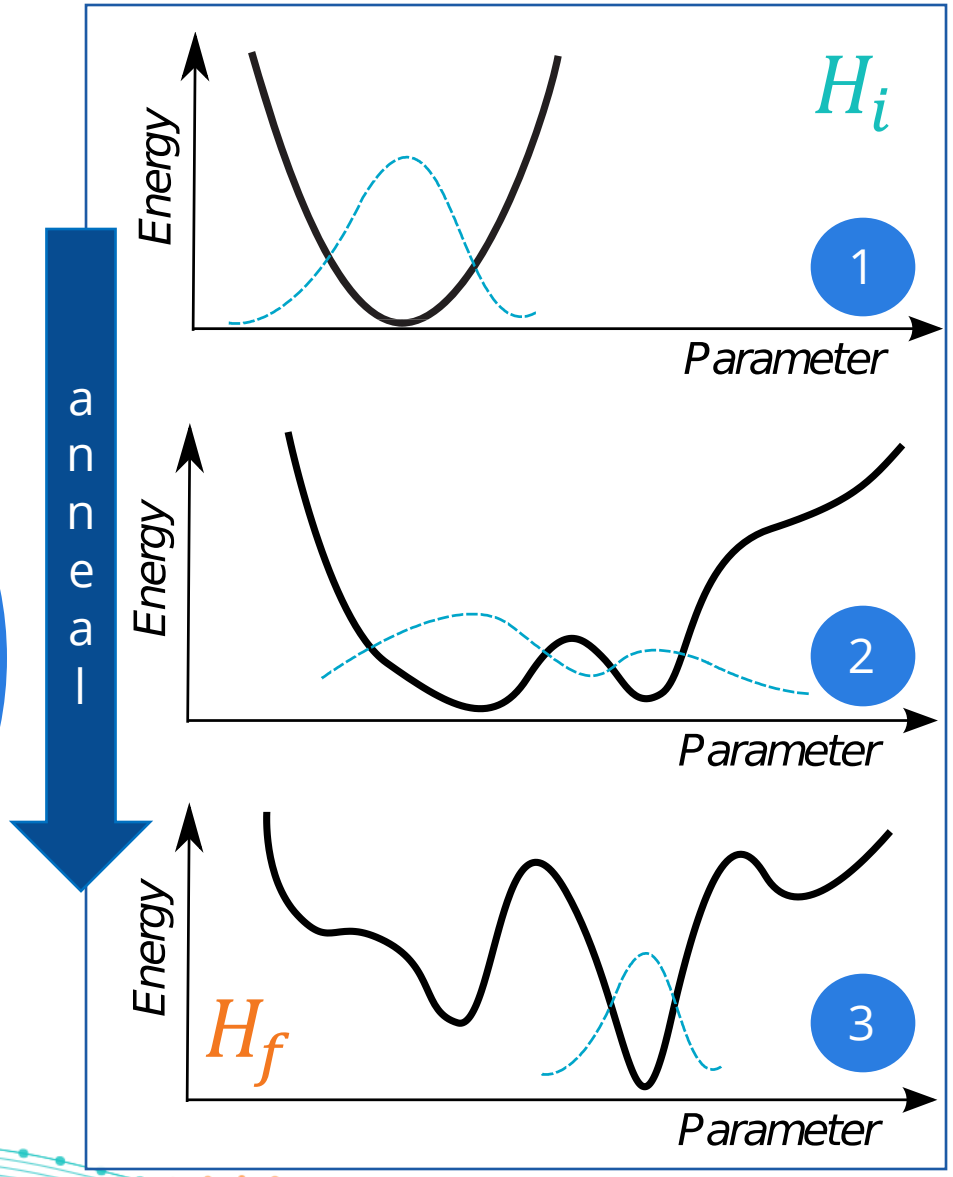
Copyright © D-Wave Systems Inc.

Quantum Annealing

Relies on the *adiabatic theorem* of quantum mechanics

2

- Multiple shallow minima with narrow barriers that allow tunneling
- Wavefunction delocalized across them



1

- Single global minimum
- A broad wavefunction
- Ground state

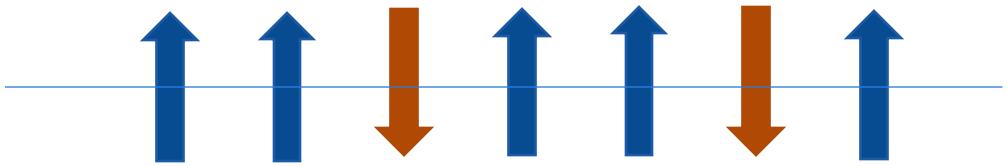
3

- Many deep minima
- Wavefunction localized around global minimum
- The ground state is a classical spin state

Copyright © D-Wave Systems Inc.

Ising Spin problem

- The spin can be in one of two states = Qubits 0 or 1
- The spins are arranged in a lattice = Qubits arrange in lattice in the chip
- Spins can interact with their neighbours = The variables interact
- The system wants to be in the lowest energy state unless is perturbed = we want to stay in the lowest energy state

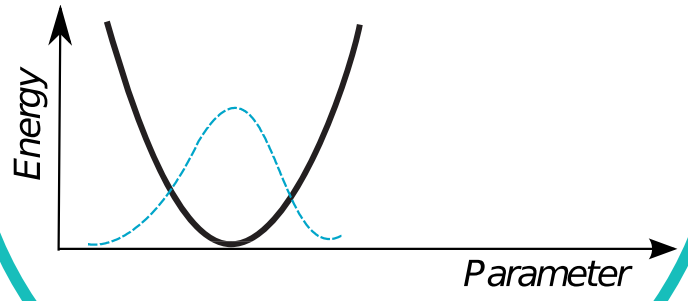


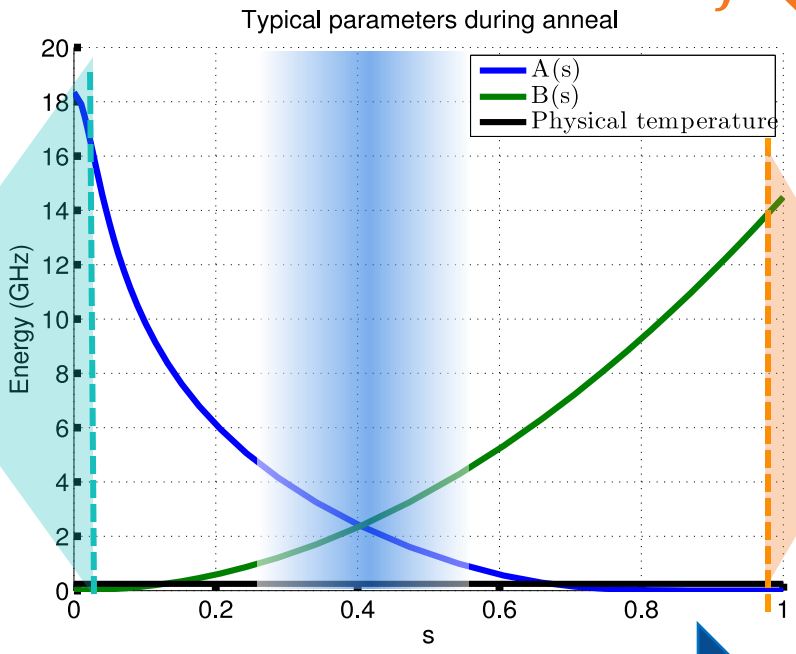
Copyright © D-Wave Systems Inc.

Quantum Annealing - Transverse Field Ising Hamiltonian

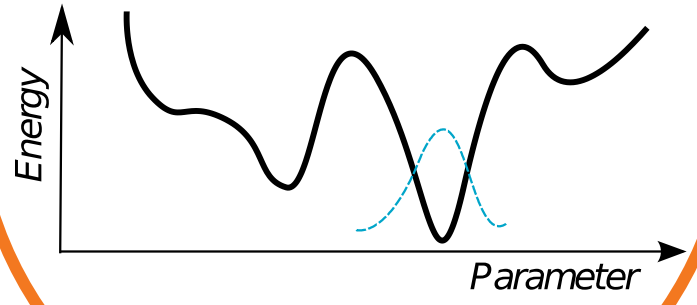
$$H(s) = \underbrace{-A(s)\left[\sum_i \boldsymbol{\sigma}_x^{(i)}\right]}_{H_i} + \underbrace{B(s)\left[-\sum_i h_i \sigma_z^{(i)} + \sum_{i,j>i} J_{ij}\sigma_z^{(i)}\sigma_z^{(j)}\right]}_{H_f}$$

Superposition of qubit states





Classical spin ground state solution

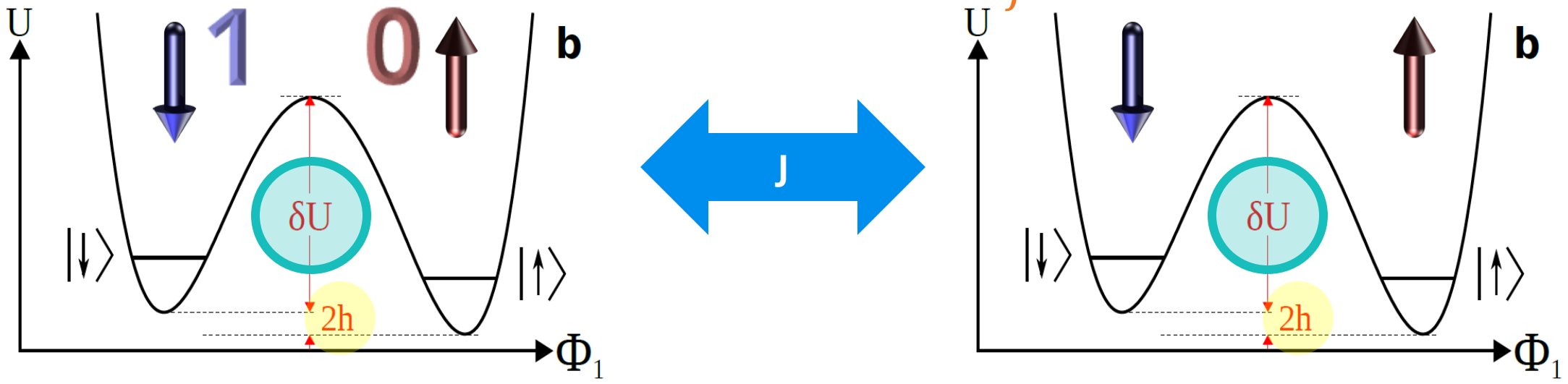


anneal

Copyright © D-Wave Systems Inc.

Quantum Annealing - Transverse Field Ising Hamiltonian

$$H(s) = \underbrace{-A(s)\left[\sum_i \sigma_x^{(i)}\right]}_{H_i} + \underbrace{B(s)\left[-\sum_i h_i \sigma_z^{(i)} + \sum_{i,j>i} J_{ij} \sigma_z^{(i)} \sigma_z^{(j)}\right]}_{H_f}$$



h_i and J_{ij} are specified with **programmable on-chip** control circuitry

Copyright © D-Wave Systems Inc.

D-Wave's Implementation

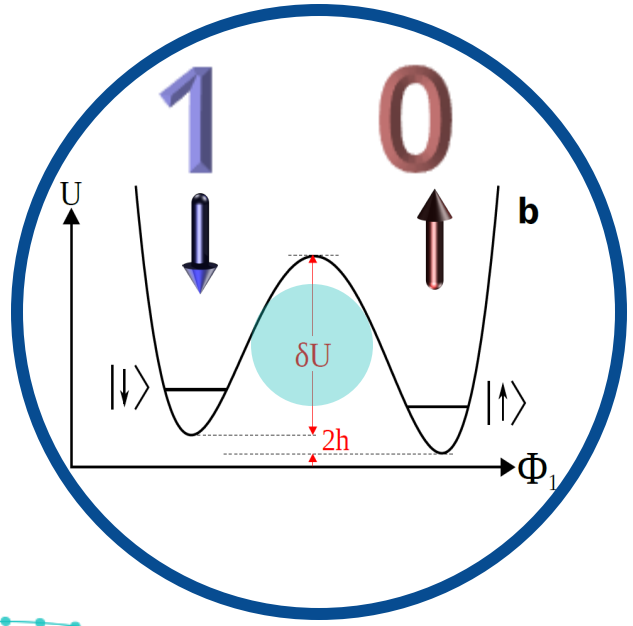
- Devices
  - Qubits
  - Couplers
  - DACS
  - Readout
- Timing
- Layout
- The chip
- The fridge

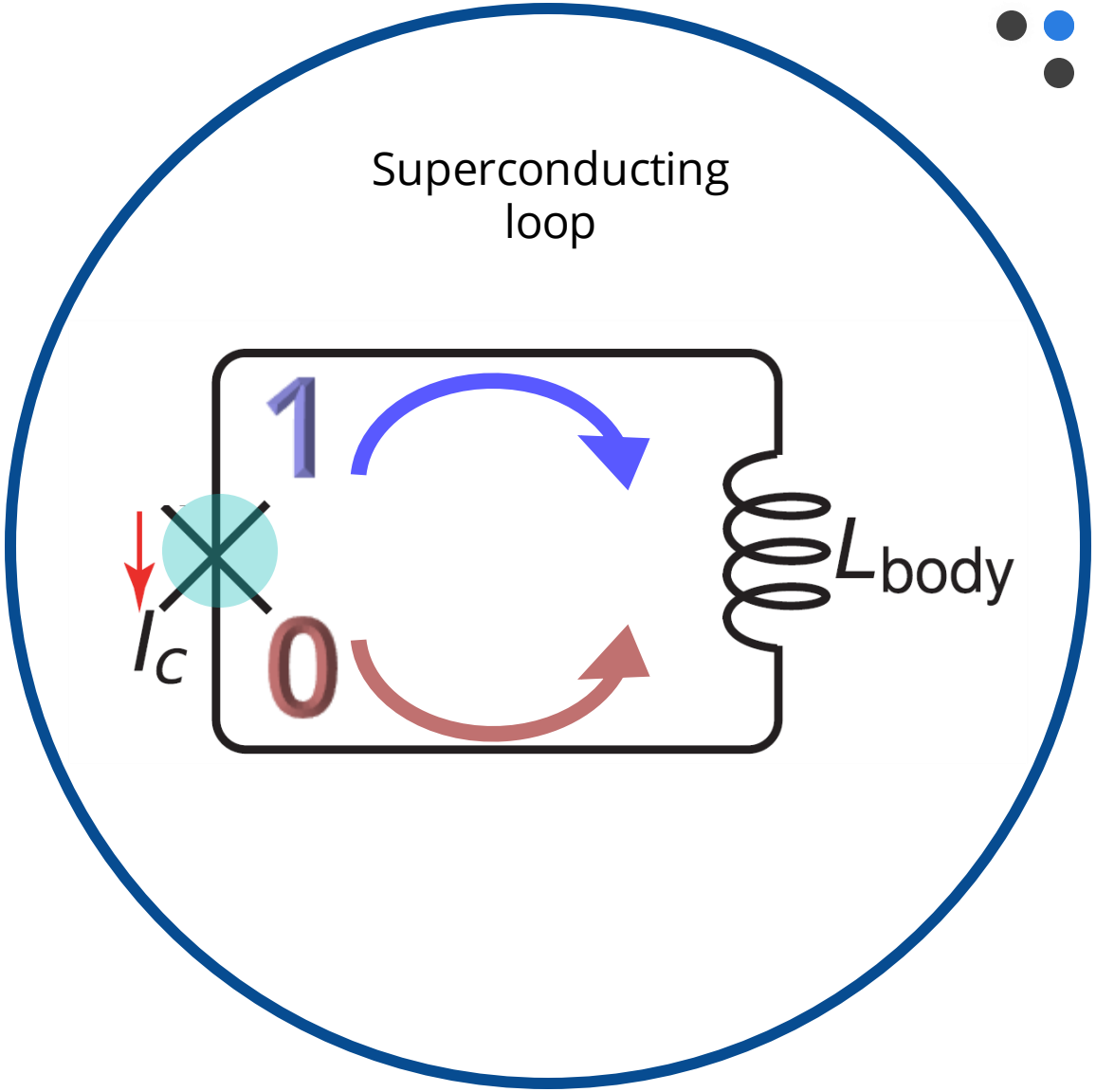
Copyright © D-Wave Systems Inc.

The Qubit – RF SQUID

Josephson Junction
creates barrier in potential

Critical current I_c
determines the barrier height



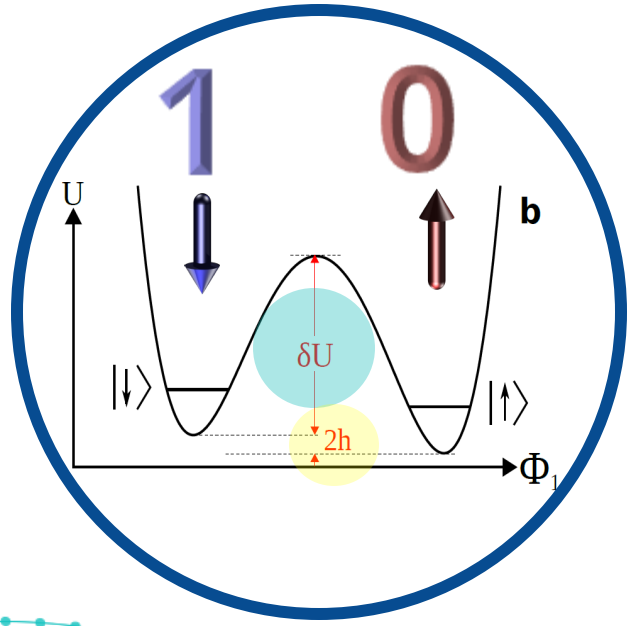


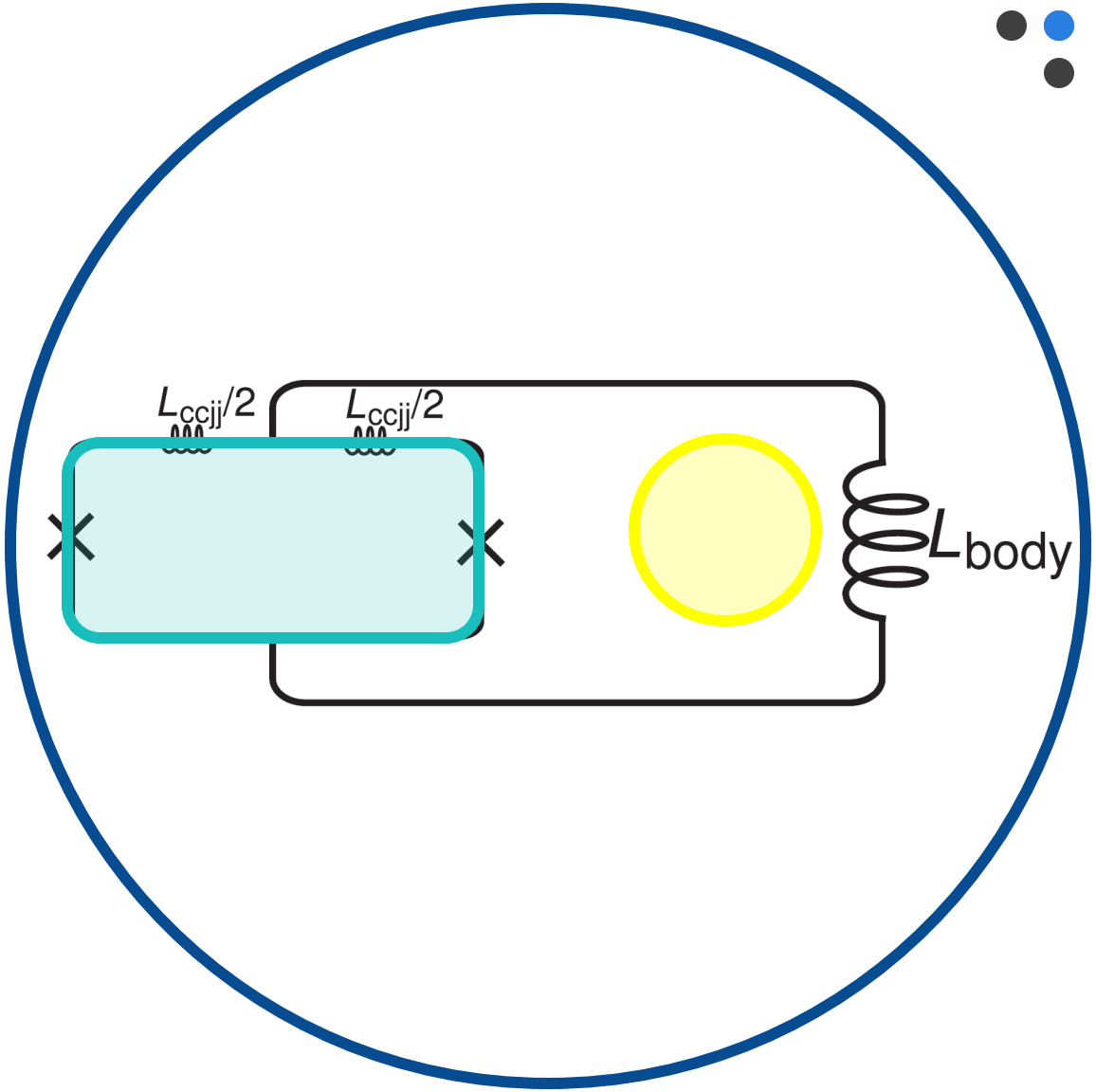
Copyright © D-Wave Systems Inc.

The Qubit – RF SQUID

$$H(s) = -A(s)\left[\sum_i \sigma_x^{(i)}\right] + B(s)\left[-\sum_i h_i \sigma_z^{(i)} + \sum_{i,j>i} J_{ij}\sigma_z^{(i)}\sigma_z^{(j)}\right]$$

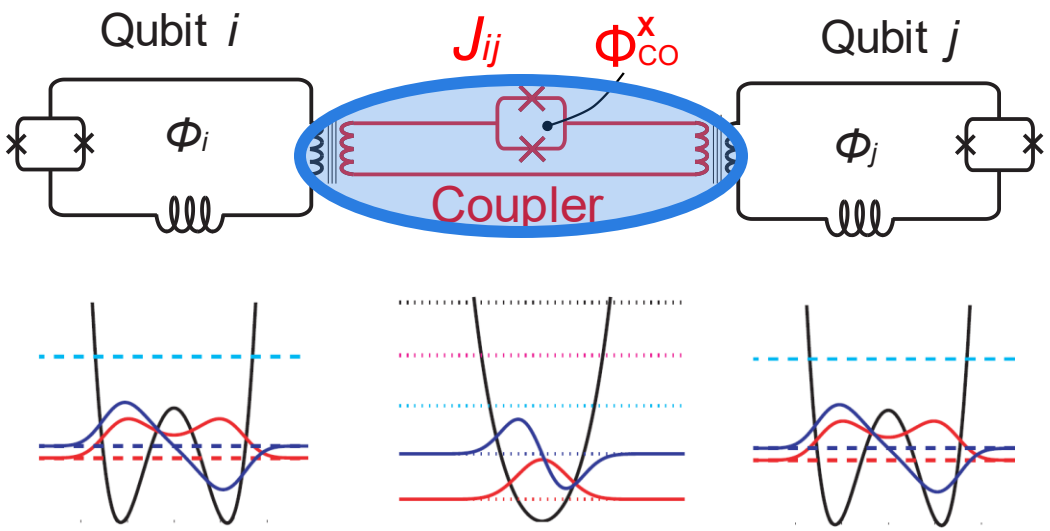
Compound Josephson Junction (CJJ) creates a **tunable** barrier

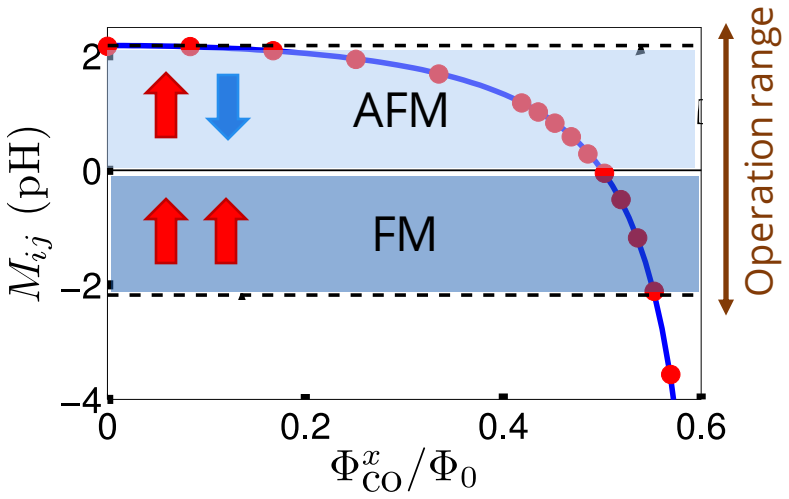




Copyright © D-Wave Systems Inc.

The Qubit – Coupling Qubits





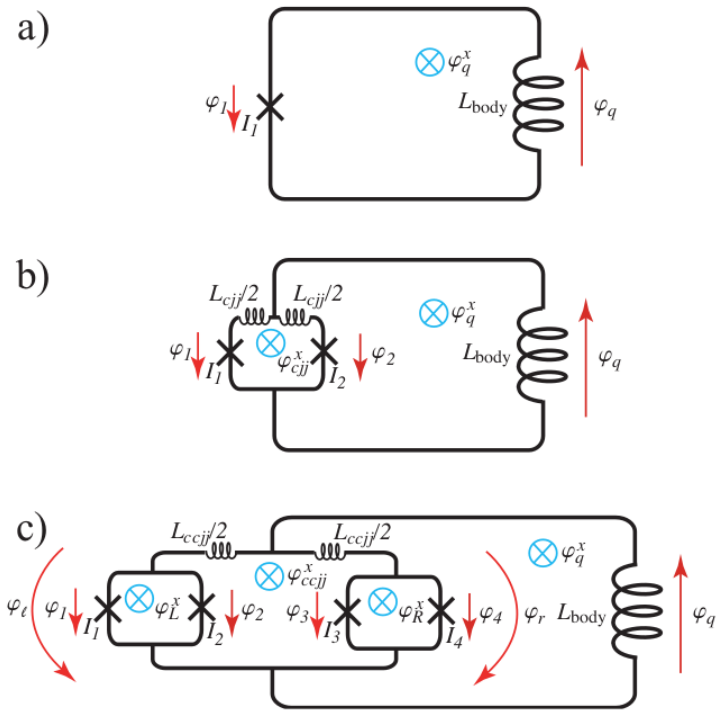
A mono-stable two-junction RF SQUID provides a tunable mutual inductance

$$M_{ij} = \frac{J_{ij}}{|I_p(t)|^2}$$

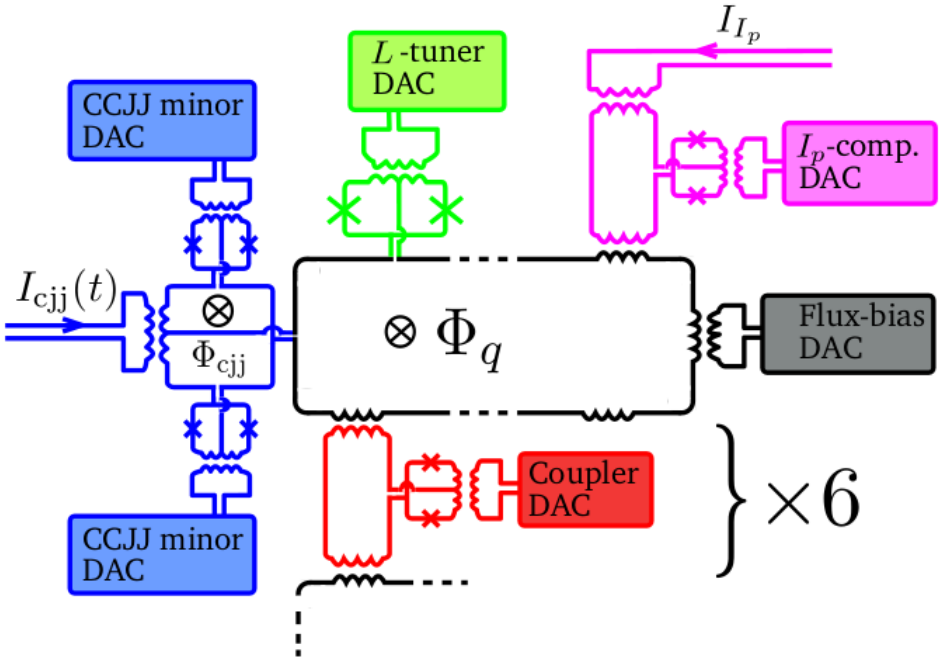
$$H(s) = -A(s)\left[\sum_i \boldsymbol{\sigma}_x^{(i)}\right] + B(s)\left[-\sum_i h_i \sigma_z^{(i)} + \sum_{i,j>i} J_{ij}\sigma_z^{(i)}\sigma_z^{(j)}\right]$$

Copyright © D-Wave Systems Inc.

The Qubit In Detail



Harris et al., 2009

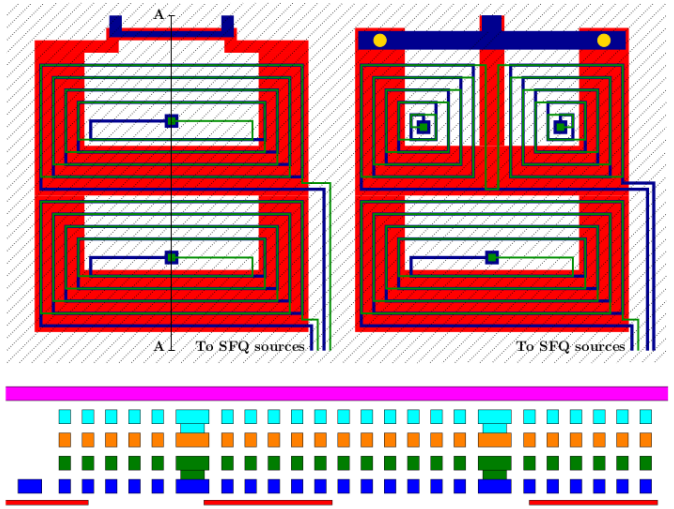


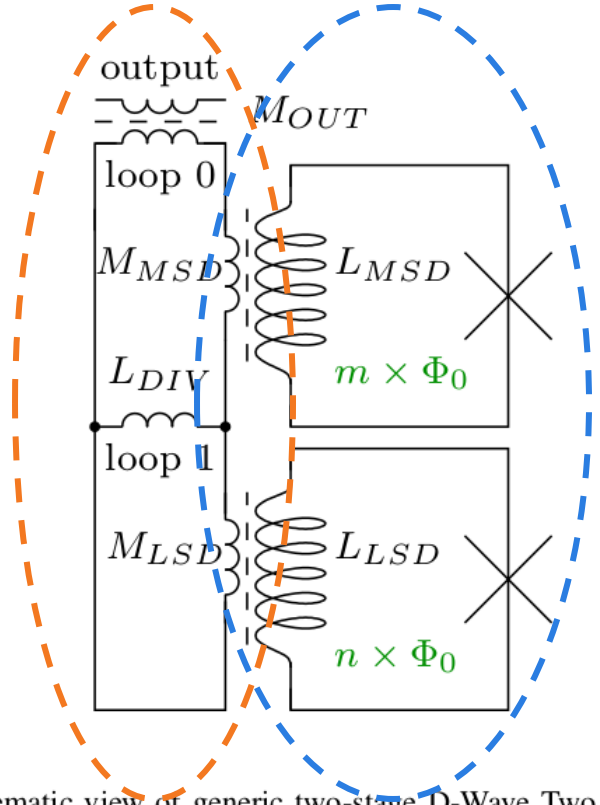
Johnson et al., 2010

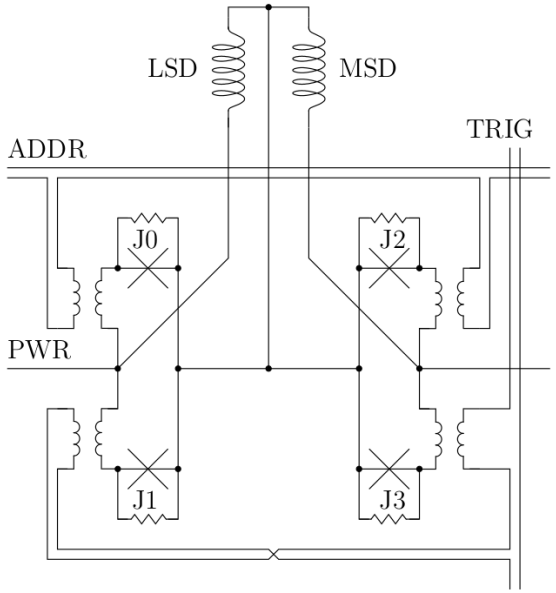
Copyright © D-Wave Systems Inc.

The On-chip Flux DAC

Inductive storage loop







SFQ pulse sources

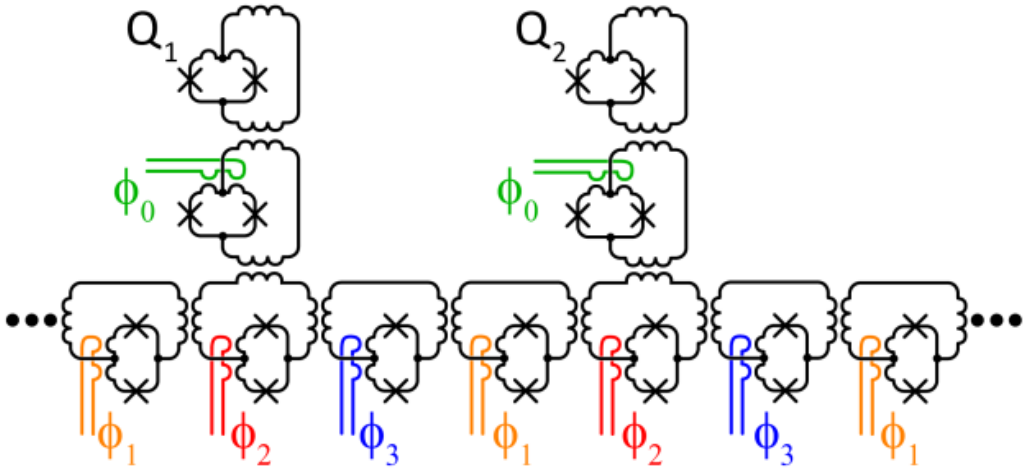
Fig. 3. Schematic view of generic two-stage D-Wave Two Φ-DAC.

Bunyk et al., 2014

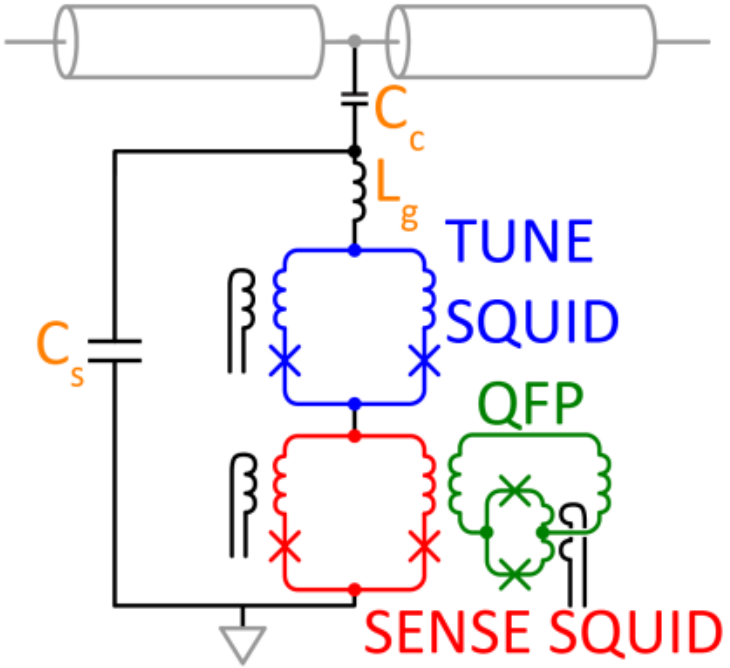
Copyright © D-Wave Systems Inc.

Readout

Shift Register



Tunable Resonator



Whittaker et al., 2016

Copyright © D-Wave Systems Inc.

Timing

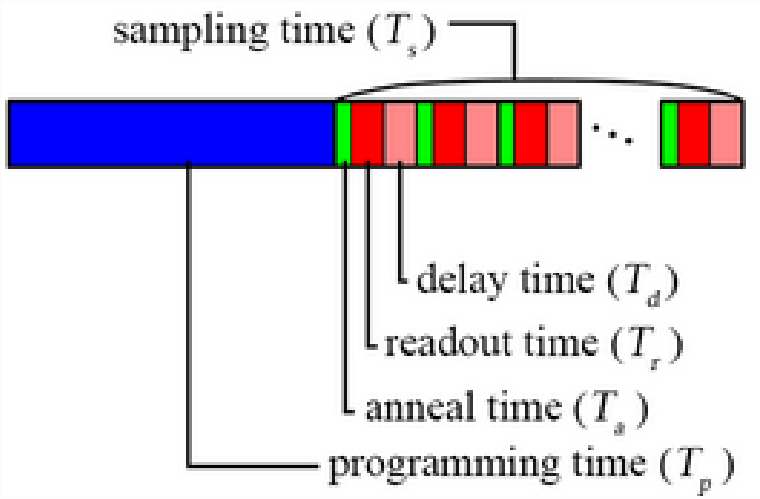


Fig. 101 Detail of QPU access time.

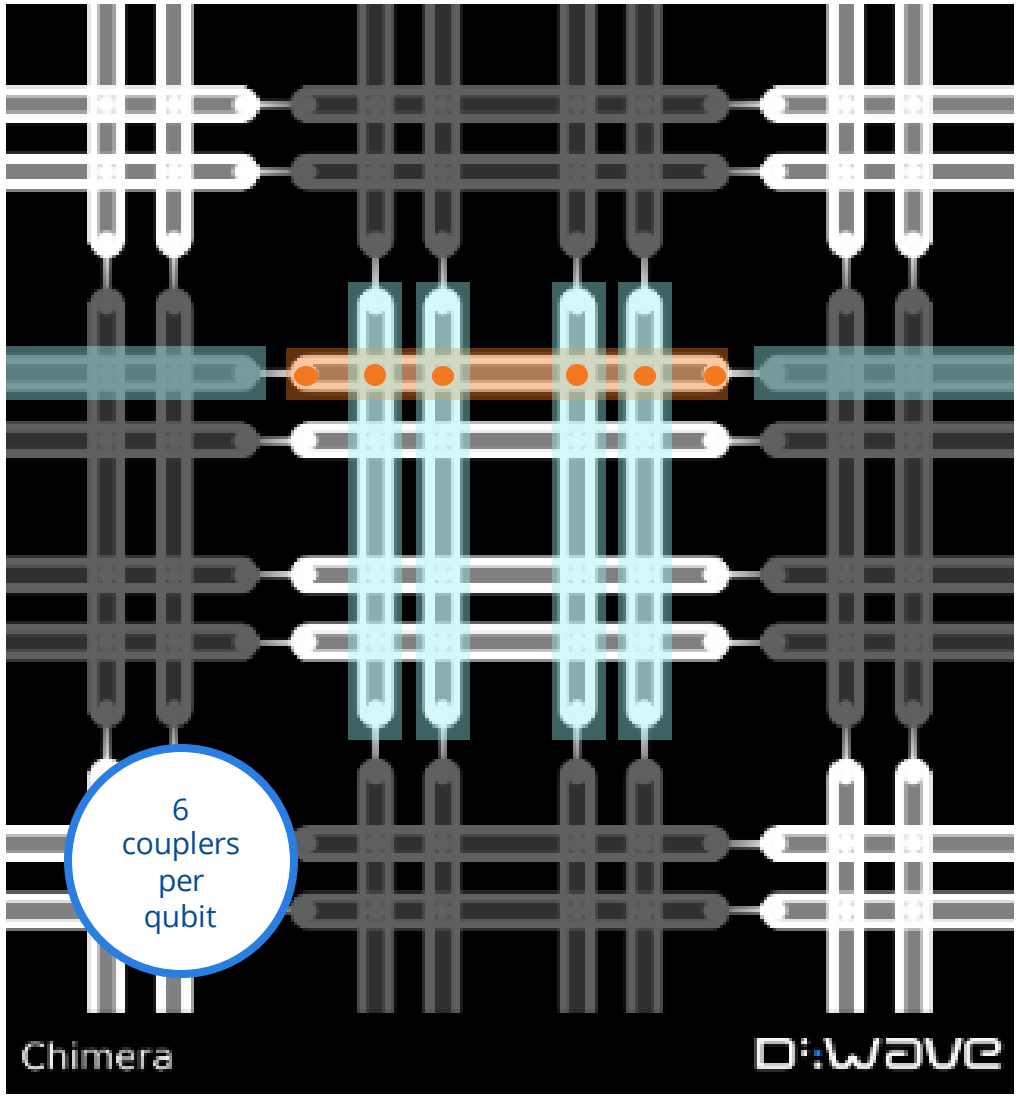
$$T = T_p + \Delta + T_s$$
$$T_s \approx R * (T_a + T_r + T_d)$$

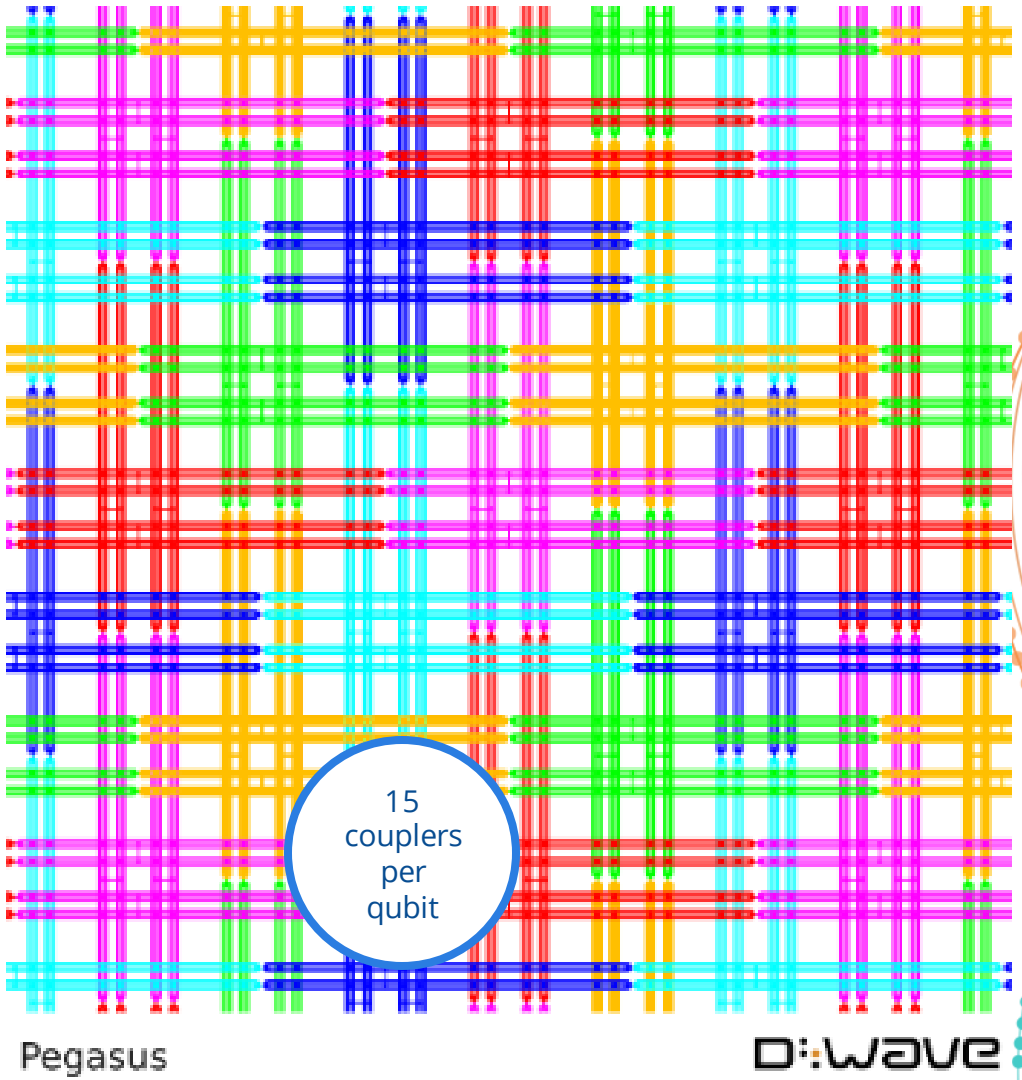
T: QPU access time
T_p: programming time
Δ: overhead time
T_s: sampling time
R: number of reads
T_a: anneal time
T_r: readout time
T_d: delay time

https://docs.dwavesys.com/docs/latest/c_qpu_timing.html

Copyright © D-Wave Systems Inc.

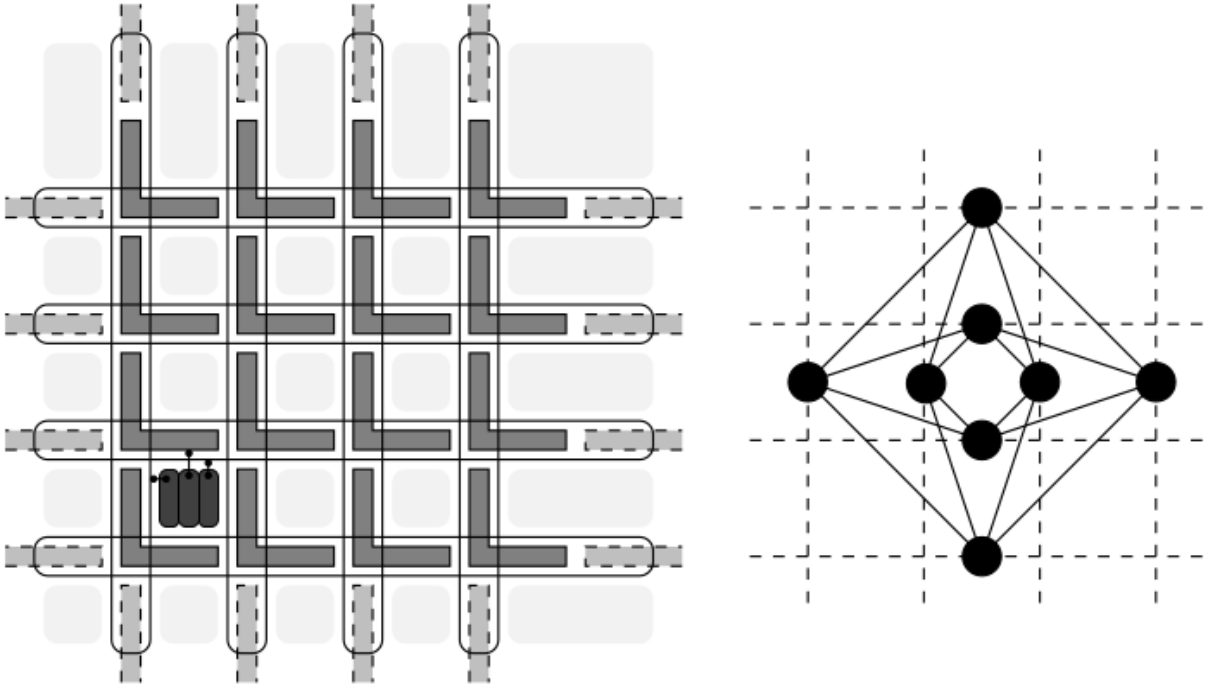
The Chip - Processor Layout





Copyright © D-Wave Systems Inc.

The Chip – Alternate layout diagram



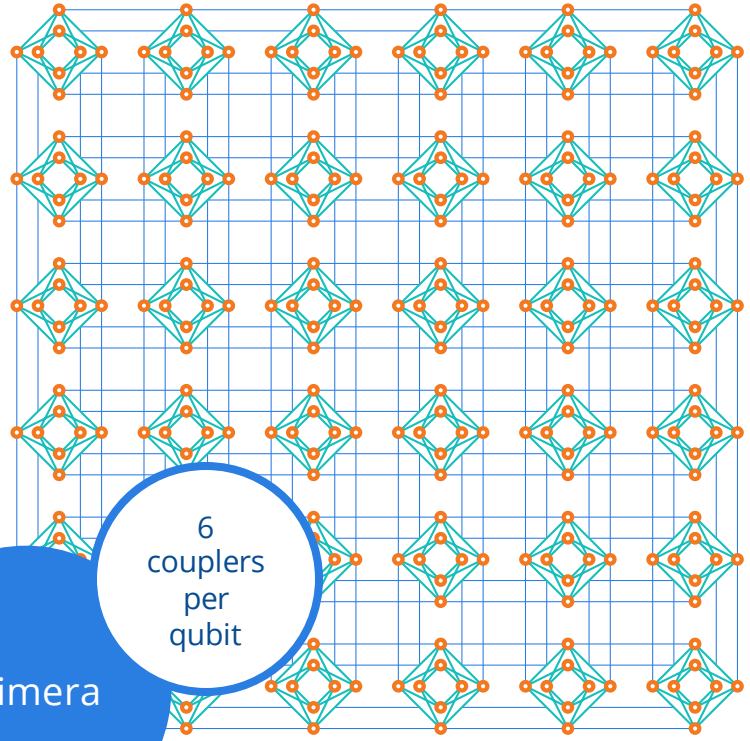
Bunyk et al., 2014

Copyright © D-Wave Systems Inc.

The Chip – Processor Layout

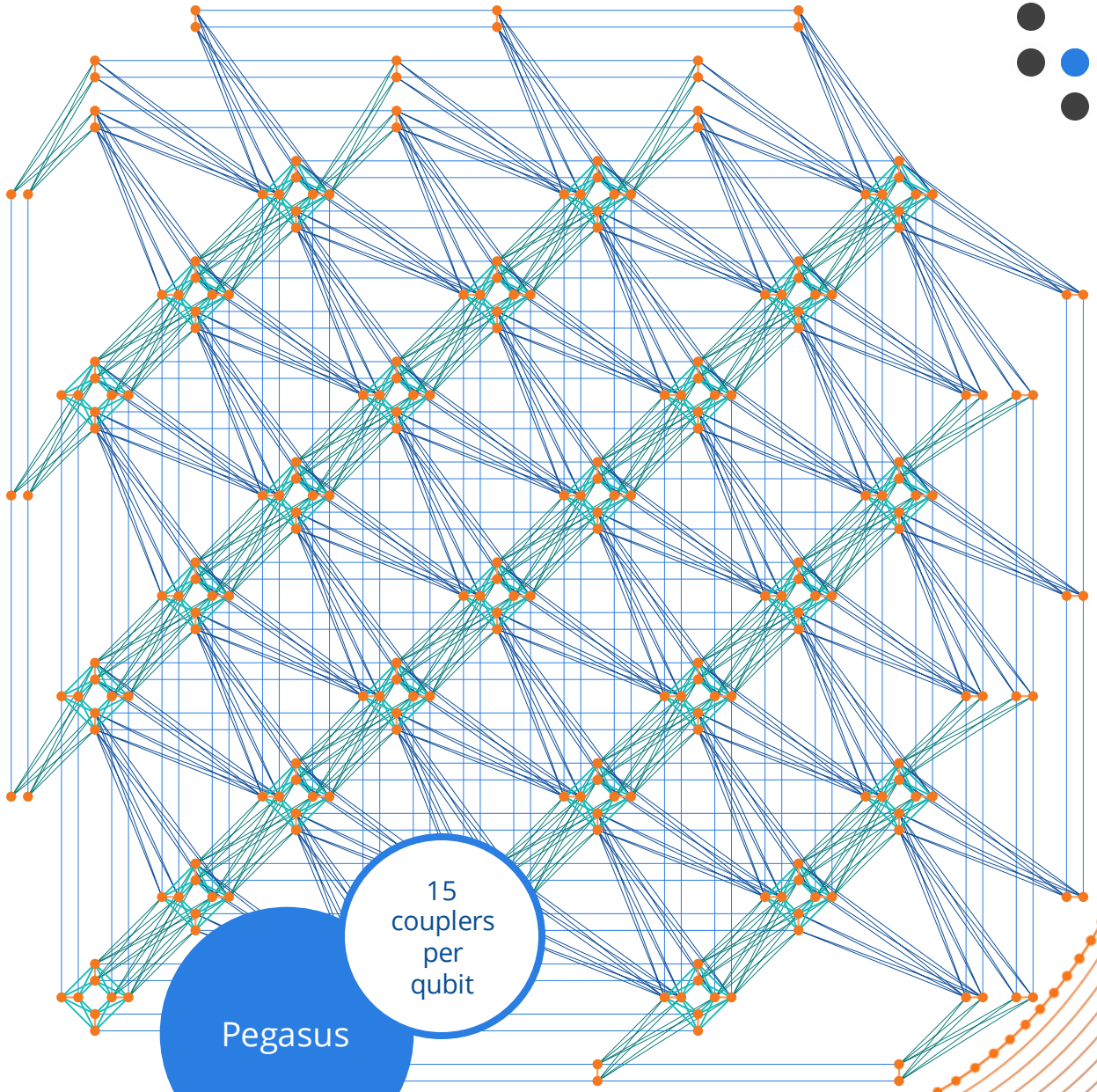
Line
=
coupler

circle
=
qubit



6
couplers
per
qubit

Chimera

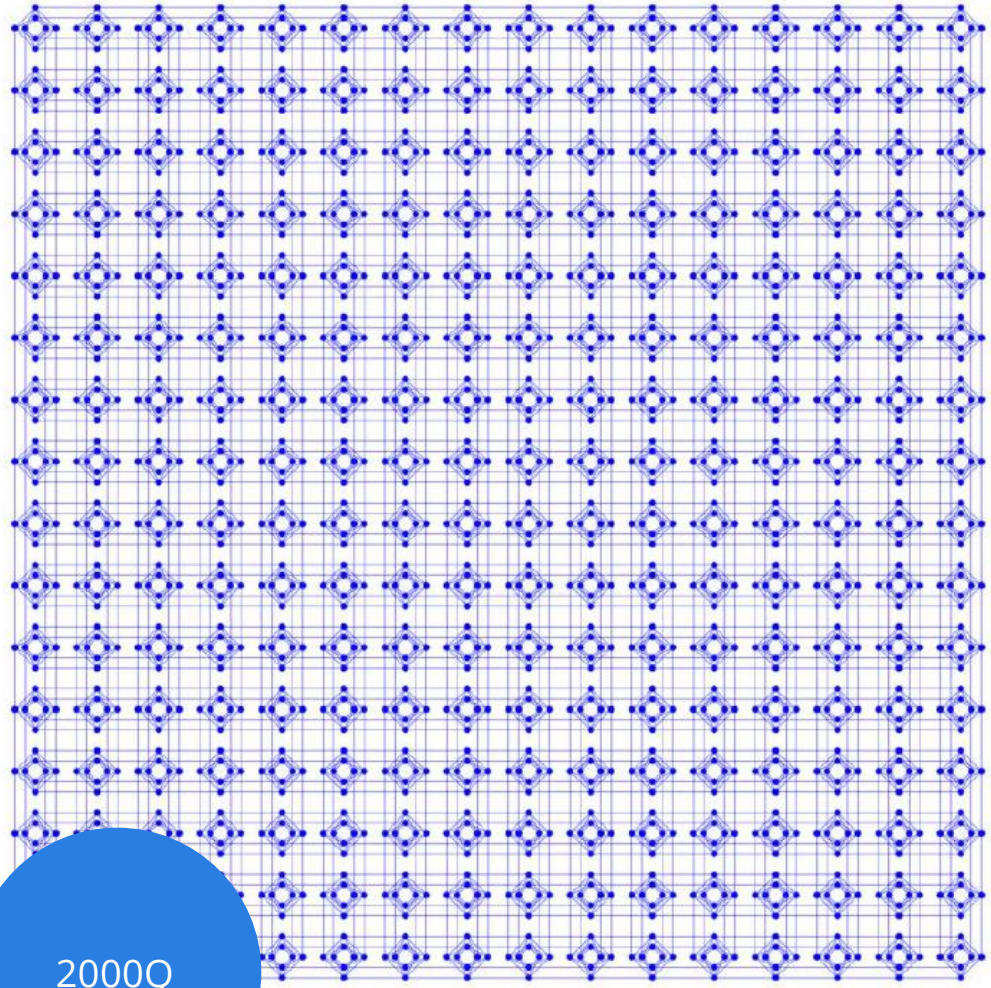


15
couplers
per
qubit

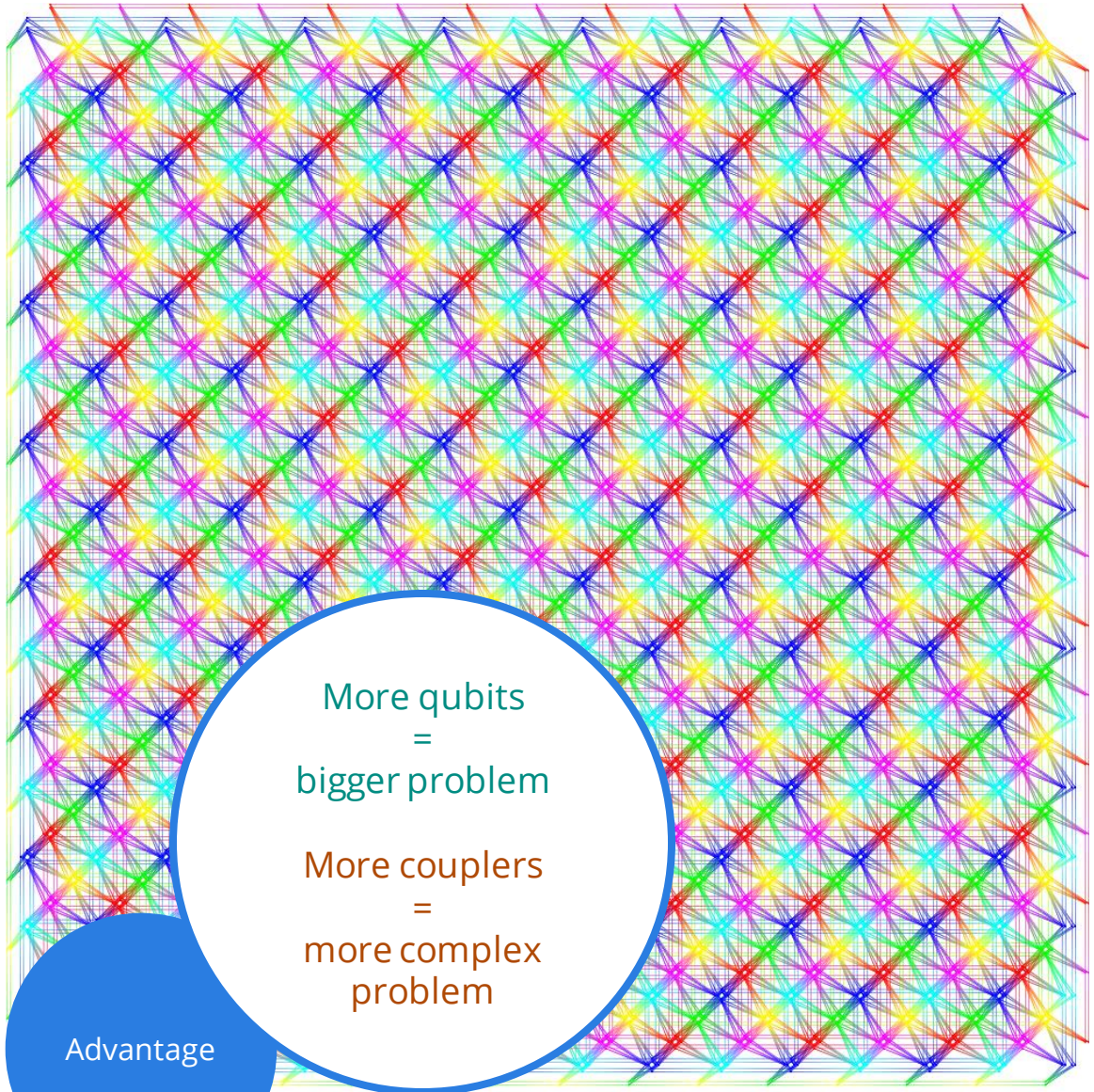
Pegasus

Copyright © D-Wave Systems Inc.

The Chip – Processor Layout



2000Q



Advantage

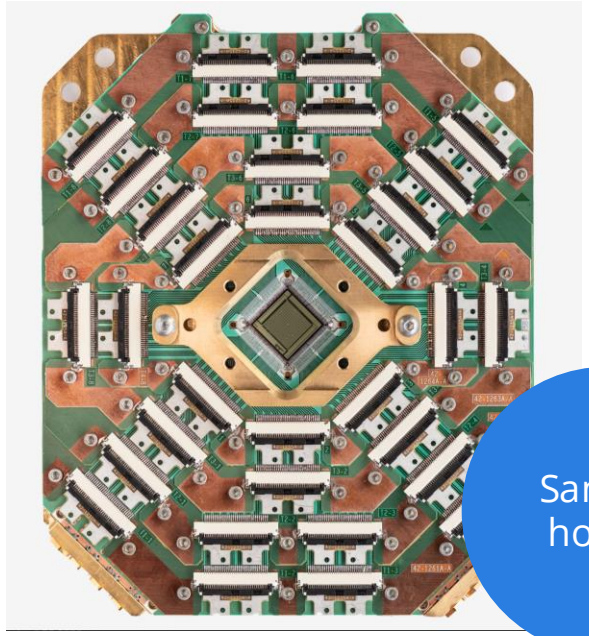
More qubits
=
bigger problem

More couplers
=
more complex problem

Copyright © D-Wave Systems Inc.

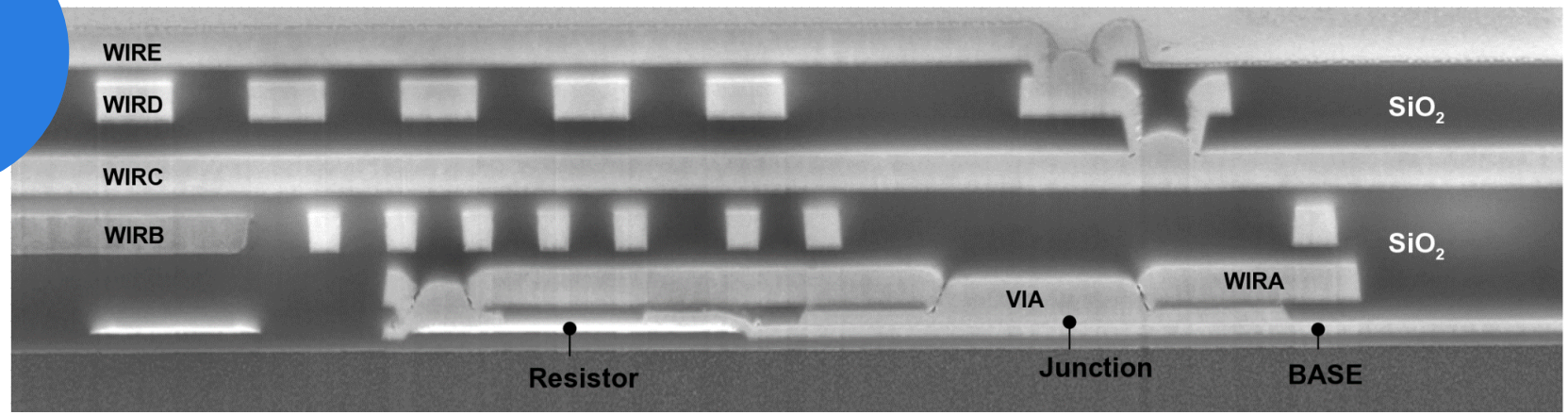
The Chip - Fabrication

- 3D integration
- On top of a silicon wafer
- Interspersed metal and dielectric layers
- Vias
- Josephson junctions
- Qubits and control circuitry are on the same chip



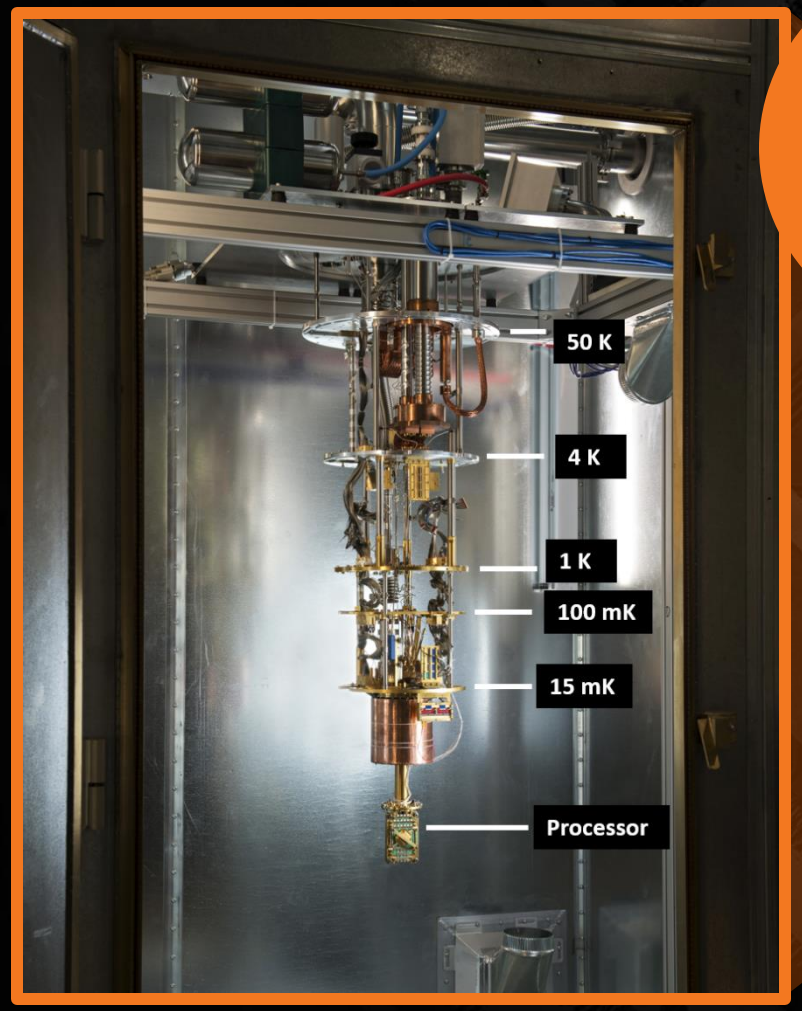
Sample holder

Cross section



Copyright © D-Wave Systems Inc.

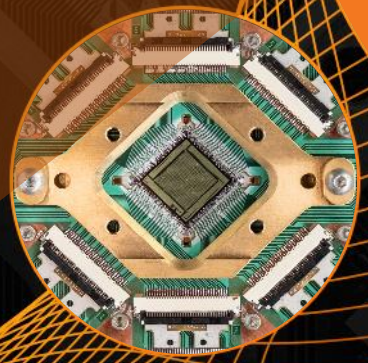
The Fridge - What's in the Box?



$P \sim 25$ kW

$B \lesssim 1$ nT

$T \sim 15$ mK



Copyright © D-Wave Systems Inc.

advantage

New Topology

Higher connectivity

More compact embeddings

Annealing Quantum Processor Design

5000+ Qubits

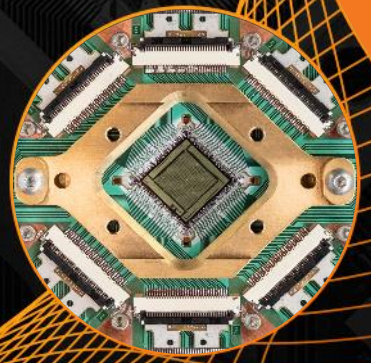
35,000+ Couplers

Superconducting Circuit Fabrication

1M+ Josephson junctions

Chip active area $(8.4mm)^2$

110m of wiring

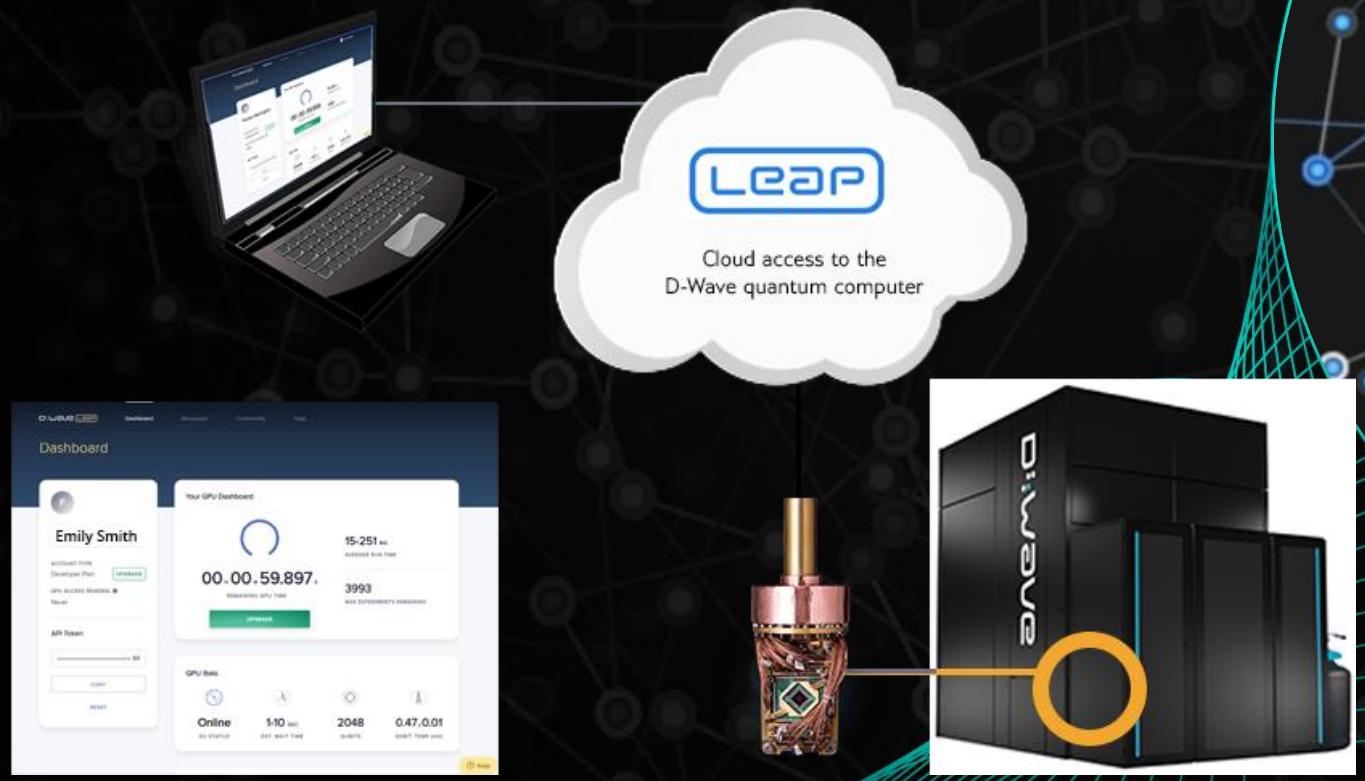


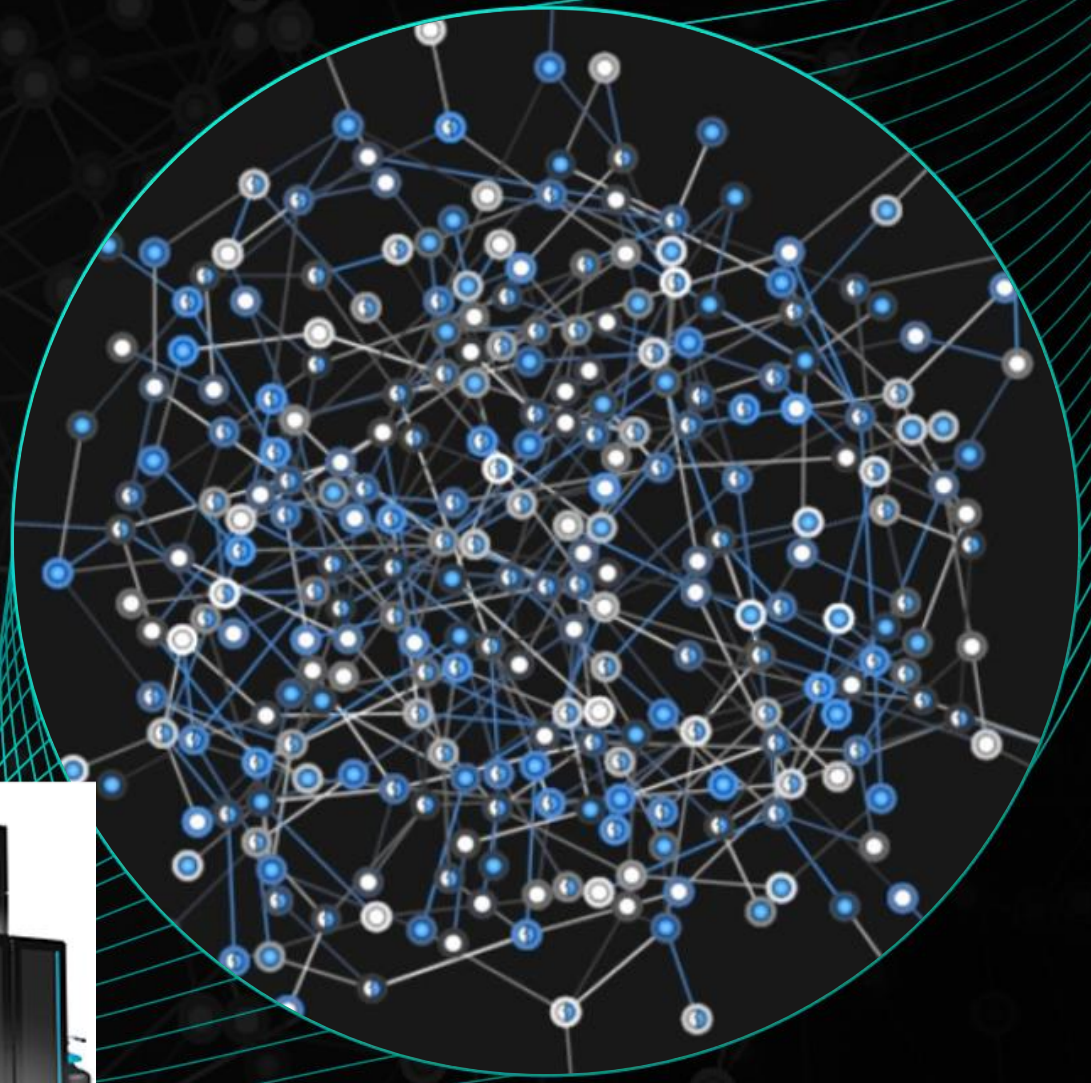
Copyright © D-Wave Systems Inc.

The Service – Leap

Cloud-based access to quantum and hybrid problem-solving resources

https://cloud.dwavesys.com/leap/signup/





Copyright © D-Wave Systems Inc.