Computer Organisation Laboratory

CS39001

Verilog Assignment 1

Group 15

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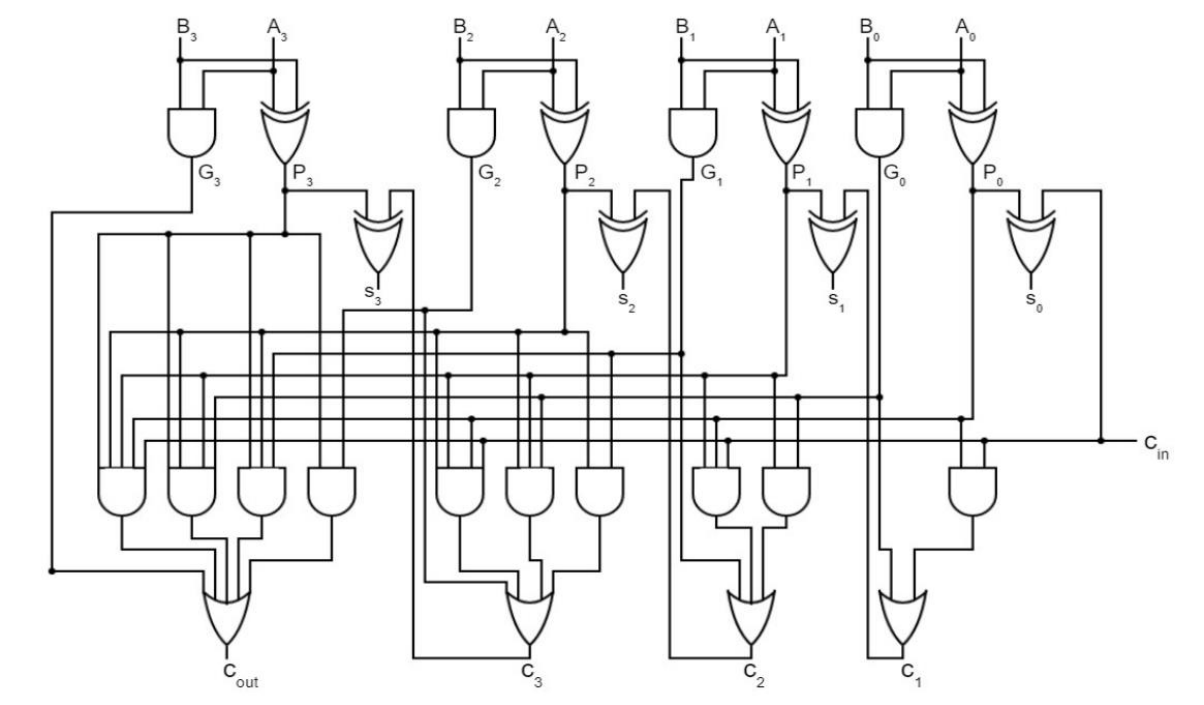
Part - II

a) 4-bit Carry Look-ahead Adder



By using a carry look-ahead adder, we can reduce the delay in calculating the sum by simultaneously calculating the carries instead of waiting for them like we do in case of ripple carry adders.

To achieve this, we define two functions for each i^{th} bit. These are:

$$G_i = A_i \cdot B_i$$

$$P_i = A_i \oplus B_i$$

Here, G_i and P_i are generate and propagate functions of stage i.

- A 4-bit adder has four carry-out signals:

$$c_1 = G_0 + P_0c_0$$
$$c_2 = G_1 + P_1G_0 + P_1P_0c_0$$
$$c_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0c_0$$
$$c_{out} = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0c_0$$

- In the Carry look-ahead design, the delays are as follows:

  1 for all P_i and G_i
  2 for all c_i
+ 1 for all s_i
———————————
  4 gate delays

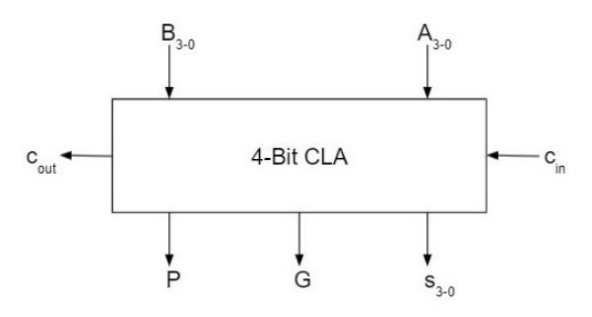
So, in this part, we have designed a 4-bit carry look-ahead adder with two 4-bit numbers and a carry-in bit as input, and then using the mechanism described above, we output the 4-bit sum and the carry-out bit.

b) In this part, we are comparing the delay of a 4-bit carry look-ahead adder with a 4-bit ripple carry adder.

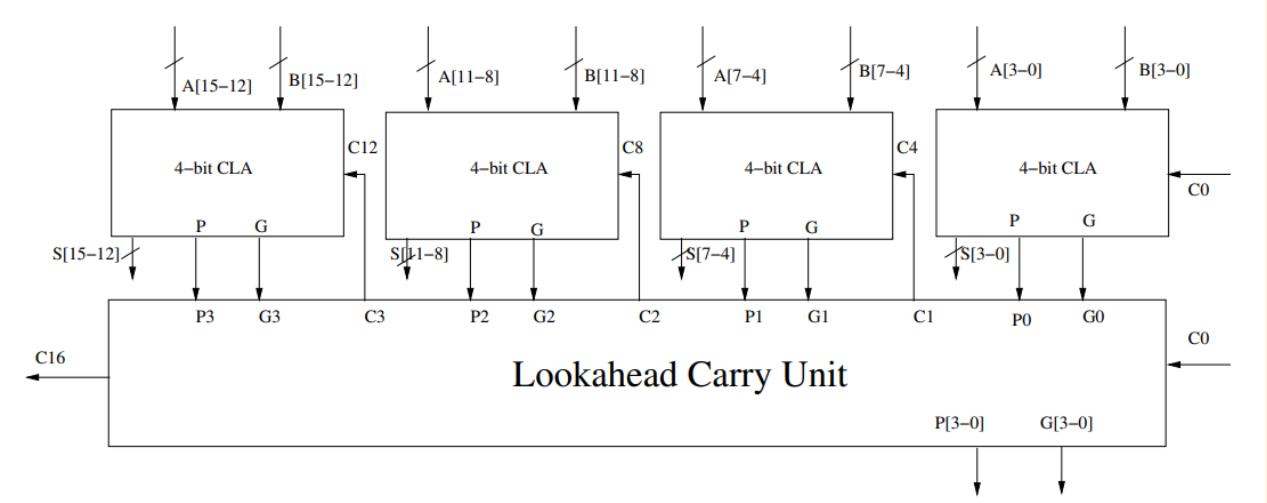
Circuit	Delay (in ns)
4-bit CLA	2.123
4-bit RCA	1.687

c) 16-bit Carry Look-ahead Adder

i) Here, we are augmenting an already created 4-bit CLA. This is done by adding two more output ports named P and G representing the block propagate and block generate for the next level.

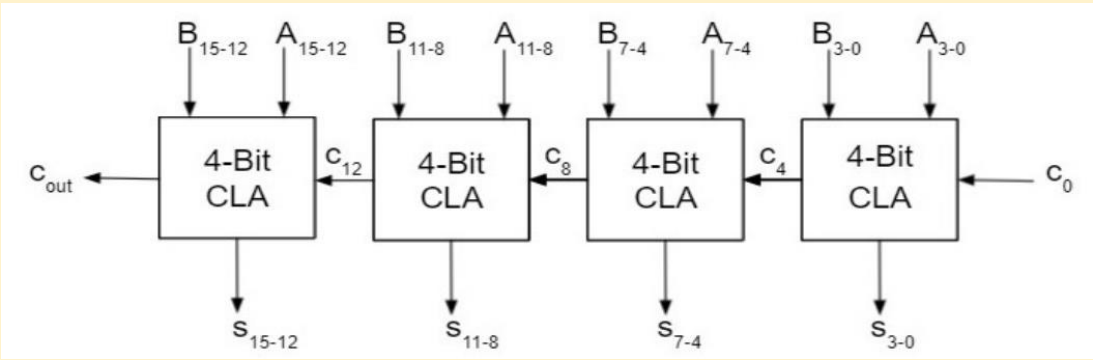


ii) Here, we are designing a Look-ahead Carry Unit, which takes the block propagate and block generate from the previous level as input, and computes the carry bit, block propagate and block generate for the next level. After designing this unit, we integrate it with four 4-bit augmented CLAs to design a 16-bit Carry Look-Ahead Adder.



iii) Here, we are going to compare the delays of the 16-bit CLA designed using the Look-ahead Carry Unit and the 16-bit Carry Look-ahead Adder when the carry is just rippled in without using the second layer of look-ahead carry unit.

Circuit	Delay (in ns)
16-bit CLA with LCU	3.623
16-bit CLA without LCU	3.768 ns



iv) Here, we are comparing the speed and the look-up table cost of the FPGA of 16-bit RCA and 16-bit CLA with Look-ahead Carry Unit.

Circuit	Delay (in ns)
16-bit CLA with LCU	3.623
16-bit RCA	6.167

Circuit	Slice LUTs used
16-bit CLA with LCU	29
16-bit CLA without LCU	43

Best case achievable delays:

Circuit	Best case Delays
4-bit CLA	2.000 ns
4-bit CLA augmented	2.129 ns
16-bit CLA ripple	3.768 ns
16-bit CLA LCU	3.623 ns