EEL 4930/5934 - System-on-Chip Design

Spring 2025

Final Project Report

Group 4: Joshua Restuccia, John Loyer, Devon Limcangco, Gabriel Machado

Problems Faced:

For this project, our initial idea for the architecture was to use the AXI Stream FIFO to stream audio data to the PWM module so that the PWM module could read data on its own clock rather than when the data was sent. The Microblaze would send audio data to the FIFO manually for task 3 and then use AXI CDMA to send the data to the FIFO in task 4. The first problem was that in the AXI Stream FIFO, the write port was a single register at a single address and by default, AXI CDMA only does incremental address DMA. There was one exception to this which meant we had to use the keyhole mode in the CDMA to get it to do fixed address DMA transactions. This led to another problem which was that the keyhole mode also turned it into a burst transaction and the current AXI SmartConnect bus we were using for all communication does not support burst transactions. To solve this, we added an AXI Interconnect in addition to the AXI SmartConnect which does support burst transfer. This is also explained in the walkthrough video starting at around 12:30.

What you learned:

Working on this project, we learned about the several different types of Vivado AXI FIFO IP and what their capabilities are. We learned about some of the differences in capabilities between the AXI CDMA and AXI DMA IP. We also learned how to represent certain audio tones so that it could be turned into sound using PWM. We also learned about the BRAM Generator and BRAM Controller IP and how that can be used in an application. We also learned about the differences between the AXI SmartConnect and AXI Interconnect (deprecated).

Other:

Demo Video: https://youtu.be/K_KaSI-Xa2U

Project Walkthrough: https://youtu.be/Mh9qgDknTXY