WELCOME

Embedded System Hardware Architectures, *Introduction*

Lecture 1 April 1st 2024

UCSC Silicon Valley Extension
PROFESSIONAL EDUCATION

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Schedule

Date:	Start Time:	End Time:	Meeting Type:	Location:
Mon, 04-01-2024	6:30 p.m.	9:30 p.m.	Flexible	SANTA CLARA / REMOTE
Mon, 04-08-2024	6:30 p.m.	9:30 p.m.	Flexible	SANTA CLARA / REMOTE
Mon, 04-15-2024	6:30 p.m.	9:30 p.m.	Flexible	SANTA CLARA / REMOTE
Mon, 04-22-2024	6:30 p.m.	9:30 p.m.	Flexible	SANTA CLARA / REMOTE
Mon, 04-29-2024	6:30 p.m.	9:30 p.m.	Flexible	SANTA CLARA / REMOTE
Mon, 05-06-2024	6:30 p.m.	9:30 p.m.	Flexible	SANTA CLARA / REMOTE
Mon, 05-13-2024	6:30 p.m.	9:30 p.m.	Flexible	SANTA CLARA / REMOTE
Mon, 05-20-2024	6:30 p.m.	9:30 p.m.	Flexible	SANTA CLARA / REMOTE
Mon, 06-03-2024	6:30 p.m.	9:30 p.m.	Flexible	SANTA CLARA / REMOTE
Mon, 06-10-2024	6:30 p.m.	9:30 p.m.	Flexible	SANTA CLARA / REMOTE

Agenda (1)

1. April 1st 6:30pm – Online
   - Tear Down Analysis, Inter-IC communications
   - Basic Concepts (Serial vs Parallel bus)
   - Quiz 1 (closed Notes)

2. April 8th 6:30pm Online

Microcontroller/ Microprocessor Systems / SoC Concepts

   - Quiz 2 (closed Notes)

Agenda (2)

3. April 15th (?) Monday 6:30pm: Online

- Volatile Memories (System and Architectures)
- Quiz 3 (closed Notes)

4. April 22nd(?) Monday 6:30pm: Online

- *Non-Volatile Memories (System and Architectures)*
- Quiz 4 (closed Notes)

Agenda (3)

5. April 29th Monday 6:30pm: Online

- *Special Functions Circuitry in Embedded Processors ColdFireV1 v S5D9 Synergy v 8051: FPU, DMA*
- Quiz 5 (closed Notes)

6. May 6th Monday 6:30pm: Online

- *Special Function Circuitry: GPIO, UART*
- *Hardware System Design Considerations: IC Packaging, IC Thermal Considerations*
- Quiz 6 (closed Notes)

Agenda (4)

7. May 13th Monday 6:30pm: Online

- *Embedded systems in Makers Faire DIY movement, single board computers, industry trends and best practices.*
- *Guest Speaker 1: CM, EspressoBin / Dragon Board/ other SBCs*
- *Project 1 Presentation Due*
- Quiz 7 (Closed Notes)

8. May 20th Monday 6:30pm: Online

- *Special Function Circuitry: PWM, WDT, PMIC*
- *Embedded System Design Methodology: FPGA, ASIC, Full-Custom Design, COTs*
- *Guest Speaker 2: "FPGA and SOMs"*
- Quiz 8 (Closed Notes)

(Memorial Day on May 27th – no class)

Agenda (5)

9. Jun 3rd Monday 6:30pm: Online

- *Special Function Circuitry: ADC , DAC, RTC*
- *Form Factor, System Benchmarking*
- *Guest Speaker 3: "Age of AI and the Transformation of Compute Infrastructure"*
- Quiz 9 (Closed Notes)

10 Jun 10th Monday 6:30pm: Online

- *CPU v GPU v TPU v NPU v VPU v XPU v DPU*
- *Software Considerations: OS, RTOS, Baremetal, Middleware*
- *Industry Case Studies*
- ***Project2 + Presentation Due,***
- ***Course Wrap Up***
- **Final Exam (Open Notes)**

Class Introduction

- Your name
- Your job title
- Company
- Why are you taking this class?

Class Expectations

- What you want to gain out of this class?

Grading

- Quizzes (9 quizzes) – 45% each
- Project1 – 15%
- Project2 – 20%
- Final Exam – 20%

Project

Choose one of the following:

1. 4-page (double spaced) minimum Research on the Topic of your choice. Topic should be related to class materials eg Main Memory development over the last 20 years.
2. Read a book on class related material and write a 4-page book review. Review topics should summarize the contents of the book and include your feedback and recommendations.
3. Designing an embedded system on paper - Choose a hardware project of your choice and draft out the system functional block diagram (1 page). Explain why you choose the components, what is the functional purpose of the component (3 page).

Project Grading

Grading to be based on:

Content: (60%)

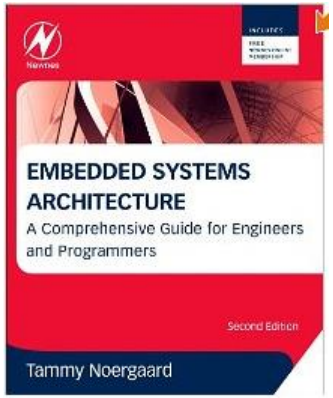
1. **Technical Accuracy**
2. **Addresses Project Complexity**
3. **Quality of Response during Q&A**

Presentation: (40%)

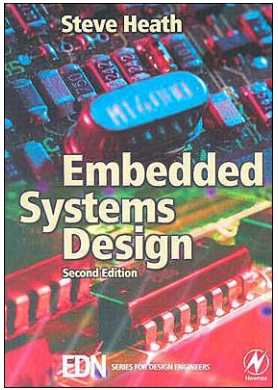
1. **Organization**
2. **Visual Aids**
3. **Time Allotment**

Suggested Readings 1

- Embedded Systems Architecture, Second Edition: A Comprehensive Guide for Engineers and Programmers [Hardcover]
- Tammy Noergaard (Author)
- Hardcover: 672 pages
- Publisher: Newnes; 2 edition (December 28, 2012)
- Language: English
- ISBN-10: 0123821967
- ISBN-13: 978-0123821966



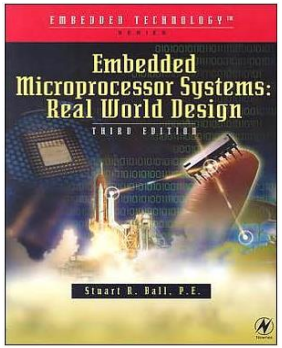
- Embedded Systems Design
- Steve Heath
- Second Edition
- ISBN: 0750655461
- Format: Paperback, 430pp
- Pub. Date: December 2002
- Publisher: Elsevier Science & Technology Books



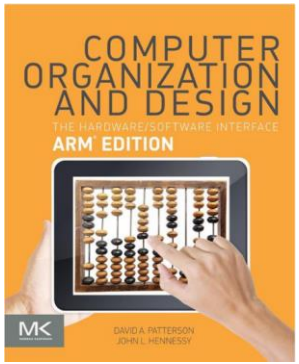
- Source attributed to www.amazon.com

Suggested Readings 2

- **Embedded Microprocessor Systems (Embedded Technology Series): Real World Design**
- Stuart Ball
- Publisher: Elsevier Science & Technology Books
- Pub. Date: January 2002
- ISBN-13: 9780750675345
- 362pp
- Edition Description: THIRD



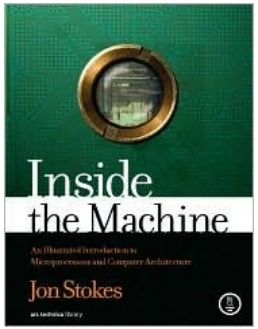
- **Computer Organization and Design, ARM Edition: The Hardware/Software Interface (The Morgan Kaufmann Series in Computer Architecture and Design) [Paperback]**
- David A. Patterson John L. Hennessy
- **Series:** The Morgan Kaufmann Series in Computer Architecture and Design
  Paperback: Publisher: Morgan Kaufmann; ARM edition
  Language: English
- ISBN-13: 978-0128017333
- ISBN-10: 0128017333



Source attributed to www.amazon.com

Suggested Readings 3

- Inside the Machine:
- John Stokes
- Publisher: No Starch Press San Francisco, CA
- Pub. Date: November 2006
- ISBN-13: 9781593271046
- 292pp



- Embedded Systems Design with Platform FPGAs: Principles and Practices [Hardcover]
- Ronald Sass (Author), Andrew G. Schmidt (Author)

- Publisher: Morgan Kaufmann; 1 edition (August 11, 2010)
- Language: English
- ISBN-10: 0123743338
- ISBN-13: 978-0123743336

Source attributed to www.amazon.com

What is an embedded system?

Typically a microprocessor-based system not thought of as a PC:

- Comprises: Memory,Storage,Buses,Micro processor
- Specialized functions circuitry
- eg. Cell phones, mp3 player, STB, routers

Terminology 1

Microprocessors (uP, MPU) - CPU that connects to external memory, I/O, Peripherals. Sometimes called GPPs

Microcontroller (uC/ MCU) – CPU Core, memory, I/O, peripherals integrated on chip

Embedded System – uP/uC based system not thought of as a PC. Example PDA, PND, PMPs etc.

DSP – Microprocessors specialized for signal processing applications.

Terminology 2 MCU Tools

I DE – Integrated Development Environment – Software package for application development. An IDE normally consists of a source code editor, a compiler and/or interpreter, build automation tools, and (usually) a debugger.

In Circuit Emulator - a hardware device used to debug the software of an embedded system. It is usually in the form of bond-out processor which has many internal signals brought out for the purpose of debugging. These signals tell about the state of a processor.

Bill of Material 1

MAXIM

MAX2312 EV KIT BILL OF MATERIAL

Date:5/1/00
BOM REV:E
BOARD REV:C
MODIFIED for 190MHz IF
* Maxim will supply component

	DESIGNATION	QTY	DESCRIPTION	E #
*	C1, C3, C9 -C11, C13, C14, C21, C22, C28, C35, C37, C38, C42	14	0.01uF 10v Min, 10% Ceramic Capacitor (0402) MURATA GRM36X7R103K016A	EC
*	C2, C4, C8, C12, C23 - C25	7	330pF 10% 10V Min, Ceramic Capacitor (0402) MURATA GRM36X7R331K050A	EC
*	C5	1	1.5 pF +/- .1pF 16V Min, Ceramic Capacitor (0402) MURATA GRM36COG1R5B050A	EC
*	C6, C7	2	12 pF 5% 16V Min, Ceramic Capacitor (0402) MURATA GRM36COG120J050A	
	C15, C26, C32, C36, C39, C40, R6, R10 R15, R17, R19 - R21, R25, R27-R30, R36,	18	**Do Not Install**	
*	C16, C33, C34	3	47pF 25v Min, 5% Ceramic Capacitor (0402) MURATA GRM36COG470J050A	EC

•Source attributed to www.maxim.com

Bill of Material 2

MAXIM

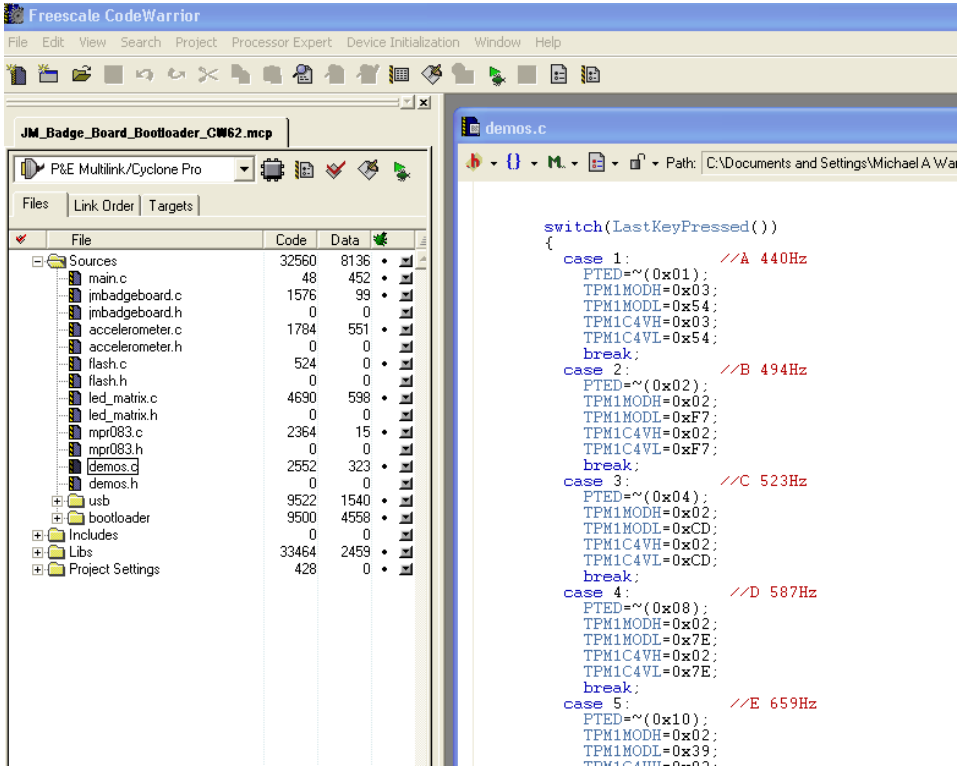
MAX2312 EV KIT BILL OF MATERIAL

Date:5/1/00
BOM REV:E
BOARD REV:C
* Maxim will supply component

*	L2	1	24 nH Inductor 0805CS-240XJBC 5% Coilcraft	EL
*	L4	1	180nH Inductor 0805CS - 181TKBC 10% Coilcraft	EL
*	L6	1	270nH Inductor 0805CS - 271TKBC 10% Coilcraft	EL
	J1-J5, J7, J8	7	SMA EDGE MT CONNECTOR 142-0701-801 DIGI-KEY J502-ND **NOTE: CUT CENTER PIN TO APPROXIMATELY 1/16" LENGTH.**	
	JU2, JU3, JU10, JU11	4	SHUNT Digi-key S9000-ND	
	Q1	1	LEAVE SITE OPEN	
	D1	1	LEAVE SITE OPEN	
*	D4	1	VARACTOR DIODE ALPHA SMV1255-003	ED0070
*	U1	1	MAX2312EEI 28QSOP	EU0432
	JU2, JU3, JU10, JU11, VCC, GND, DGND	7	1X2 Header Digi-key S1012-36-ND	
	\STBY\, \BUF_EN\, DIV_SEL, \SHDN\	4	1X3 Header Digi-key S1012-36-ND	
	DATA, \EN\, CLK,	1	2X6	

•Source attributed to www.maxim.com

Codewarrior IDE



Source attributed to– Freescale.com Codewarrior IDE

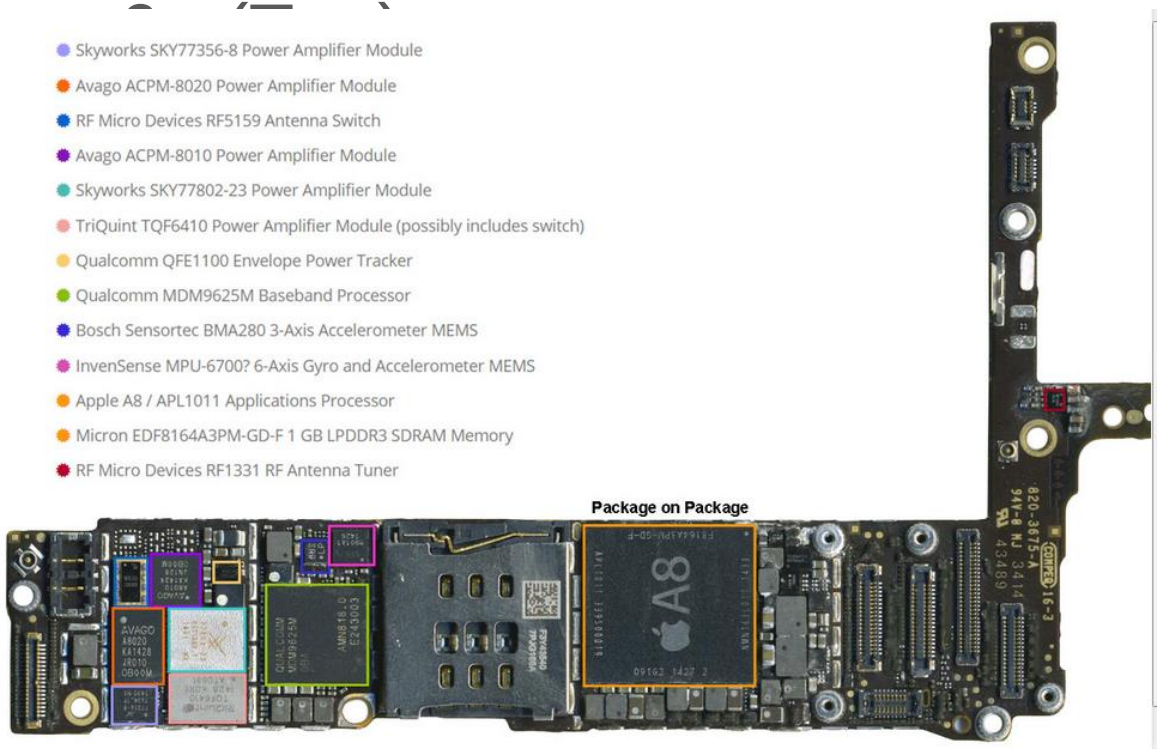
Terminology MCU Tools 3

Evaluation and Development Kit - low costs, easy to use hardware tools.

3rd Party tools – H/W S/W tools made by non MCU vendor

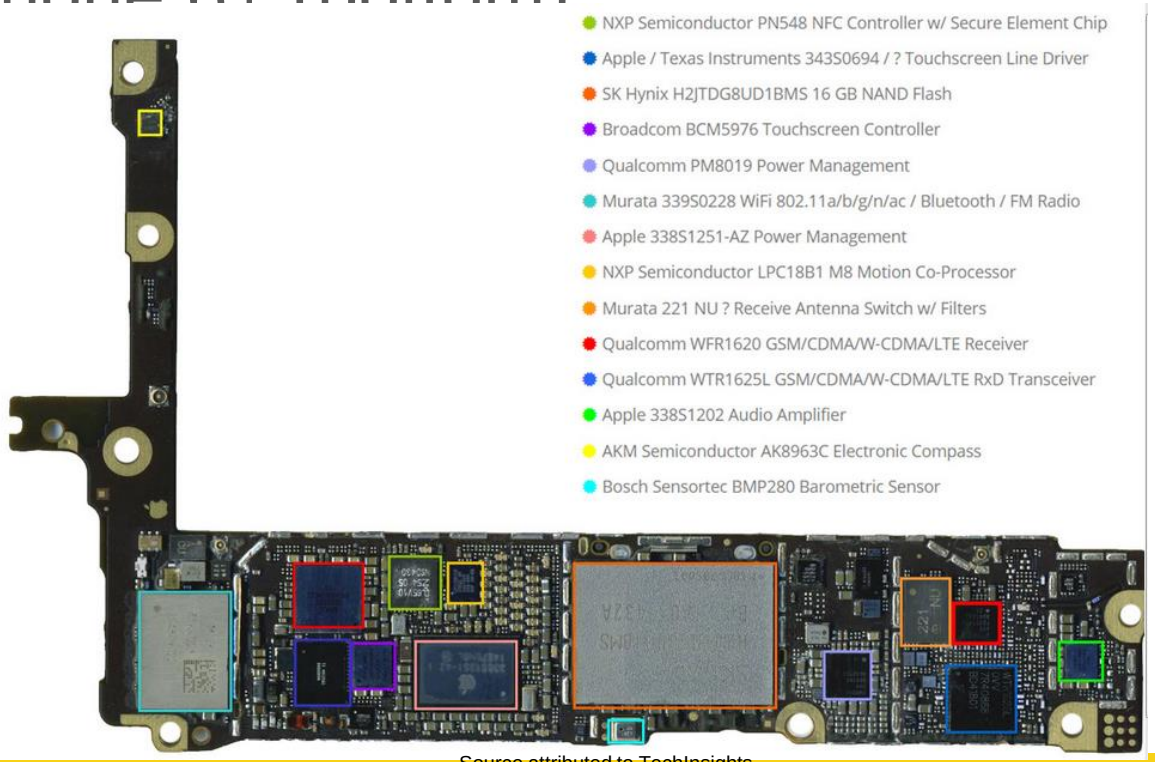
Tear Down Analysis 1
Apple iPh

- Skyworks SKY77356-8 Power Amplifier Module
- Avago ACPM-8020 Power Amplifier Module
- RF Micro Devices RF5159 Antenna Switch
- Avago ACPM-8010 Power Amplifier Module
- Skyworks SKY77802-23 Power Amplifier Module
- TriQuint TQF6410 Power Amplifier Module (possibly includes switch)
- Qualcomm QFE1100 Envelope Power Tracker
- Qualcomm MDM9625M Baseband Processor
- Bosch Sensortec BMA280 3-Axis Accelerometer MEMS
- InvenSense MPU-6700? 6-Axis Gyro and Accelerometer MEMS
- Apple A8 / APL1011 Applications Processor
- Micron EDF8164A3PM-GD-F 1 GB LPDDR3 SDRAM Memory
- RF Micro Devices RF1331 RF Antenna Tuner



Source attributed to TechInsights

Tear Down Analysis 2
Apple iPhone 6+ (bottom)



Source attributed to TechInsights

Tear Down Analysis 3
Apple iPhone 6+/6/ 5s Comparison

Features			
Specifications	iPhone 5S A1533	iPhone 6 QTT	iPhone 6 Plus QTT
Operating System	iOS 7	iOS 8	iOS 8
Display	4" IPS (1136x640)	4.7" IPS (1334x750)	5.5" IPS (1920x1080)
Battery	1560 mAh	1810 mAh	2915 mAh
Camera	8 Megapixel with 1.5µ pixels, f/2.2 + 1.2MP Front	8 Megapixel with 1.5µ pixels, f/2.2 + 1.2MP Front	8 Megapixel with 1.5µ pixels, f/2.2 OIS + 1.2MP Front
Connectivity & Sensors	2.4 + 5GHz 802.11 a/b/g/n Bluetooth 4.0	2.4 + 5GHz 802.11 a/b/g/n/ac Bluetooth 4.0	2.4 + 5GHz 802.11 a/b/g/n/ac Bluetooth 4.0
NAND	16 GB	16 GB	16 GB
SDRAM	1 GB	1 GB	1 GB
Processor	Apple A7 + M7 1.3 GHz Dual-Core 64 Bit ARMv8 Processor	Apple A8 + M8 1.4 GHz Dual-Core 64 Bit ARMv8 Processor	Apple A8 + M8 1.4 GHz Dual-Core 64 Bit ARMv8 Processor
BB+XCR	Qualcomm MDM9615M Qualcomm WTR1605L	Qualcomm MDM9625M Qualcomm WTR1625L Qualcomm WFR1620	Qualcomm MDM9625M Qualcomm WTR1625L Qualcomm WFR1620

teardown.com

Source attributed to TechInsights

Tear Down Analysis 4
Apple iPhone 6+/6/ 5s BOM

Tear Down Analysis 5
Sonos Audio system

Fig.1: Sonos system comprises ZP100 (center) with integrated 50-W amplifier, ZP80 and wireless controller (left).

Source attributed to EETimes – Under the Hood

Tear Down Analysis 6
Sonos

Source attributed to EETimes – Under the Hood

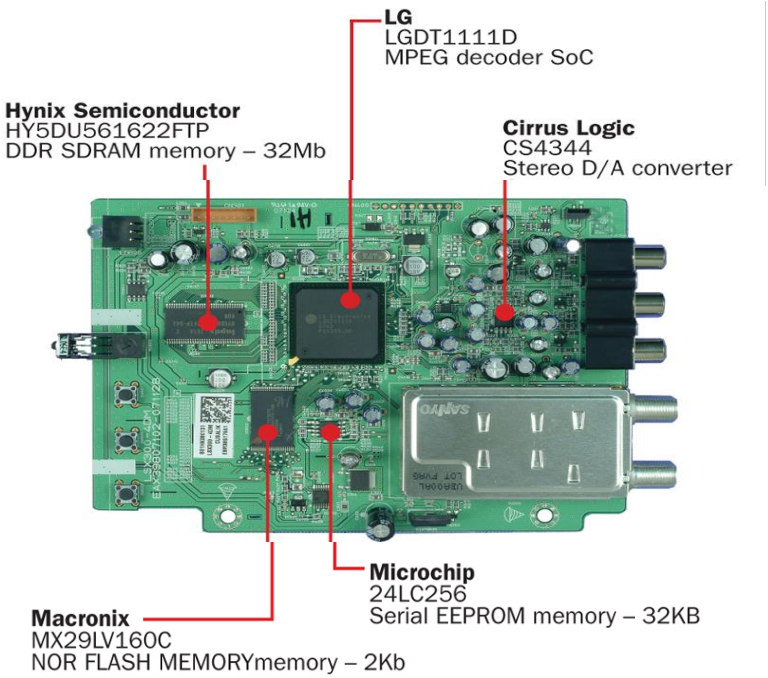
Tear Down Analysis 7
Sonos

Again it has a Renesas SH-4 and M16 microcontroller, a TI '5402 DSP, RealTek RTL8139CL Ethernet MAC, Atmel OTP EPROM, two ISSI 16-Mbyte x 8 synchronous DRAMs, the Samsung NAND (32 Mbytes) etc However, though the ZP80 has only two Ethernet ports, it still uses a Marvell 88E6060 6-port Ethernet switch (versus the Kendin controller on the ZP100) with an LF-H20P-1 magnetics chip.

The controller relies on an Atheros AR2414A mini-PCI card and instead of 32 Mbtyes has 16 Mbytes of Samsung NAND flash. The controller is also differentiated by having a ball-bearing-based motion sensor and a Sharp 1/4-VGA transflective LCD display. Again, a Renesas M16 microncontroller is included, but this time to also manage the control buttons and scroll wheel.

Source attributed to EETimes – Under the Hood

Tear Down Analysis 8
Converter Box

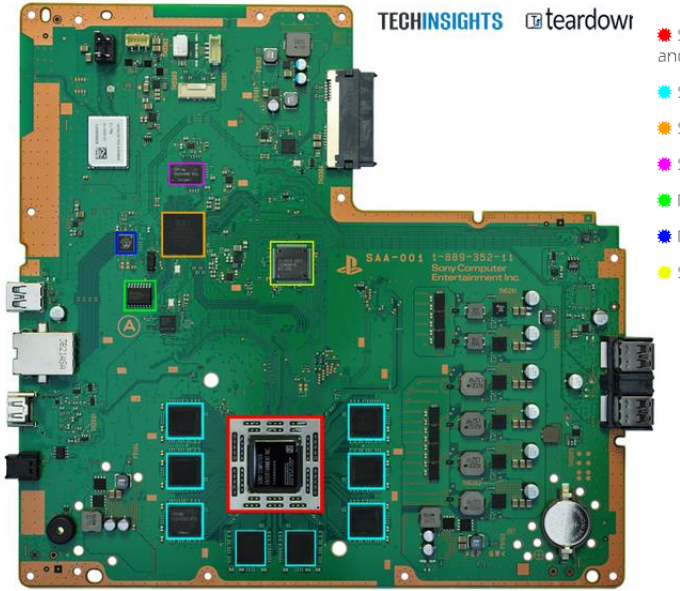


Source attributed to EETimes – Under the Hood

Tear Down Analysis 9
Sony Playstation 4

Source attributed to TechInsights

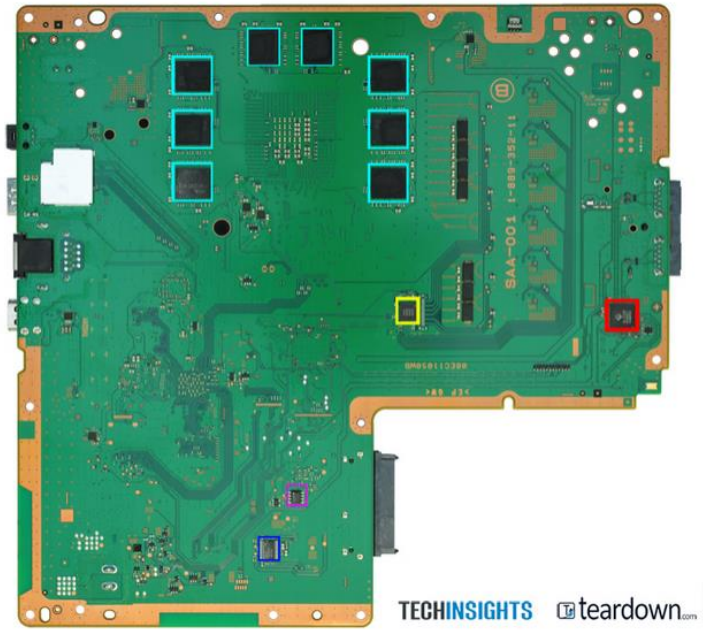
Tear Down Analysis 10
Sony P[illegible]



- SCEI (Sony Computer Entertainment, Inc.) CXD90026G SoC (includes AMD "Jaguar" Cores and AMD Radeon Graphics GPU)
- Samsung K4G41325FC-HC03 4 Gb (512 MB) GDDR5 SGRAM (total of 16 x 512 MB = 8 GB)
- SCEI CXD90025G
- Samsung K4B2G1646E-BCK0 2Gb DDR3 SDRAM
- Macronix MX25L25635FMI 256Mb Serial Flash Memory
- Marvell 88EC060-NNB2 Ethernet Controller
- SCEI 1328KM476

Source attributed to TechInsights

Tear Down Analysis 11
Sony Playstation 4



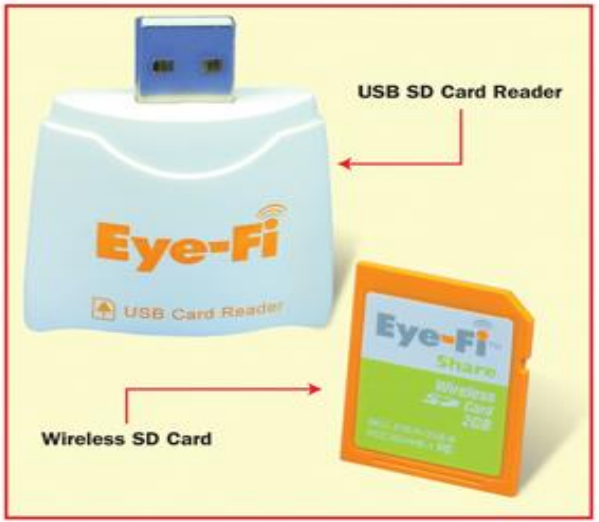
- Genesys Logic GL3520 USB 3.0 Hub Controller
- Samsung K4G41325FC-HC03 4 Gb (512 MB) GDDR5 SGRAM
- International Rectifier 3585B N326P IC2X
- Macronix MXIC B01 25L1006E CMOS Serial Flash Memory
- TI 53123A 2AK64 D756

Source attributed to TechInsights

Tear Down Analysis 12
Sony Playstation 4

Source attributed to TechInsights

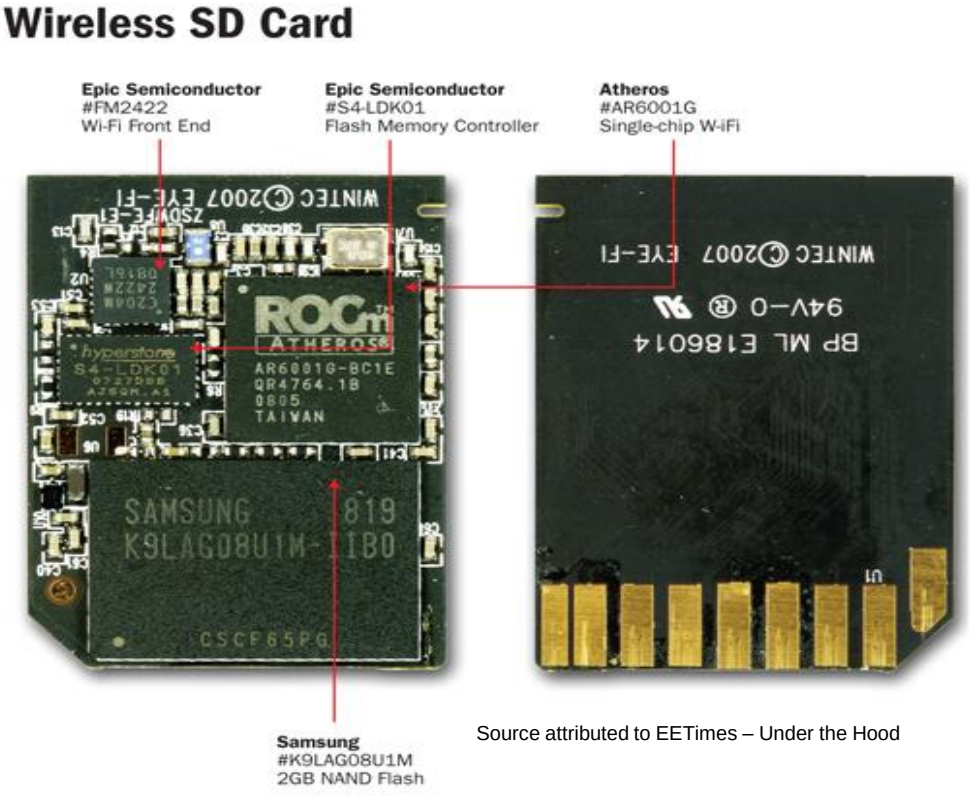
Tear Down Analysis 13
Wireless SD Ca



A Wi-Fi-enabled SD card makes it easy and affordable to add Wi-Fi connectivity to any digital camera with an SD card slot

Source attributed to EETimes – Under the Hood

Tear Down Analysis 14
Wireless SD Card



Source attributed to EETimes – Under the Hood

Tear Down Analysis 15
Amazon Kindle Fire

Amazon Kindle Fire Front

- Texas Instruments TWL6030B107
  Power Management IC with Switch Mode Charger
- Package-on-package - Elpida B4064B2PB
  Multichip Memory Package 512 MB DDR2 Mobile
- Package-on-package - Texas Instruments OMAP4430
  Applications Processor
- Texas Instruments SN75LVDS83B - FlatLink 10-135 MHz Transmitter
- Samsung KLM8G2FEJA - 8GB moviNAND Flash memory module
- Jorjin WG7310 – Wireless Connectivity Module
  containing WL1270B 802.11b/g/n WiFi + Bluetooth and
  Triquint TQM679002 WLAN/Bluetooth Front-End Module

Source attributed to TechInsights

Tear Down Analysis 16
Amazon K[illegible] Fire

- Texas Instruments TLV320AIC3110
  Low-Power Audio Codec With 1.3W Stereo Class-D Speaker Amplifier
- Texas Instruments SN74AVCH4T245
  4-Bit Dual-Supply Bus Transceiver

Source attributed to TechInsights

Tear Down Analysis 17
Amazon Kindle Fire

Primary Component Listing

•Package-on-Package with: Elpida B4064B2PB - Multichip Memory Package - 512 MB DDR2 Mobile SDRAM
Texas Instruments OMAP4430 – Applications Processor
•Samsung KLM8G2FEJA - 8GB moviNAND Flash memory module
•Texas Instruments SN75LVDS83B - FlatLink 10-135 MHz Transmitter
•Texas Instruments TWL6030B107 - Power Managment IC with Switch Mode Charger
•Jorjin WG7310 – Wireless Connectivity Module containing: Texas Instruments WL1270B 802.11b/g/n WiFi + Bluetooth and Triquint TQM679002 WLAN/Bluetooth Front-End Module
•Texas Instruments TLV320AIC3110 - Low-Power Audio Codec With 1.3W Stereo Class-D Speaker Amplifier
•Texas Instruments SN74AVCH4T245 - 4-Bit Dual-Supply Bus Transceiver
•ILITEK 21D7QS001K - Touch Screen Controller

Source attributed to TechInsights

Tear Down Analysis 18
Amazon Kindle Fire comparison

Features	Original Amazon Kindle Fire	Kindle Fire HD 8.9" 4G LTE 32GB	Kindle Fire HD 8.9" 16GB	Kindle Fire HD 7" 16GB	Google Nexus 7 8GB
Display	7" 1024 x 600	8.9" 1920 x 1200	8.9" 1920 x 1200	7" 1280 x 800	7" 1280x800
Battery	4400 mAh	6100 mAh?	6100 mAh?	4800 mAh?	4325 mAh
Camera		2MP?	2MP?	2MP?	1.2MP Front Camera
Wi-Fi/BT/GPS	802.11 b/g/n Bluetooth 2.1	MIMO 802.11 a/b/g/n Bluetooth	MIMO 802.11 a/b/g/n Bluetooth	MIMO 802.11 a/b/g/n Bluetooth	802.11 b/g/n Bluetooth 4.0 GPS
NAND	8GB	32GB	16GB	16GB	8GB
SDRAM	512MB	1GB?	1GB?	1GB?	1GB
Processor	TI OMAP 4430	TI OMAP 4470	TI OMAP 4470	TI OMAP 4460	NVIDIA Tegra 3
BB+XCR		Qualcomm?			

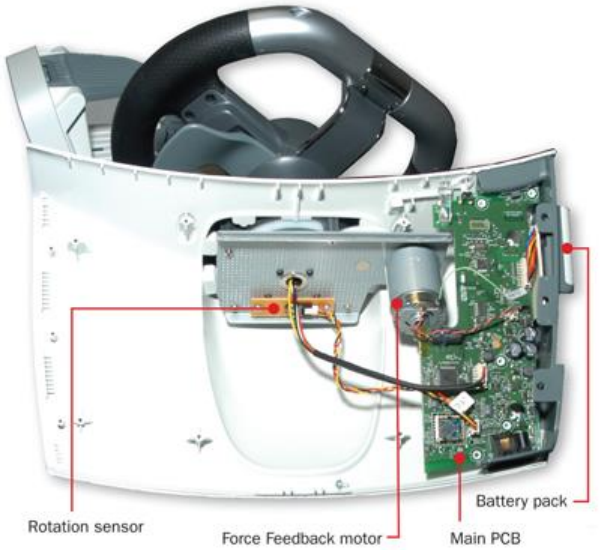
Cost	Amazon Kindle Fire	Kindle Fire HD* 8.9" 4G LTE 32GB	Kindle Fire HD* 8.9" 16GB	Kindle Fire HD* 7" 16GB	Google Nexus 7 8GB
	Dec-11	Sep-12	Sep-12	Sep-12	Sep-12
Display	$35	$45	$45	$35	$29
Touchscreen	$19	$20	$20	$15	$20
Battery	$11	$12	$12	$9	$11
Cameras		$4	$4	$4	$3
Wi-Fi/BT/GPS	$4	$6	$6	$4	$5
NAND	$10	$17	$9	$9	$6
SDRAM	$8	$4	$4	$4	$5
Processor	$18	$28	$28	$21	$25
BB+XCR		$27			
Non-electronic	$20	$16	$16	$14	$20
Other	$25	$36	$32	$30	$30
Supporting Materials	$3	$3	$3	$3	$4
Total	$153	$218	$179	$148	$158

* Estimate only since device has not been fully analyzed

Source attributed to TechInsights

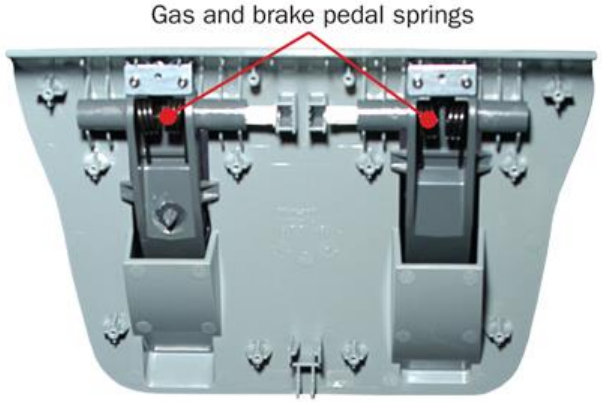
Tear Down Analysis 19
Xbox 360 driving

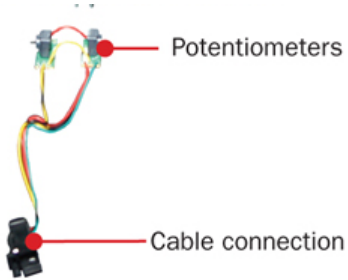
Bluetooth allows wireless control of the Xbox 360 driving experience.



Source attributed to EETimes – Under the Hood

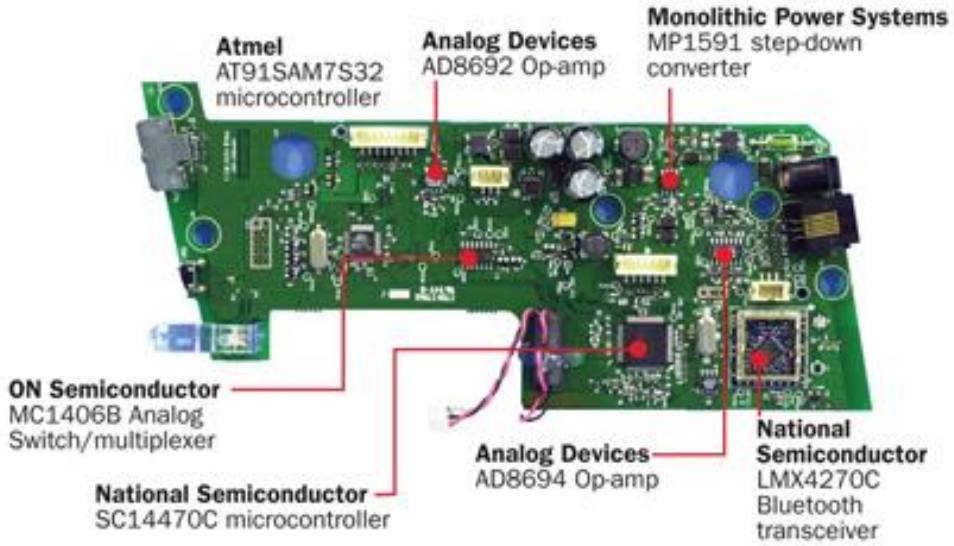
Tear Down Analysis 20
Xbox 360 driving





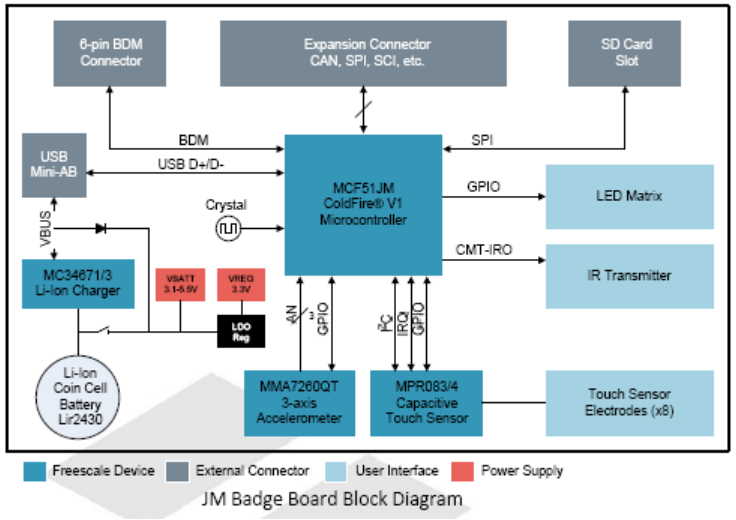
Source attributed to EETimes – Under the Hood

Tear Down Analysis 21
Xbox 360 driving



Source attributed to EETimes – Under the Hood

JM Badge



Source attributed to– Freescale.com

MCF51JM Block Diagram

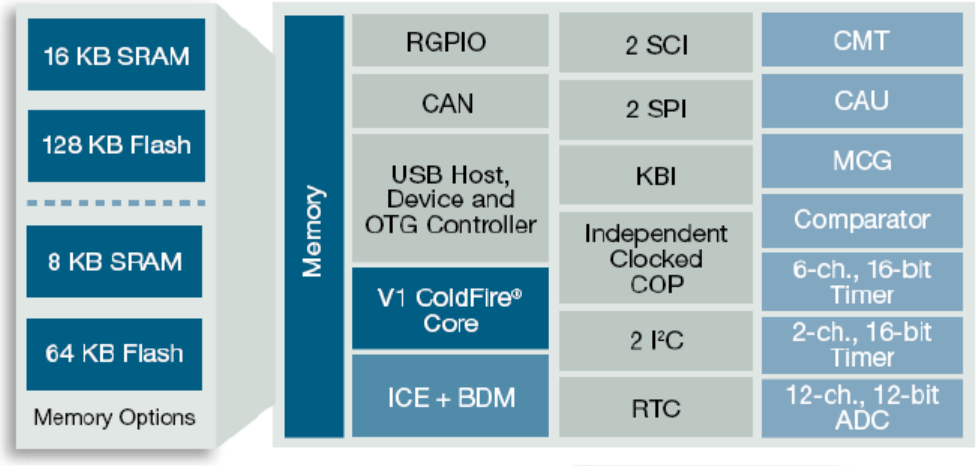


Figure 1. MCF51JM Block Diagram

Source attributed to– Freescale.com

CodeWarrior for Microcontrollers (RS08/HC(S)08/ColdFire V1)

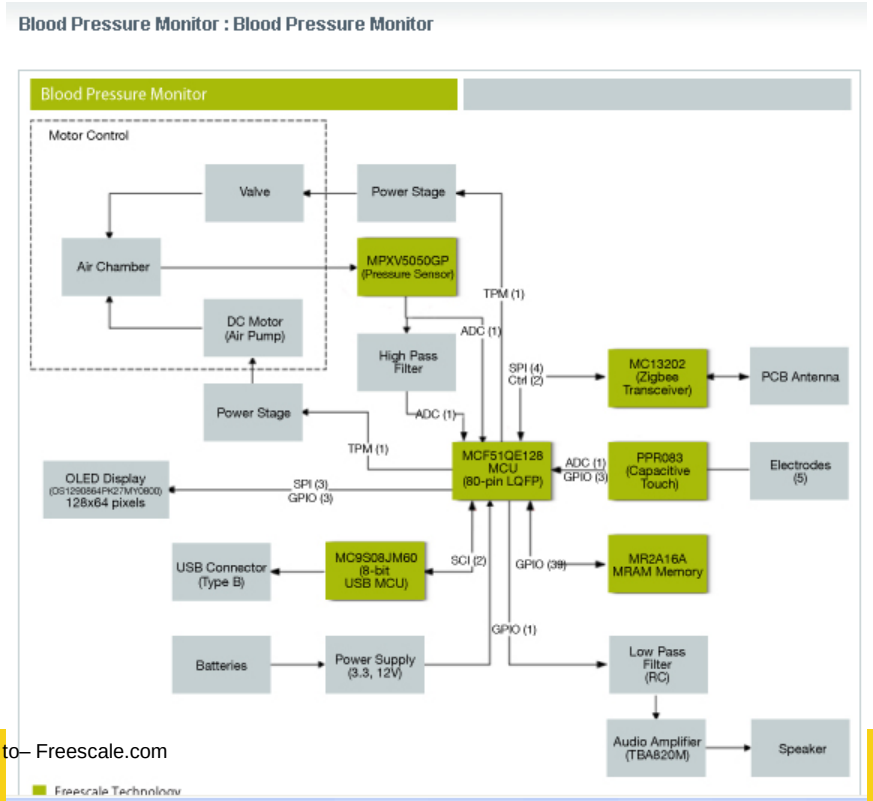
	SPECIAL buy | info $0 (free)	BASIC buy | info from $395	STANDARD buy | info from $995	PROFESSIONAL buy | info from $1995
Supported Platforms				
HC(S)08/RS08 Microcontrollers	✓	✓	✓	✓
ColdFire® Architectures (V1)	✓	✓	✓	✓
Build Tools				
Macro Assembler	✓	✓	✓	✓
Compiler (C/C++)	▨	▨	✓	✓
Libmaker	▨	▨	✓	✓
Debug Tools				
Source-Level Debugger	▨	▨	✓	✓
Flash Programmer	▨	▨	✓	✓
Data Visualization and I/O Stimulation	▨	▨	✓	✓
Simulator			✓	✓
Decoder			✓	✓
OSEK Awareness				✓
Advanced Tools				
Device Initialization	✓	✓	✓	✓
Processor Expert	✓	✓	✓	✓
- Basic Beans	✓	✓	✓	✓
- Software Beans			✓	✓
- Advanced Beans				✓
- Bean Wizard				✓
PC-Lint Plug-in				✓
Profile Analysis and Code Coverage				✓

▨ – code size and other limitations to feature

✓ – included in suite

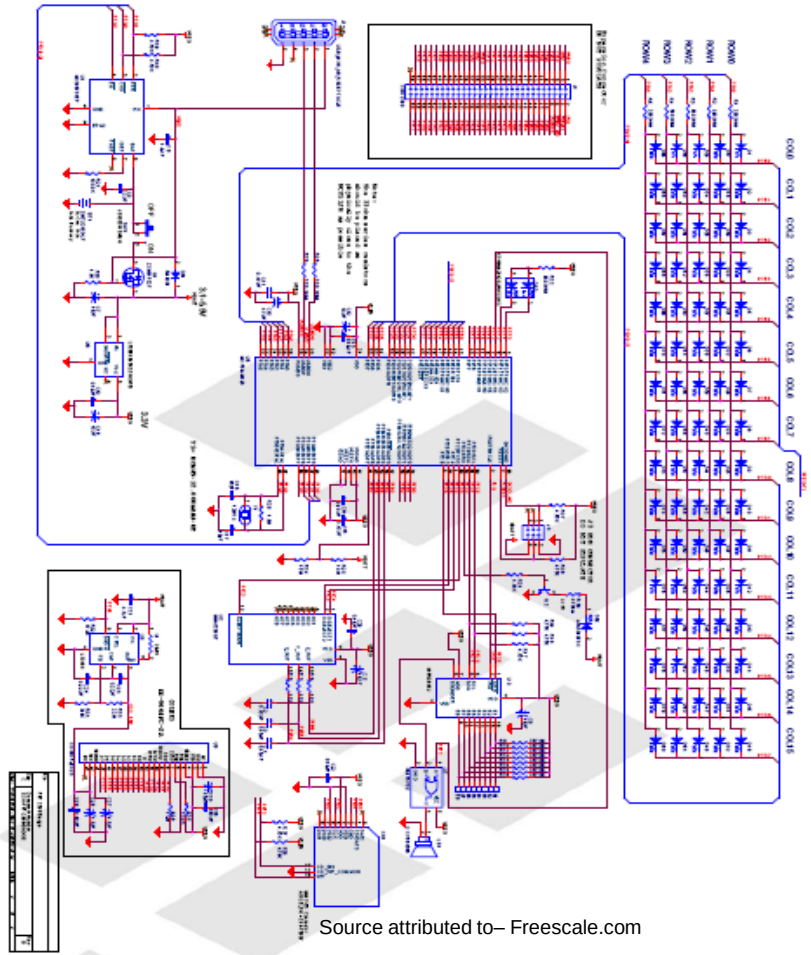
Source attributed to– Freescale.com

Reference Designs



Source attributed to– Freescale.com

5 Schematics



Source attributed to– Freescale.com

Basic Concepts (1)

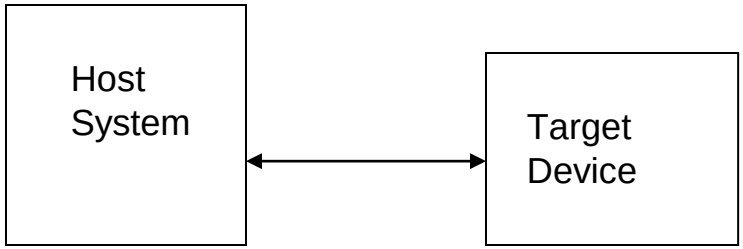
- Parallel vs Serial Communications
- Highway Example: 1 lane highway versus 8 lane highway
- Concepts applies to system and Inter-IC communications

Basic Concepts (2)

- Systems

Parallel Example: SCSI, IEEE1284

Serial Example: USB, Firewire 1394a/b

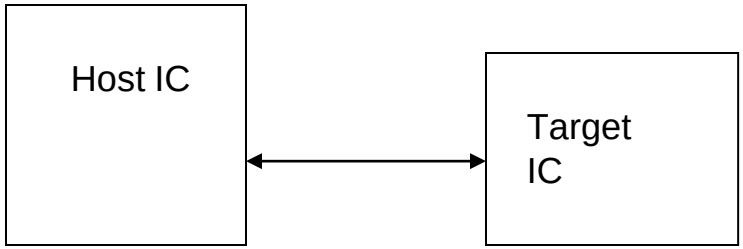


Basic Concepts (3)

- Inter-IC communications

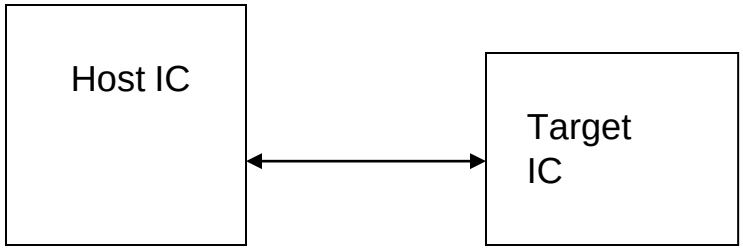
Parallel Example: PCI, FSB, MemBus

Serial Example: I2C, SPI, JTAG…



Basic Concepts (4)

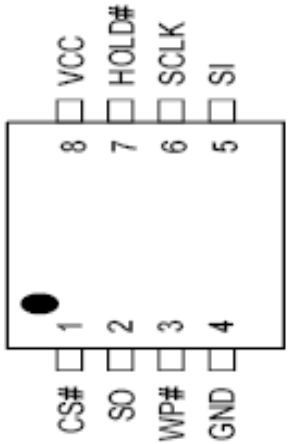
- SPI- Serial Peripheral Interface
- 4 wire
- SCLK, SI, SO, CS#



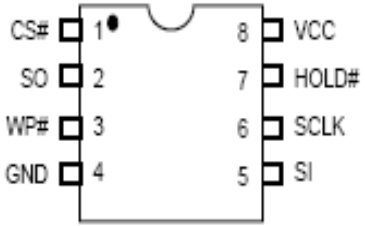
Basic Concepts (5)

PIN CONFIGURATIONS

8-PIN SOP (150/200mil)



8-PIN PDIP (300mil)



PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI	Serial Data Input
SO	Serial Data Output
SCLK	Clock Input
HOLD#	Hold, to pause the device without deselecting the device
WP#	Write Protection
VCC	+ 3.3V Power Supply
GND	Ground

Source attributed to– Macronix.com

Basic Concepts (6)

- SPI : Serial Peripheral Interface– command definition

Table 2. COMMAND DEFINITION

COMMAND (byte)	WREN (write Enable)	WRDI (write disable)	RDID (read ident-ification)	RDSR (read status register)	WRSR (write status register)	READ (read data)	Fast Read (fast read data)
1st	06 Hex	04 Hex	9F Hex	05 Hex	01 Hex	03 Hex	0B Hex
2nd						AD1	AD1
3rd						AD2	AD2
4th						AD3	AD3
5th							x
Action	sets the (WEL) write enable latch bit	reset the (WEL) write enable latch bit	output the manufacturer ID and 2-byte device ID	to read out the status register	to write new values to the status register	n bytes read out until CS# goes high	

Source attributed to– Macronix.com

Basic Concepts (7)

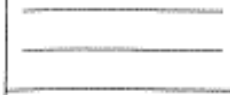
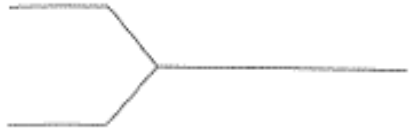
- SPI : Serial Peripheral Interface –more command definition

COMMAND (byte)	SE (Sector Erase)	BE (Block Erase)	CE (Chip Erase)	PP (Page Program)	DP (Deep Power Down)	RDP (Release from Deep Power-down)	RES (Read Electronic ID)	REMS (Read Electronic Manufacturer & Device ID)
1st	20 Hex	52 or D8 Hex	60 or C7 Hex	02 Hex	B9 Hex	AB Hex	AB Hex	90 Hex
2nd	AD1	AD1		AD1			x	x
3rd	AD2	AD2		AD2			x	x
4th	AD3	AD3		AD3			x	ADD(1)
5th								
Action								Output the manufacturer ID and device ID

Source attributed to– Macronix.com

Basic Concepts (8)

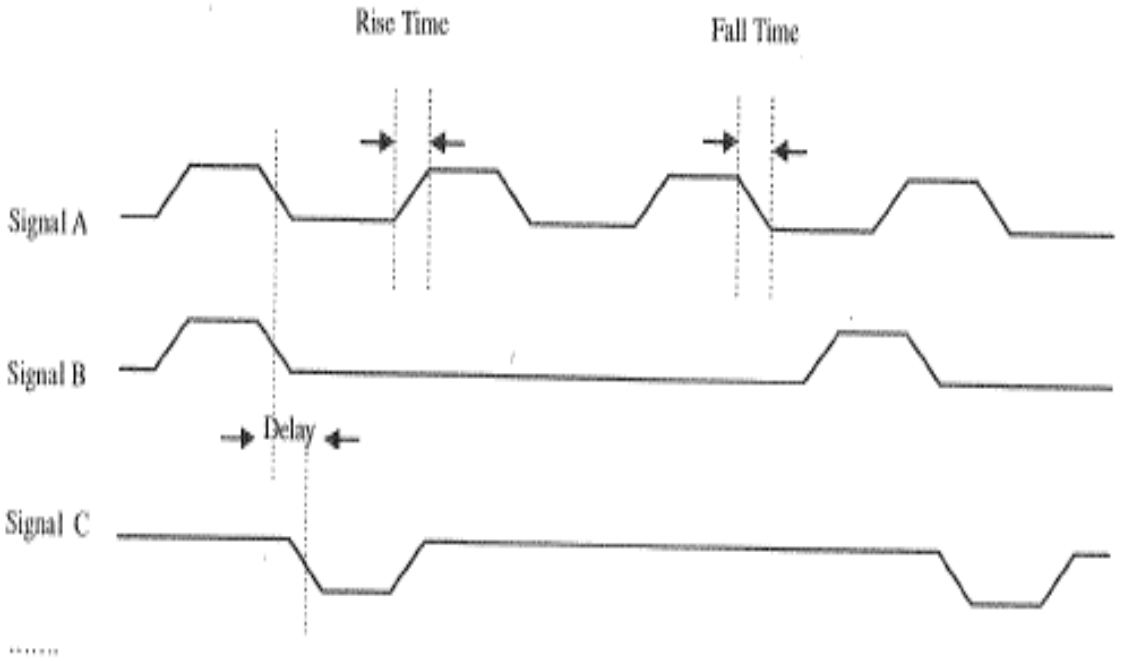
Timing Diagram Symbol Table

Symbol	Input Signals	Output Signals
	Input signal must be valid	Output signal will be valid
	Input signal doesn't affect system, will work regardless	Indeterminate output signal
	Garbage signal (nonsense)	Output signal not driven (floating), tristate, HiZ, high impedance
	If the input signal rises	Output signal will rise
	If the input signal falls	Output signal will fall

Source attributed to– "Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers:" by Tammy Noergaard

Basic Concepts (9)

Timing Diagram Example

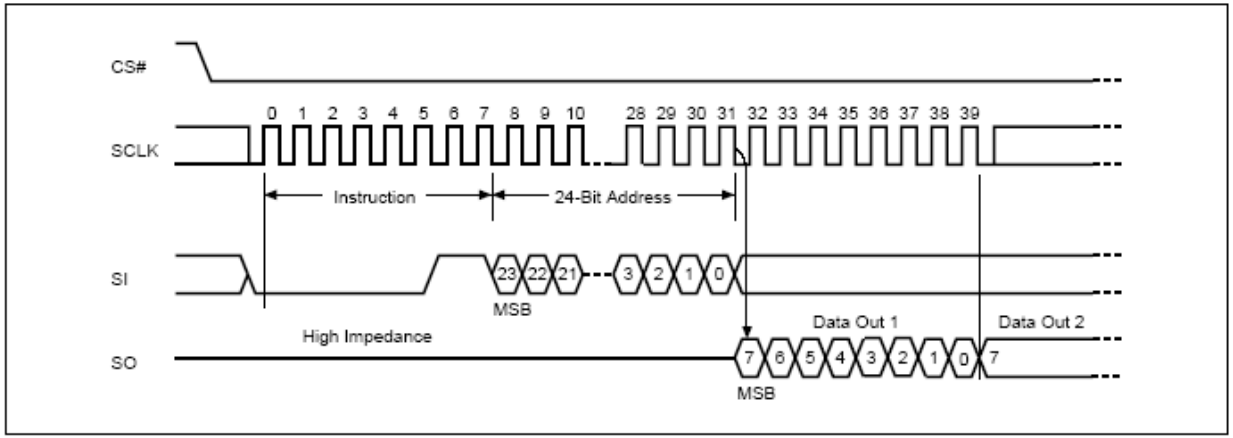


Source attributed to– "Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers:" by Tammy Noergaard

Basic Concepts (10)

- SPI : Serial Peripheral Interface- 03# command

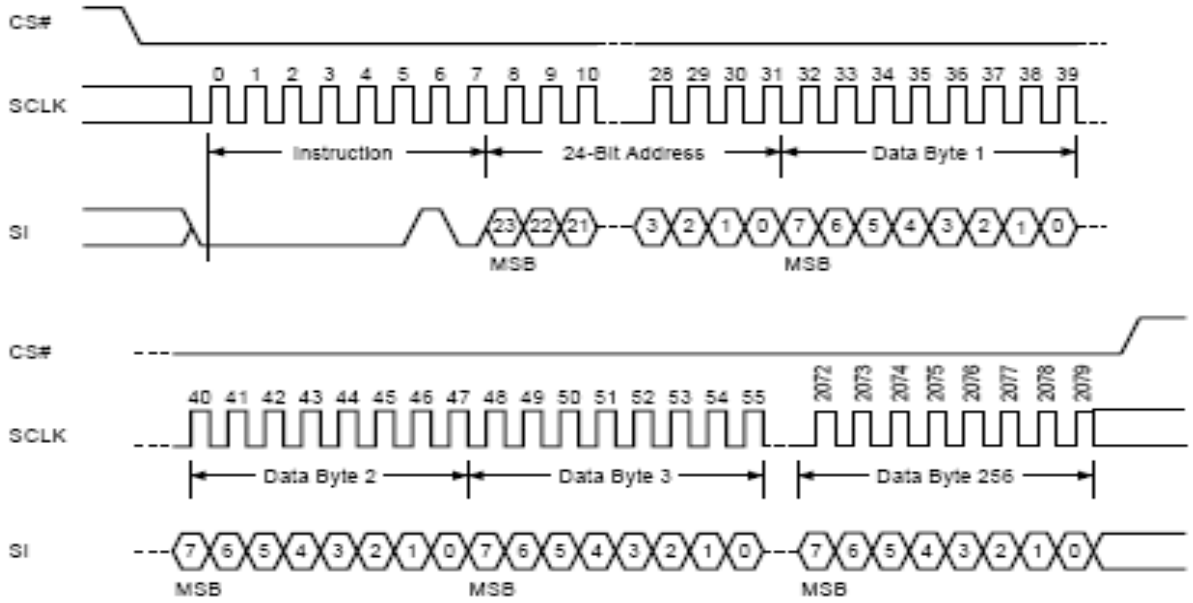
Figure 16. Read Data Bytes (READ) Instruction Sequence and Data-Out Sequence



Source attributed to– Macronix.com

Basic Concepts (11)

- SPI : Serial Peripheral Interface (02 Command- page program)

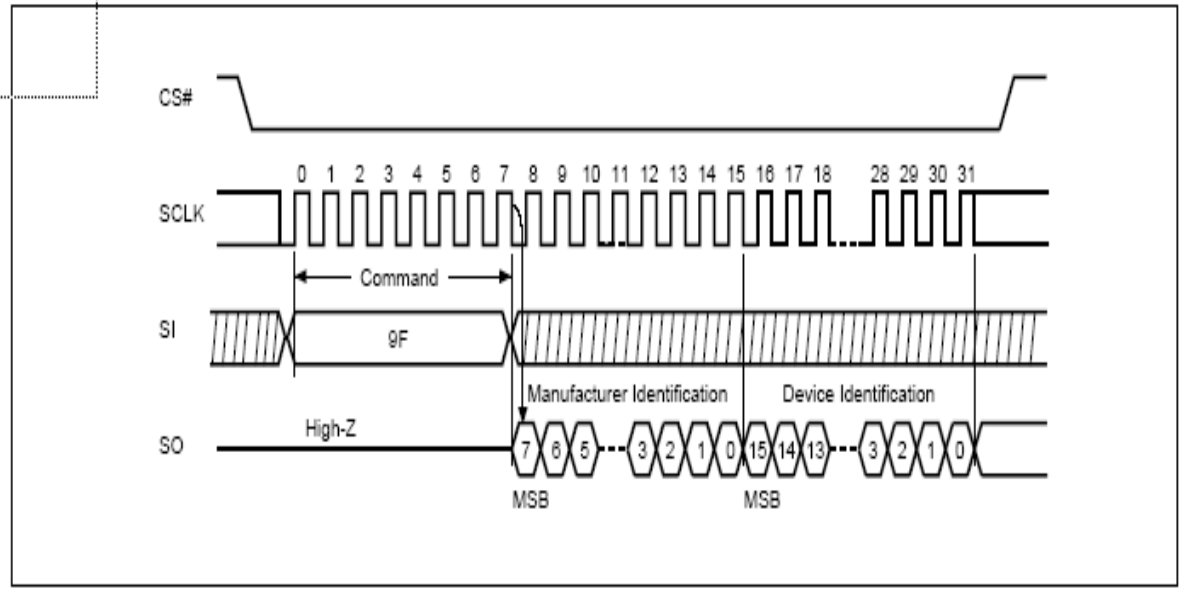


Source attributed to– Macronix.com

Basic Concepts (12)

- SPI Serial Peripheral Interface (9F Command

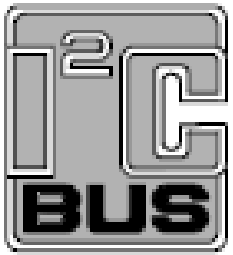
Figure 13. Read Identification (RDID) Sequence (Command 9F)



Source attributed to– Macronix.com

Basic Concepts (13)

- I2C
- Invented by Philips 20+ year ago
- Version 2.1 Jan 2000
- 2 wire: SCL Serial Clock, SDA Serial Data



Source attributed to *www.**i2c**-bus.org/*

Basic Concepts (14)

- I2C

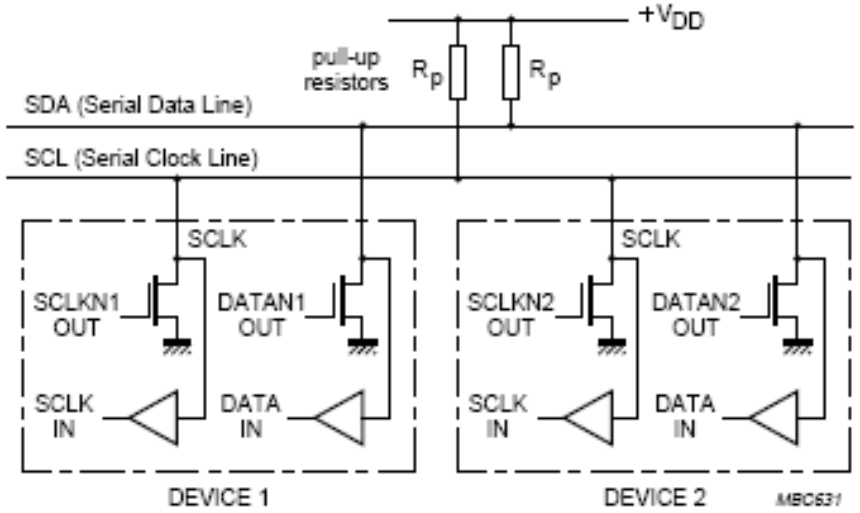


Fig.3 Connection of Standard- and Fast-mode devices to the I²C-bus.

Source attributed to *www.**i2c**-bus.org/*

Basic Concepts (15)

- I2C

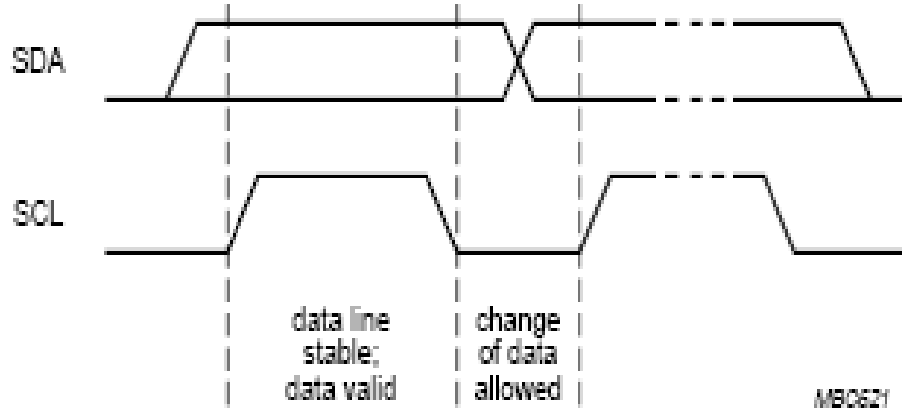


Fig.4 Bit transfer on the I²C-bus.

Source attributed to *www.**i2c**-bus.org/*

Basic Concepts (16)

- I2C

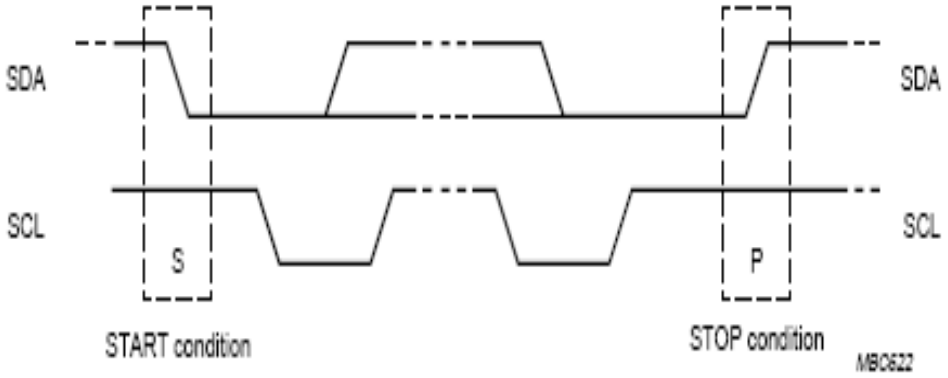
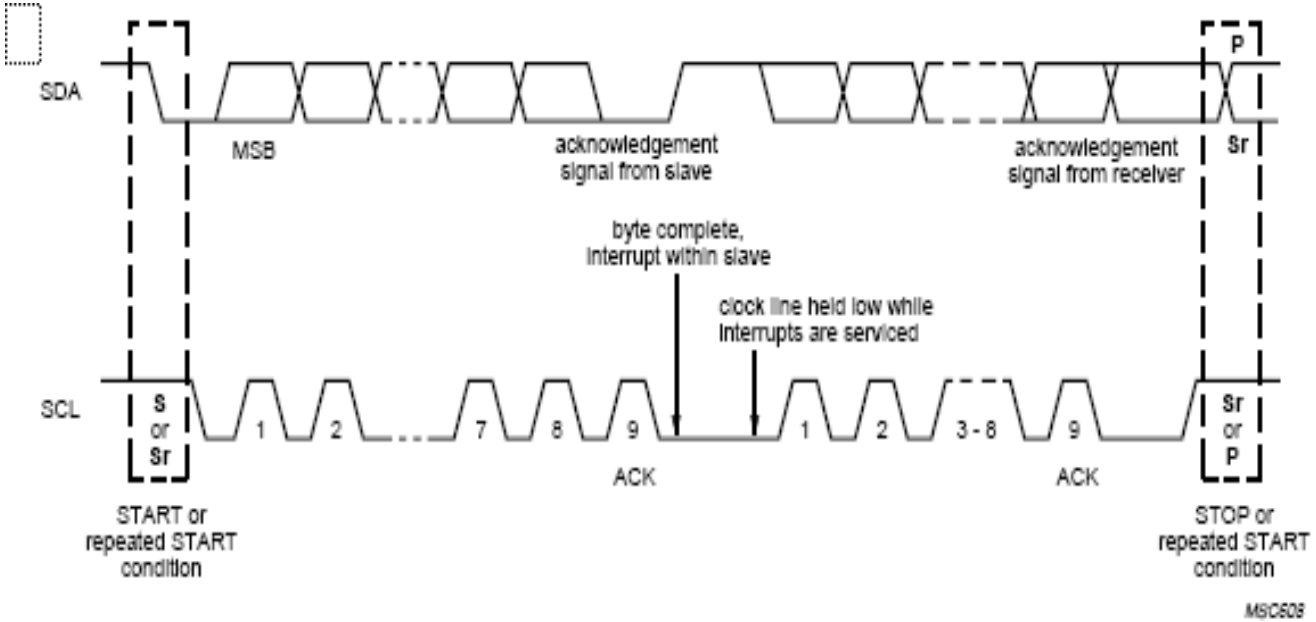


Fig.5 START and STOP conditions.

Basic Concepts (17)

- I2C



Source attributed to *www.**i2c**-bus.org/*

Basic Concepts (18)

- JTAG – Joint Test Action Group 1985
  - IEEE 1149.1

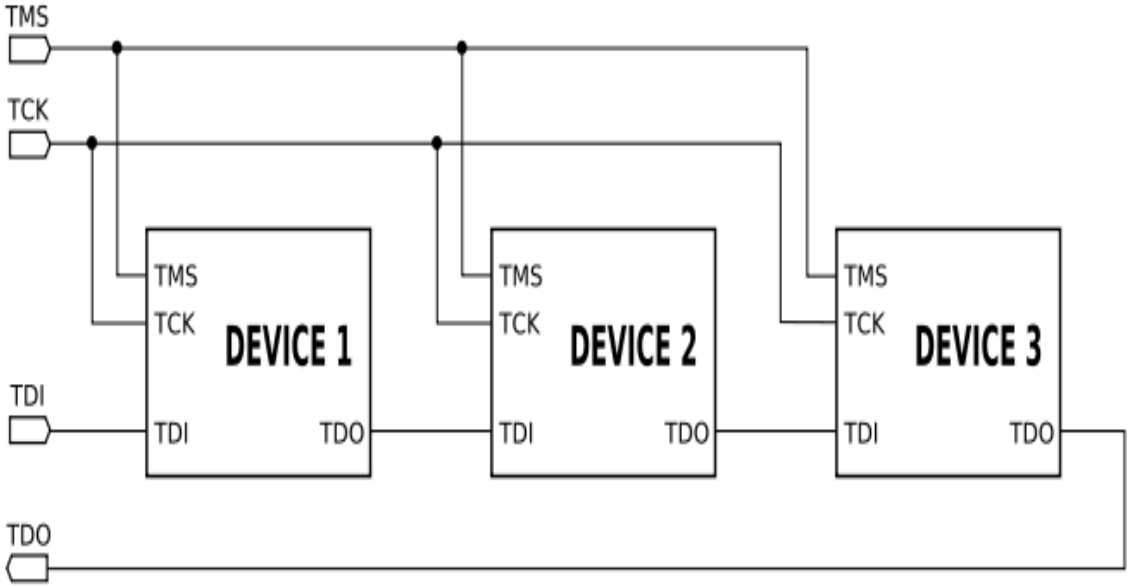
1. **TDI** (Test Data In)
2. **TDO** (Test Data Out)
3. **TCK** (Test Clock)
4. **TMS** (Test Mode Select)
5. **TRST** (Test Reset) optional.

Source attributed to *www.**jtag.com**/*

Basic Concepts (19)

- JTAG daisy chained devices

Test reset signal is not shown in the image.



Source attributed to *www.**jtag.com**/*

Basic Concepts (20)

- JTAG – Most FPGAs have JTAG ports – SPI Programming for PROM

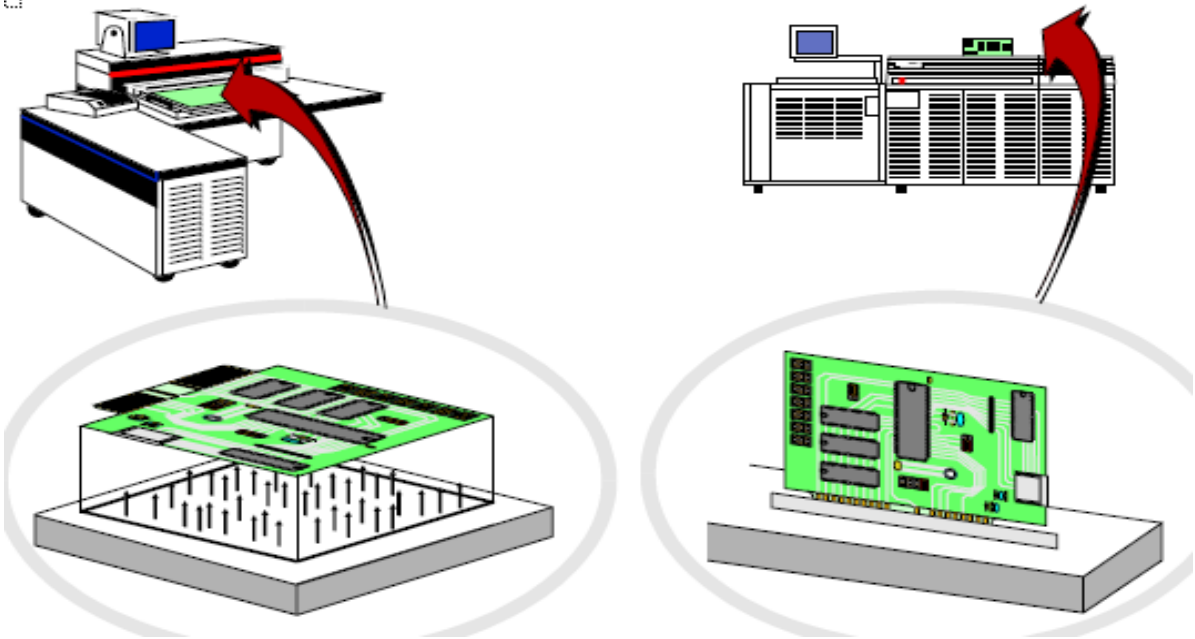
Table 5: **Download Header Signal Description for SPI Programming Mode**

Ribbon Cable Number	SPI Programming Mode	JTAG/Slave Serial Configuration Mode Signal Cross Reference	Type	SPI Header Usage Description
2	V_{REF}	V_{REF}	In	**Target Reference Voltage.** This pin should be connected to a voltage bus on the target system that serves the JTAG, Slave-serial, or SPI interface. The target reference voltage must be regulated and must not have a current-limiting resistor in series with the V_{REF} pin.
4	$\overline{SS}$	TMS/PROG	Out	**Chip Select (S).** This pin is used to enable the device to accept an instruction.
6	SCK	TCK/CCLK	Out	**SPI Clock (C).** SPI flash memory clock provides the timing for the serial interface and is produced by the Xilinx cable.
8	MISO	TDO/DONE	In	**Serial Data Output (Q).** This signal is used to transfer data serially out of the device.
10	MOSI	TDI/DIN	Out	**Serial Data Input (D).** This input signal is used to transfer data serially into the device. The device receives instructions, addresses, and the data to be programmed from this signal.
12	N/C	N/C	–	**Reserved.** This pin is reserved for Xilinx diagnostics and should not be connected to any target circuitry.
14	–	– /INIT	BIDIR	–
1, 3, 5, 7, 9, 11, 13	–	GND	GND	**Digital Ground.**

Source attributed to *www.**xilinx.com**/*

Basic Concepts (21)

- JTAG applications – Boundary Scan replaces “bed of nails”



Source attributed to *www.**jtag.com**/*

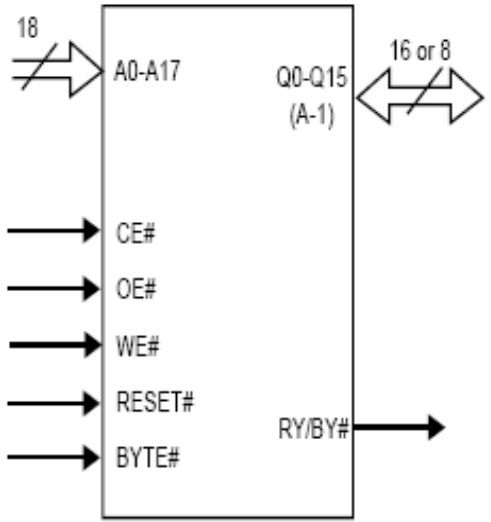
Basic Concepts (22)

- Parallel Flash Interface - JEDEC

PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A17	Address Input
Q0~Q14	Data Input/Output
Q15/A-1	Q15(Word mode)/LSB addr(Byte mode)
CE#	Chip Enable Input
WE#	Write Enable Input
BYTE#	Word/Byte Selection input
RESET#	Hardware Reset Pin/Sector Protect Unlock
OE#	Output Enable Input
RY/BY#	Ready/Busy Output
VCC	Power Supply Pin (+5V)
GND	Ground Pin

LOGIC SYMBOL

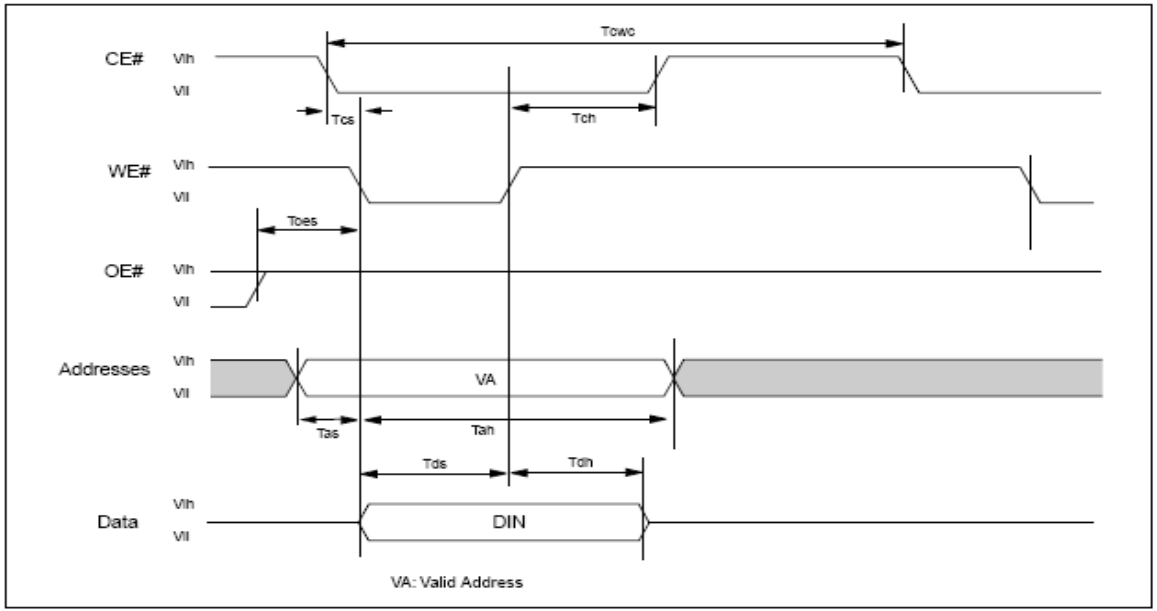


Source attributed to– Macronix.com

Basic Concepts (23)

- Parallel Flash Interface – JEDEC

Figure 1. COMMAND WRITE OPERATION

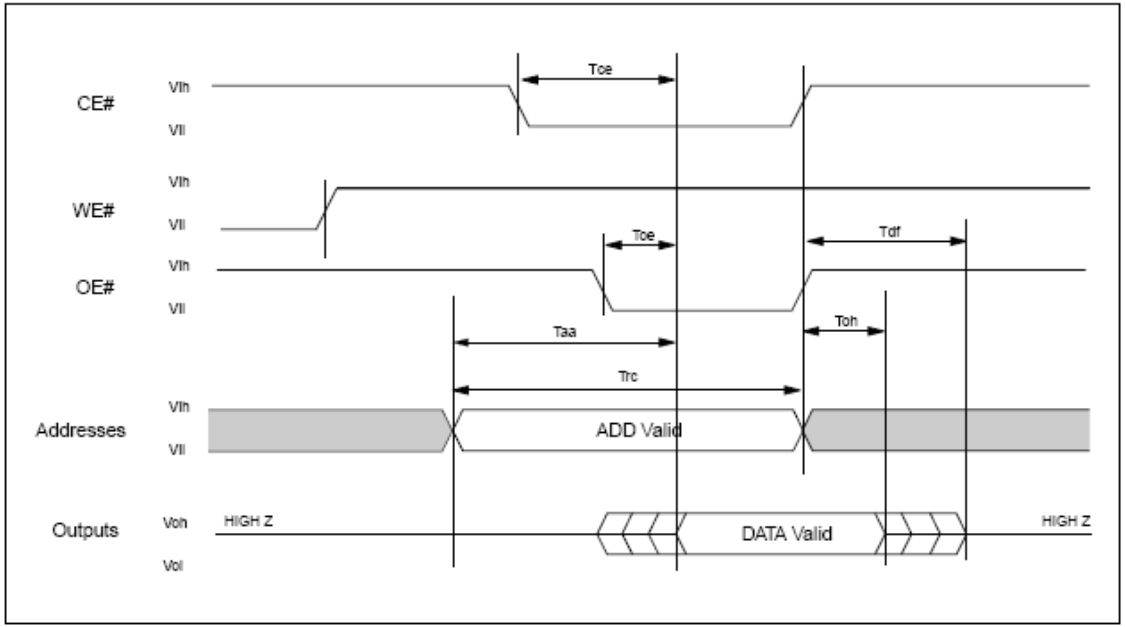


Source attributed to– Macronix.com

Basic Concepts (24)

- Parallel Flash Interface - JEDEC

Figure 2. READ TIMING WAVEFORMS

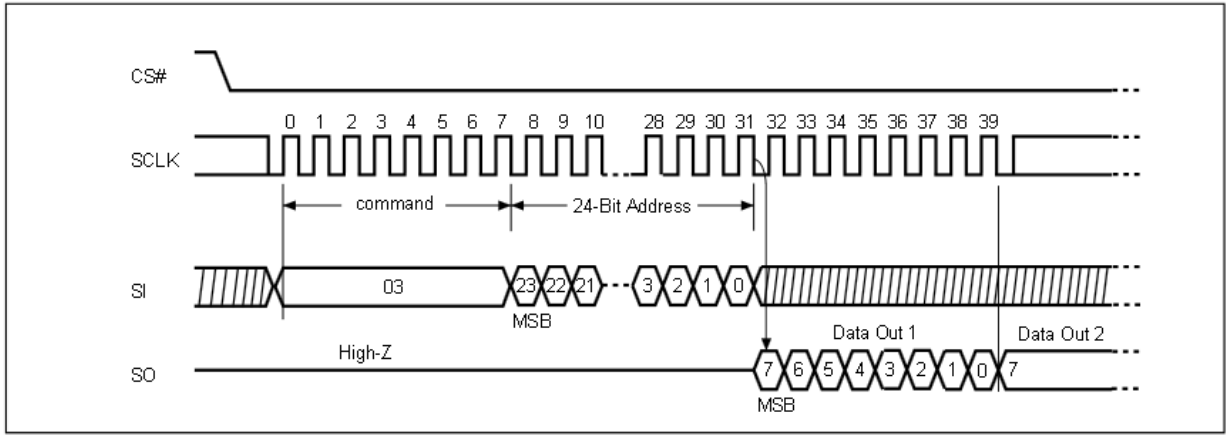


Source attributed to– Macronix.com

Basic Concepts (25)

- Serial Peripheral Interface – Single IO Normal Read

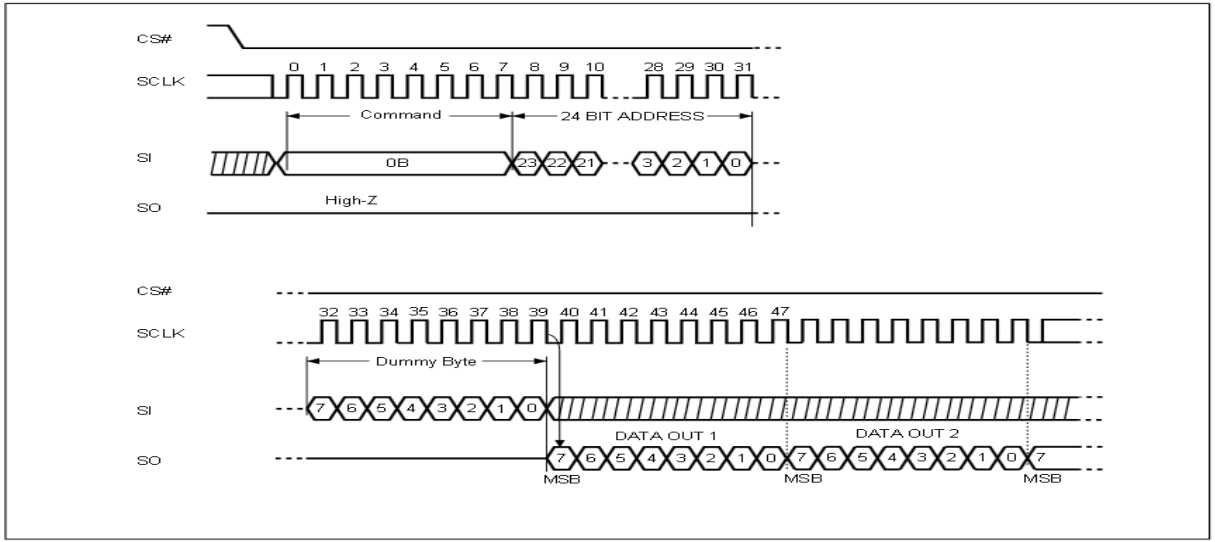
Figure 15. Read Data Bytes (READ) Sequence (Command 03)



Basic Concepts (26)

- Serial Peripheral Interface – Fast Read/ Dummy Cycles

Figure 16. Read at Higher Speed (FAST_READ) Sequence (Command 0B)

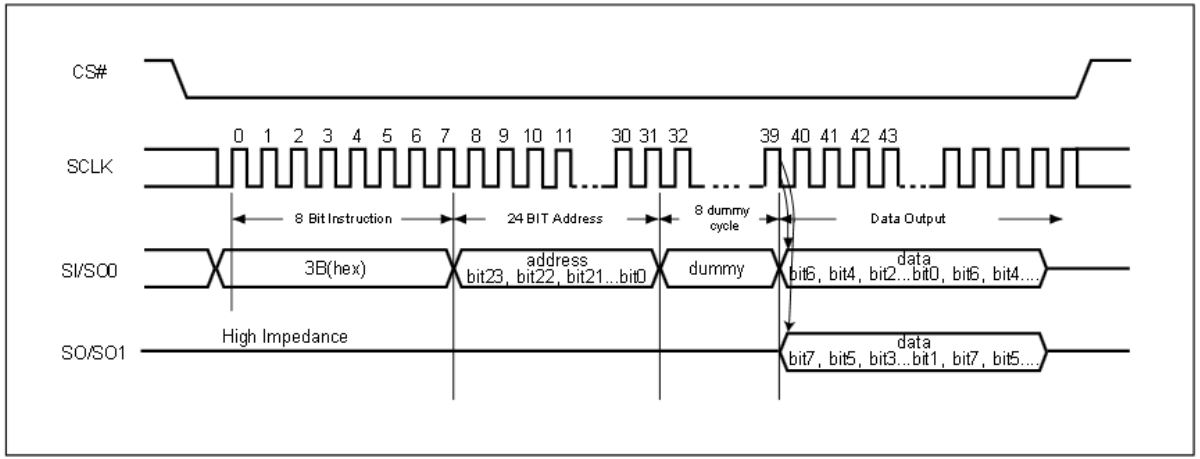


Source attributed to– Macronix.com

Basic Concepts (26)

- Serial Peripheral Interface – Dual Output Read

Figure 17. Dual Output Read Mode Sequence (Command 3B)

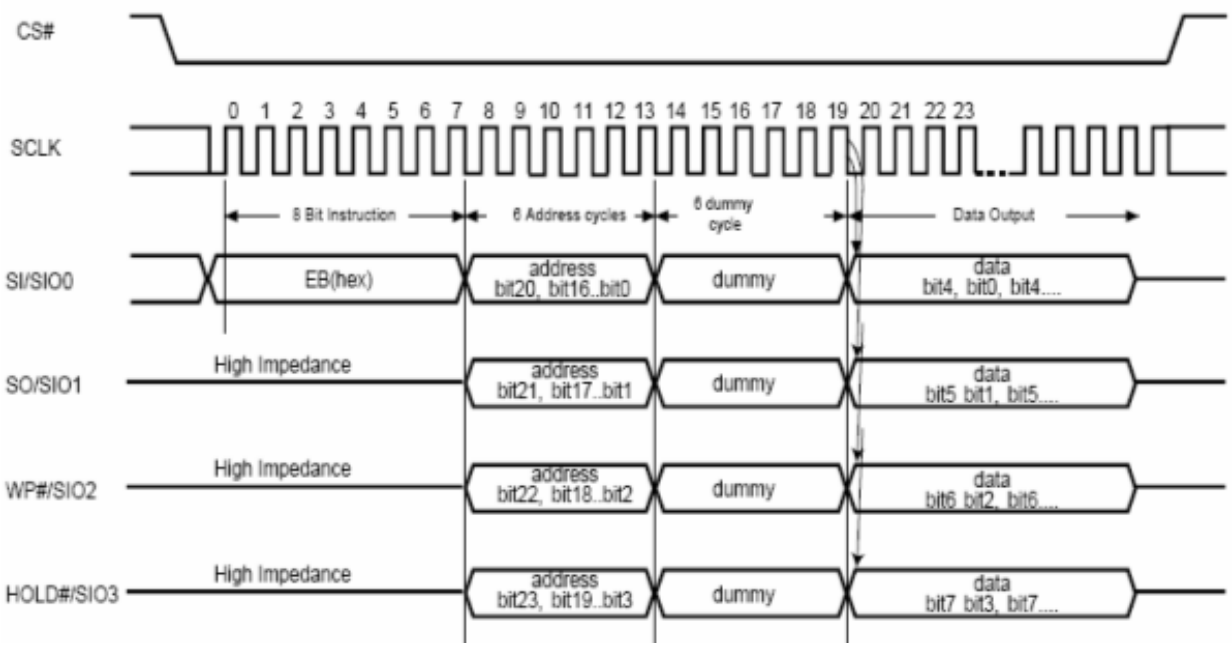


Source attributed to– Macronix.com

Basic Concepts (27)

- Serial Interface – Quad IO

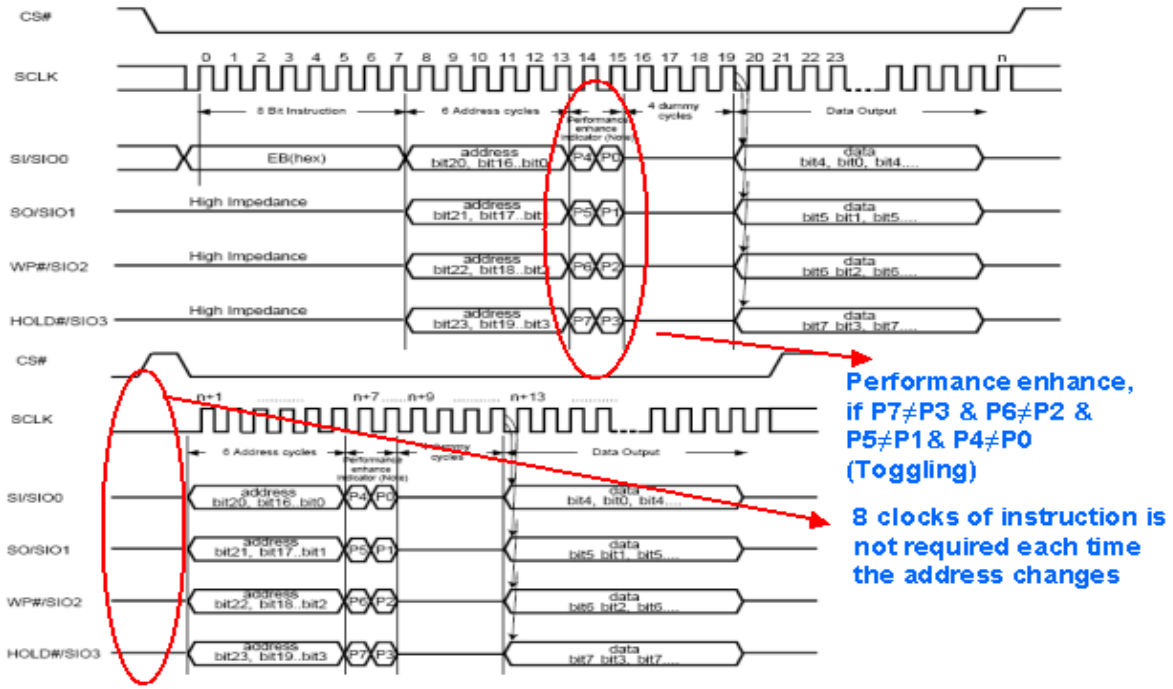
Waveform for Quad I/O read :



Source attributed to– Macronix.com

Basic Concepts (28)

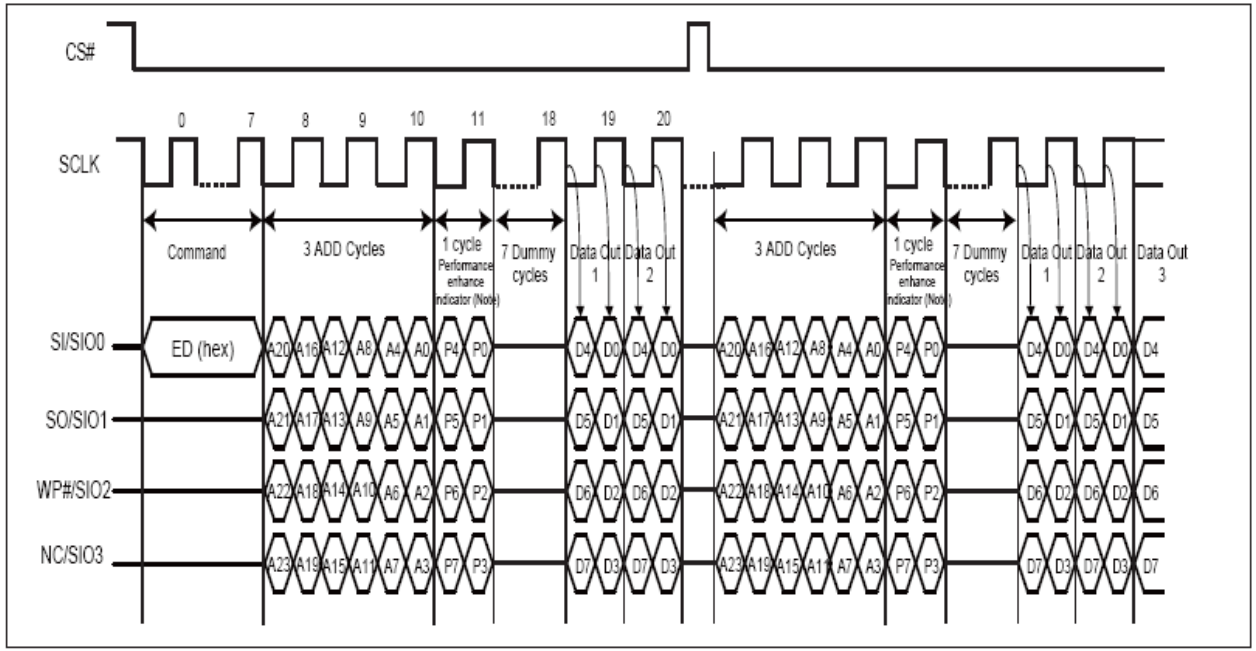
- Serial Interface – Quad IO w/ Performance



Source attributed to– Macronix.com

Basic Concepts (29)

- Serial Interface – Quad IO with DTR



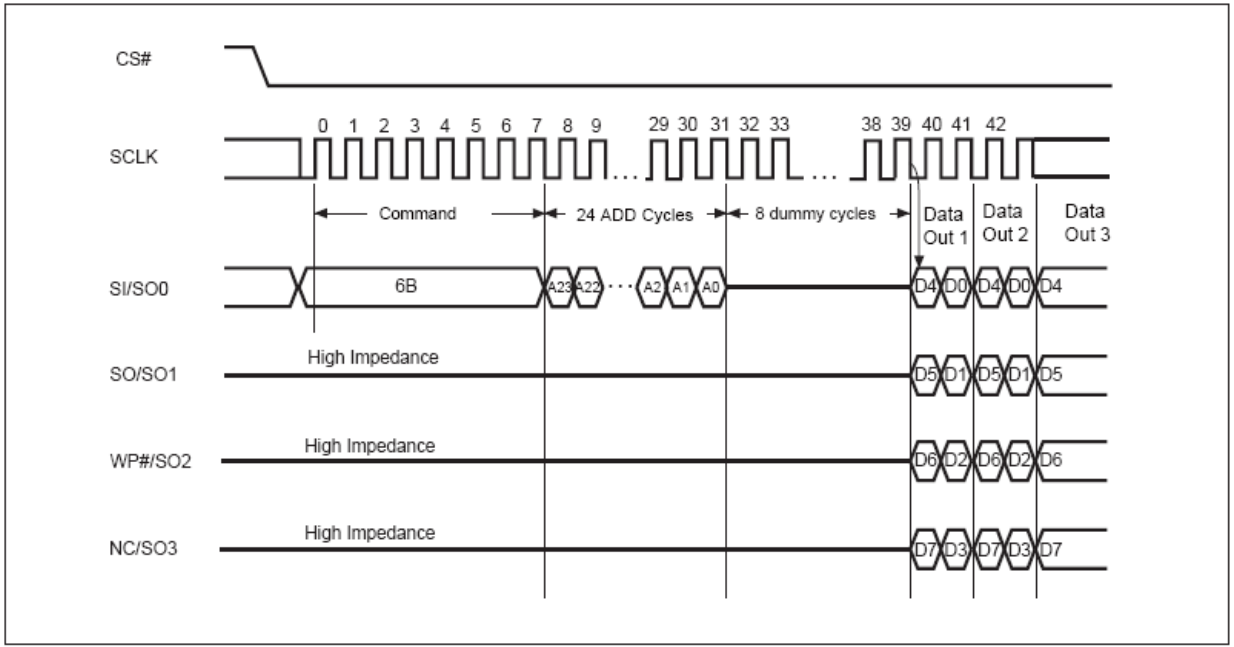
Note: Performance enhance, if P7≠P3 & P6≠P2 & P5≠P1 & P4≠P4 (Toggle)

Source attributed to– Macronix.com

Basic Concepts (30)

- Serial Interface – Quad IO (single –in multi out)

Figure 16. Quad Read Mode Sequence (Command 6B)



Source attributed to– Macronix.com

Basic Concepts (31)

- Serial Peripheral Interface – Octa SPI OPI Command Set

Table 6. OPI Command Set

Read/Write Array Commands

Command (byte)	8READ (Octa IO Read)	8DTRD (Octa IO DT Read)	RDID (read identification)	RDSFDP
1st byte	EC (hex)	EE (hex)	9F (hex)	5A (hex)
2nd byte	13 (hex)	11 (hex)	60 (hex)	A5 (hex)
3rd byte	ADD1	ADD1	00h	ADD1
4th byte	ADD2	ADD2	00h	ADD2
5th byte	ADD3	ADD3	00h	ADD3
6th byte	ADD4	ADD4 (Note 6)	00h	ADD4
7th byte	Dummy (Note 7)	Dummy (Note 7)		Dummy(20)
Data Cycles			3 (Note 8)	
Action	Octa I/O STR read	Octa I/O DTR read	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	Read SFDP mode

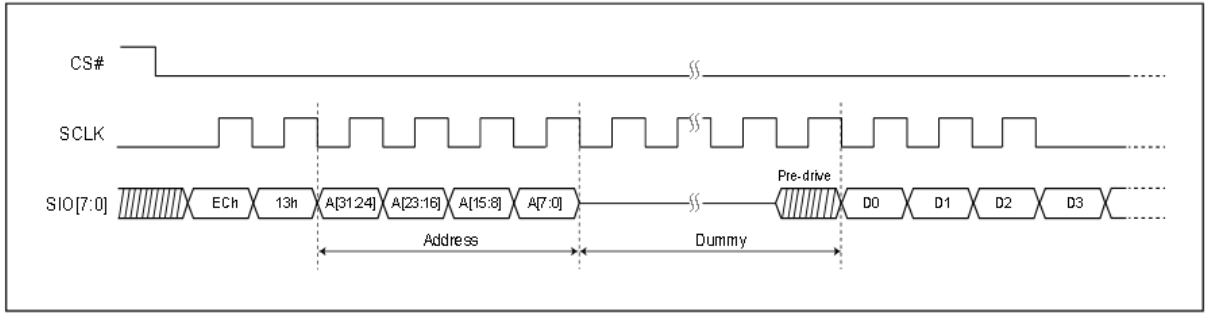
Command (byte)	PP (page program)	SE (sector erase)	BE (block erase 64KB)	CE (chip erase)
1st byte	12 (hex)	21 (hex)	DC (hex)	60 or C7 (hex)
2nd byte	ED (hex)	DE (hex)	23 (hex)	9F or 38 (hex)
3rd byte	ADD1	ADD1	ADD1	
4th byte	ADD2	ADD2	ADD2	
5th byte	ADD3	ADD3	ADD3	
6th byte	ADD4 (Note 6)	ADD4	ADD4	
7th byte				
Data Cycles	1-256			
Action	to program the selected page	to erase the selected sector	to erase the selected block	to erase whole chip

Source attributed to– Macronix.com

Basic Concepts (32)

- Serial Peripheral Interface – Octa STR Output Read

Figure 42. OCTA Read Mode Sequence (STR-OPI Mode)

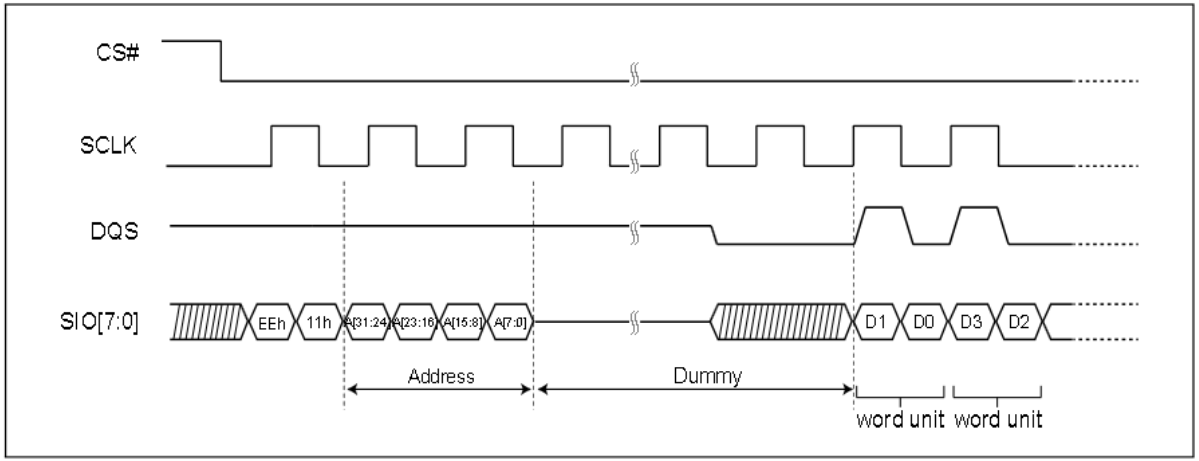


Source attributed to– Macronix.com

Basic Concepts (33)

- Serial Peripheral Interface – Octa DTR Output Read

Figure 43. OCTA Read Mode Sequence (DTR-OPI Mode)



Source attributed to– Macronix.com

Basic Concepts (34)

- Other Commonly Used Interface/ Bus
  - SDIO - A SDIO (Secure Digital Input Output) card is an extension of the SD specification to cover I/O functions. SDIO cards are only fully functional in host devices designed to support their input-output functions (typically PDAs like the Palm Treo, but occasionally laptops or mobile phones). These devices can use the SD slot to support GPS receivers, modems, barcode readers, FM radio tuners, TV tuners, RFID readers, digital cameras, and interfaces to Wi-Fi, Bluetooth, Ethernet, and IrDA.

SD Mode (1 and 4-bit)			SPI Mode		
Name	Type	Description	Name	Type	Description
CMD	Bidir.	Command/Response	DI	Input	Data In
CLK	Input	Clock	SCLK	Input	Clock
DAT[0]	Bidir.	Data Line 0	DO	Output	Data Out
DAT[1]	Bidir.	Data Line 1	RSV	-	-
DAT[2]	Bidir.	Data Line 2	RSV	-	-
DAT[3]	Bidir.	Data Line 3	CS	Input	Chip-select

There are 3 fundamental modes that the SD Physical layer can operate in:

1. 4-bit SD DAT Mode
2. 1-bit SD DAT Mode
3. SPI-Mode

Source attributed to– Wikipedia.com

Basic Concepts (34)

- Other Commonly Used Interface
  - CAN Bus-Controller Area Network is a multi-master serial bus standard for connecting Electronic Control Units [ECUs] also known as nodes.
  - Two or more nodes are required on the CAN network to communicate.
  - Commonly used in Automotive.
  - Maximum BW is about 1Mbps
  - Based on ISO-11898:2003*- The ISO-11898:2003 standard specifies differential data transmission and half duplex communication over any cable type (although the use of twisted pair has become best practice) at up to 1Mbps.

* About ISO-(International Organization for Standardization) is an independent, non-governmental membership organization and the world's largest developer of voluntary International Standards-specifications for products, services and systems, to ensure quality, safety and efficiency. They are instrumental in facilitating international trade.

Source attributed to– Wikipedia.com and www.can-cia.org.

Basic Concepts (34)

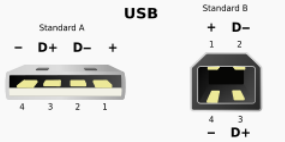
- Other Commonly Used Interface-- USB

Universal Serial Bus (USB)

Certified USB logo

Type	Bus
Production history	
Designer	Compaq, DEC, IBM, Intel, Microsoft, NEC and Nortel
Designed	1996
Manufacturer	Compaq, DEC, IBM, Intel, Microsoft, NEC and Nortel
Produced	1997–present
Superseded	Serial port, parallel port, game port, Apple Desktop Bus, and PS/2 connector
General specifications	
Length	2–5 m (6 ft 7 in–16 ft 5 in) (by category)
Width	12 mm (A-plug),[1] 8.45 mm (B-plug); 7 mm (mini/micro-USB)
Height	4.5 mm (A-plug),[1] 7.78 mm (B-plug, pre-v3.0); 1.5–3 mm (mini/micro-USB)
Hot pluggable	Yes
External	Yes
Cable	Four wires plus shield (pre-3.0); nine wires plus shield (USB 3.0)
Pins	Four: one power supply, two data, one ground (pre-3.0); nine (USB 3.0); 11 (powered USB 3.0); five (pre-3.0 micro-USB)
Connector	Unique

Electrical	
Signal	5 V DC
Max. voltage	5.00±0.25 V (pre-3.0) $5.00^{+0.25}_{-0.55}$ V (USB 3.0)
Max. current	0.5–0.9 A (general) 5 A (charging devices)
Data	
Data signal	Packet data, defined by specifications
Width	One bit
Bitrate	1.5/12/480/5,000/10,000 Mbit/s (depending on mode)
Max. devices	127
Protocol	Serial
Pin out	



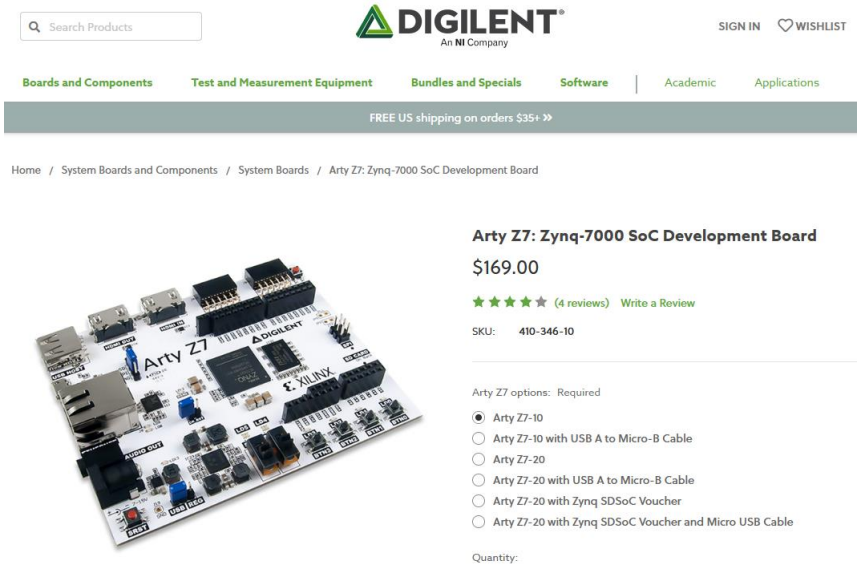
The standard-A USB plug (left) and standard-B plug (right)

Pin 1	V_{CC} (+5 V, red wire)
Pin 2	Data− (white wire)
Pin 3	Data+ (green wire)
Pin 4	Ground (black wire)

Version	Max. Signaling Rate	Date Introduced
USB 1.1	12Mbps	Jan-96
USB 2.0	480 Mbps	Apr-00
USB 3.0	5Gbps	Nov-08
USB 3.1	10Gbps	Jan-13

Source attributed to– Wikipedia.com

Introducing the ArtyZ7 Board



Source attributed to https://digilent.com/shop/arty-z7-zynq-7000-soc-development-board/