CSE121: Embedded System Design

PCB/DMA

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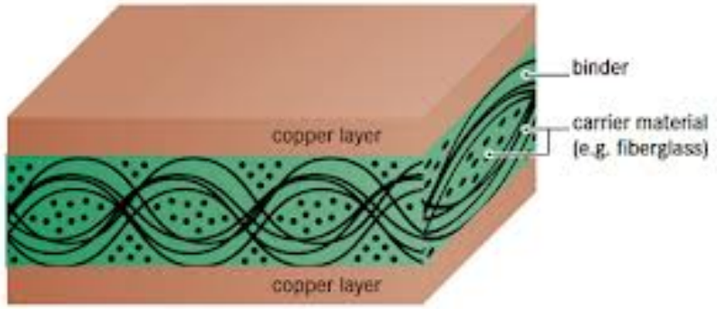
Announcements

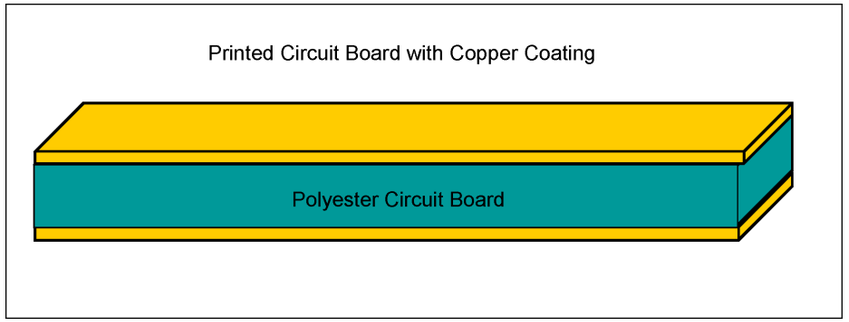
- Lab5 next week
- Lab6 posted

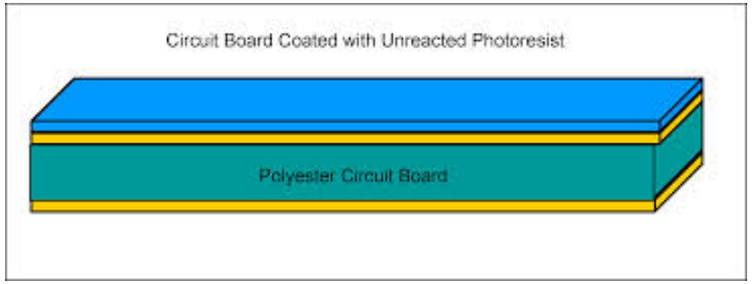
How to design my own PCB?

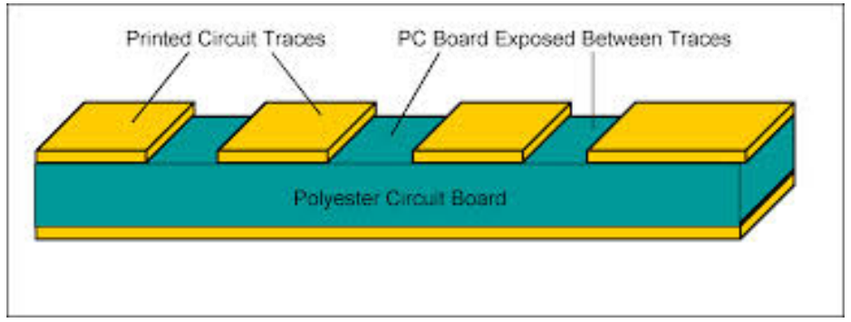
- General design. What parts are needed?
- Draw schematic, and layout for all components, refer to data sheets (schematic & layout)
- Generate component database
- Draw schematic, Design Rule Check (DRC)
- raw Layout, check
- Generate Gerber files, send to fab
- Procure all components
- Assembly (manual soldering or manufacture)

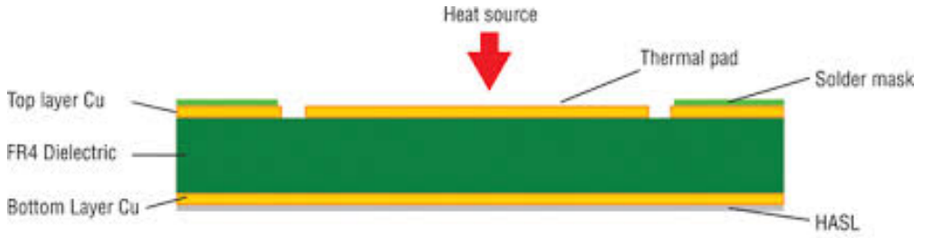
PC Board Construction











Source: EE 445L – Bard, McDermott, Valvano

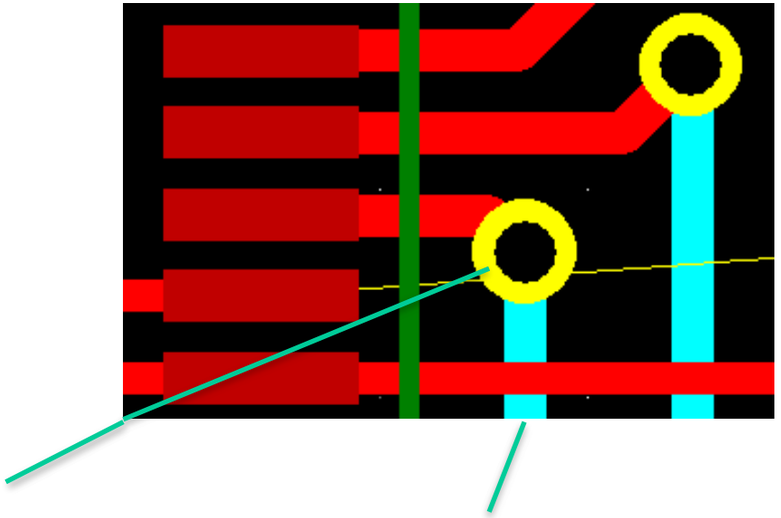
Minimum Trace Width For Various Currents

Length	Temperature Rise	Current	Thickness	Resistance	Trace Width
5"	1 C	100 mA	1 oz/ft^2	1 Ω	2 mil
5"	1 C	200 mA	1 oz/ft^2	0.47 Ω	5 mil
5"	1 C	500 mA	1 oz/ft^2	0.13 Ω	20 mil
5"	1 C	1 A	1 oz/ft^2	0.05 Ω	50 mil
5"	1 C	2 A	1 oz/ft^2	0.02 Ω	120 mil

Rule of thumb:
8 mil for digital
20 mil for power

Specifications

- Minimum trace width = 6 mil
- Minimum trace clearance = 6 mil
- Minimum drill size = 15 mil
- Maximum board size = 60 in2
- No multi-board layouts
- Smallest via is 25 mil pad, 15 mil hole
  - min annular ring 5 mil

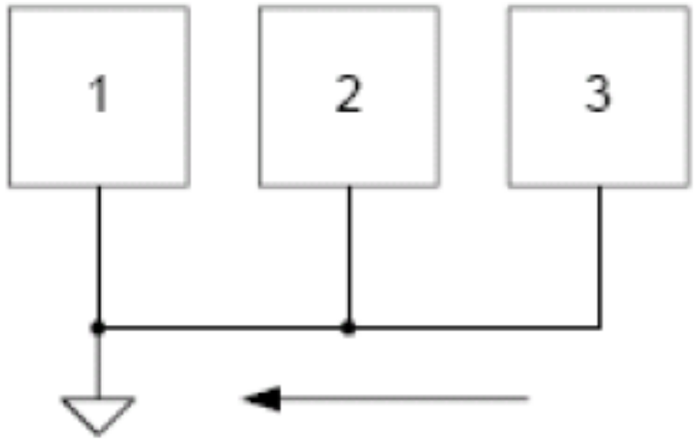


8 mil trace

Red is top copper
Yellow is through hole
Cyan is bottom copper
Orange is top mask
Grey is bottom mask

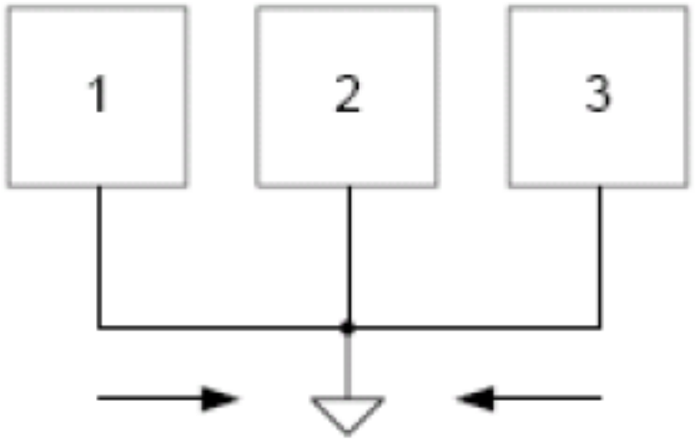
Routing

Series



- Simple wiring
- Common impedance causes different potentials
- High impedance at high frequency (>10 kHz)

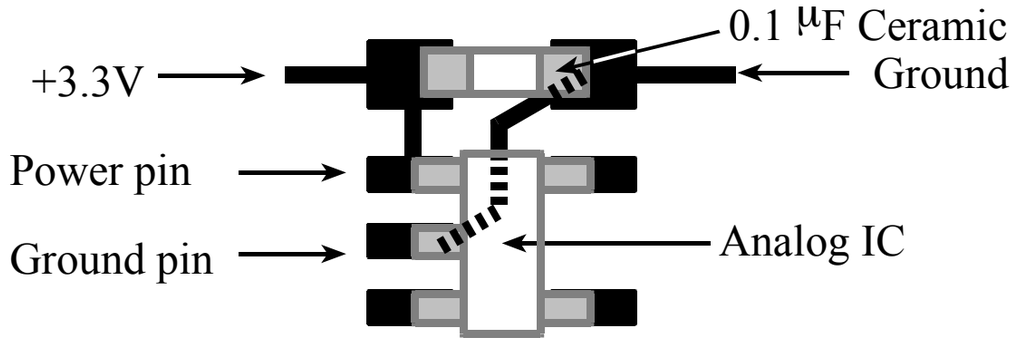
Parallel



- Complicated wiring
- Low differential potentials at low frequencies
- High impedance at high frequency (>10 kHz)

PC Board Layout Considerations

- ALL NETS HAVE NAMES
- Position the bypass capacitors as close to the chip as possible (yes)
- Place a ground plane under sensitive analog circuits
- Separate digital ground from analog ground



PC Board Layout Considerations

- Place all fixed location parts first
  - Carefully consider interface placement within the mechanical boundaries of the box
  - Think about how connectors will plug in
- Place parts near where they are connected
- Place bypass caps as close as possible
- Execute Tools->DesignRuleCheck - frequently
- Make sure the Snap to Grid mode is active (experiment with different settings of the snap)
- Add Top Silk labels for your initials, your TA's initials, the date, and the purpose of the board,
- Place all though-hole components on the top side (surface mount components can go on either side)
- If possible, align all chips in the same direction

PC Board Layout Considerations

- Configure board so that all though-hole soldering occurs on the bottom side,
- Add Top/Bottom Silk labeling to assist construction and debugging,
- Add test points at strategic points to assist in debugging,
  - Either by placing two holes 0.1 in apart then soldering a U wire into it,
  - or by making a 0.090 in pad with 0.043 in hole then solder a test point into the one hole
- All components need labels (e.g., U1 R1 C1 J1 etc.), shown both on the board and the circuit diagram
- Avoid 90-degree turns, convert them to two 45 degree turns,
- An assist to make it all fit is to go left-right on one side and up-down on the other side

PC Board Layout Considerations

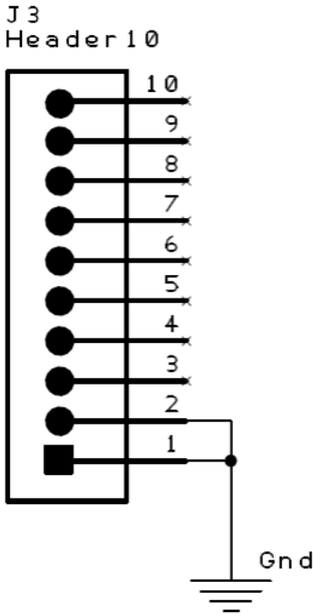
- The reality is that the signal-integrity benefits of avoiding 90° angles are insignificant at the frequencies/edge-rates seen in microcontroller circuits (even up to and past 1 GHz/100ps). [Johnson, H and Graham, M, High-Speed Digital Design: a Handbook of Black Magic, Prentice Hall: New Jersey, 1993.]
- There is a higher possibility of an acid-trap forming during etching on the inside of the angle (especially in acute angles). An acid trap causes over-etching which can be a yield issue in PC boards with small trace widths.
- Routing at 45° typically reduces overall trace length, frees board area
- It looks better. This is an important factor for anyone who appreciates the art of PCB layout.

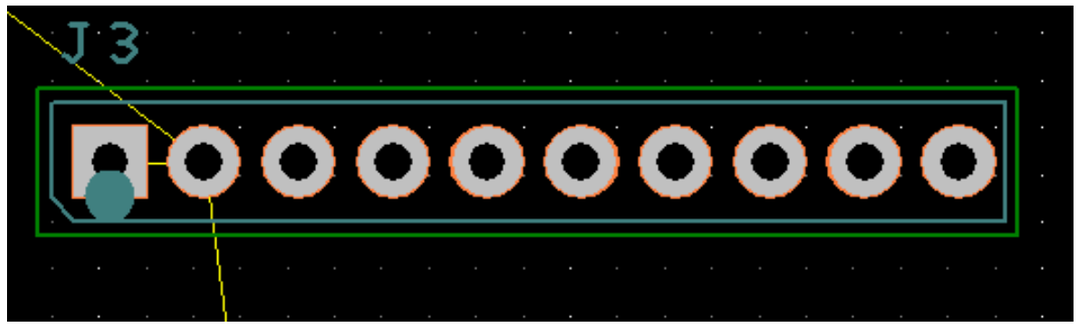
Unused Connections

Function	Signal Name	Pin Number	Acceptable Practice	Preferred Practice
GPIO	All unused GPIOs	-	NC	GND

Our advice for some of the unused I/O pins
Leave unconnected
Route to a via or logic analyzer pin
Can be used for fixing/testing

Connect digital signals to logic analyzer





PCB Layout

20+ Layers, connected by VIAs
Signals
GND and VDD planes (act like large cap)
Highspeed signals shielded with 2 GND planes

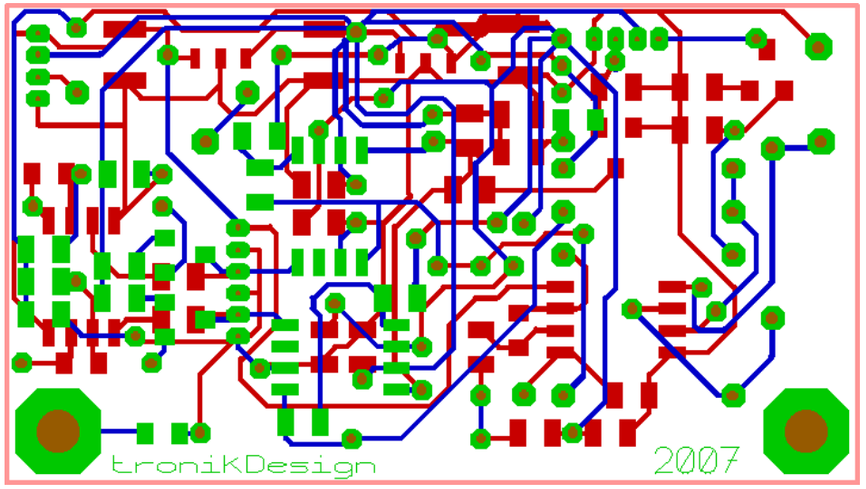
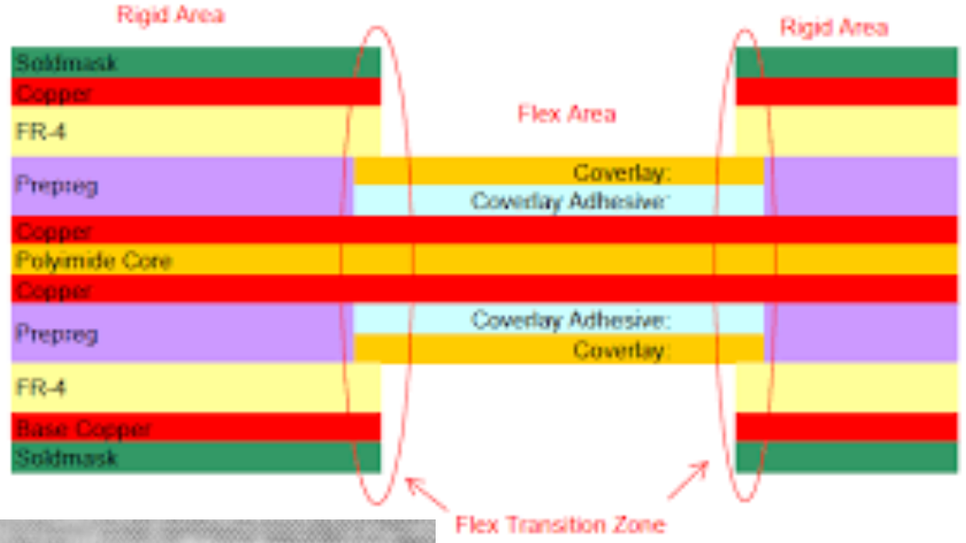
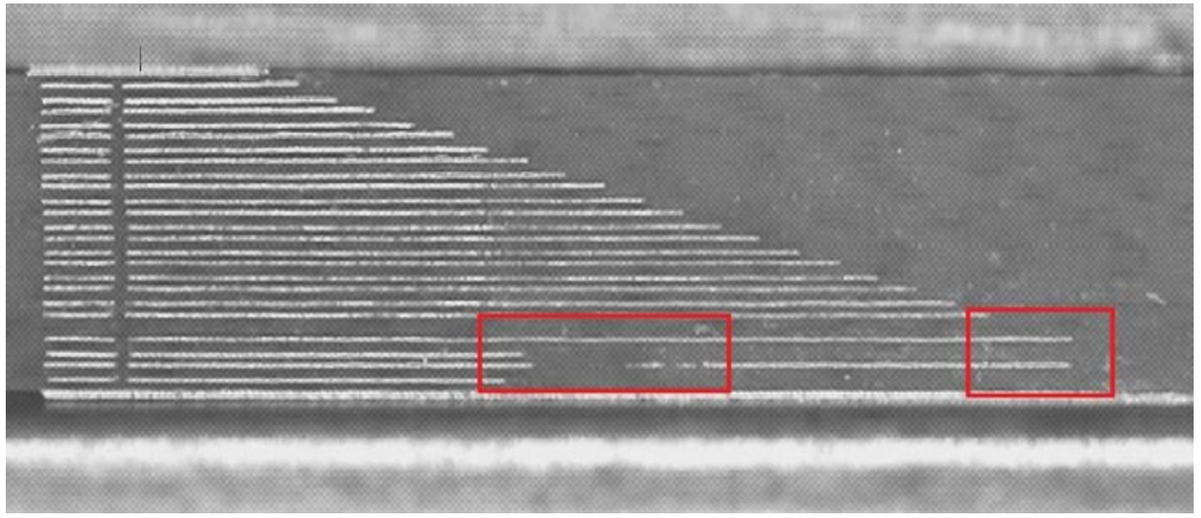


Image source: wikimedia

How many layers

- 20+ in modern designs





A bit more complex Layout..

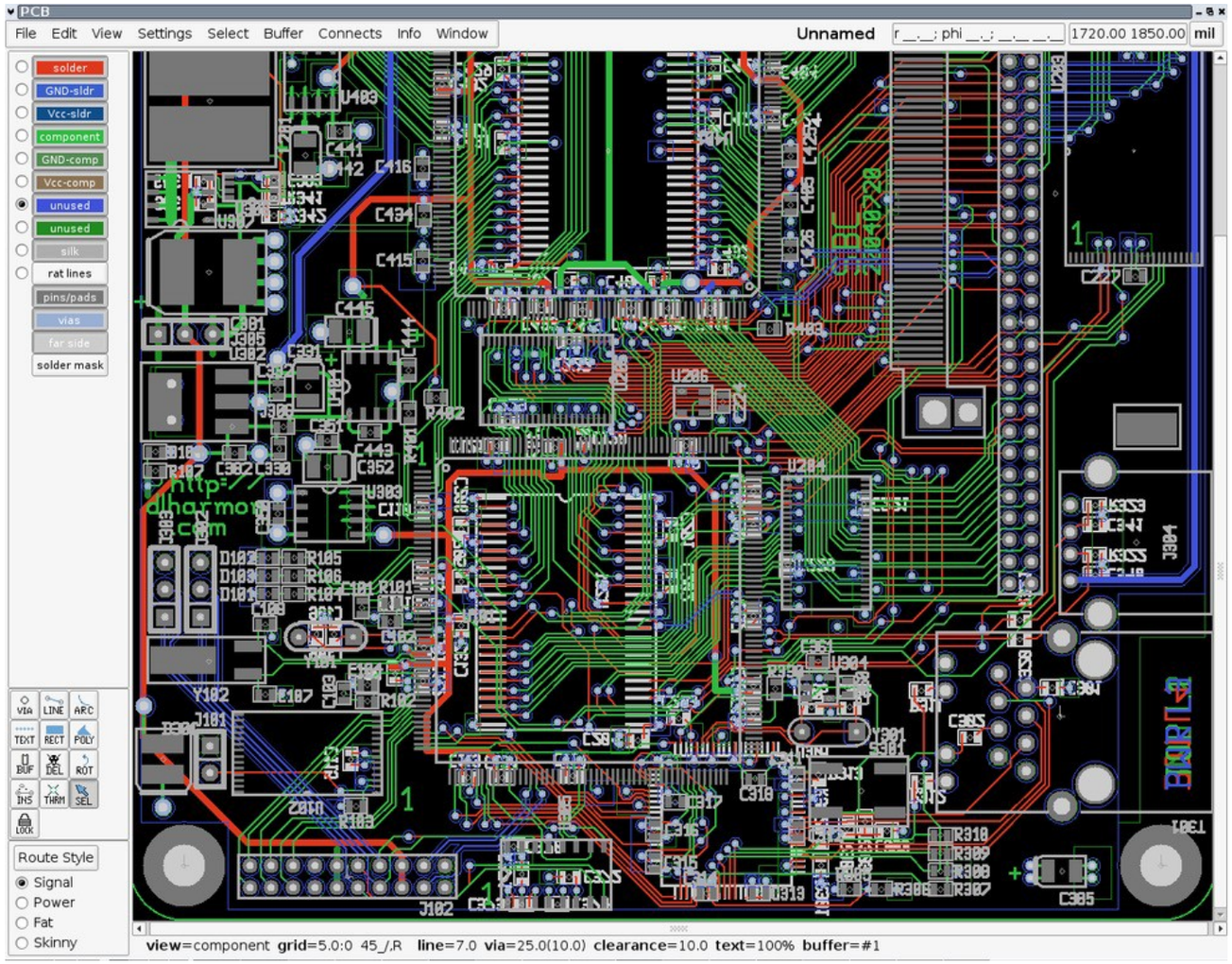


Image source:
wikimedia

PCB Design

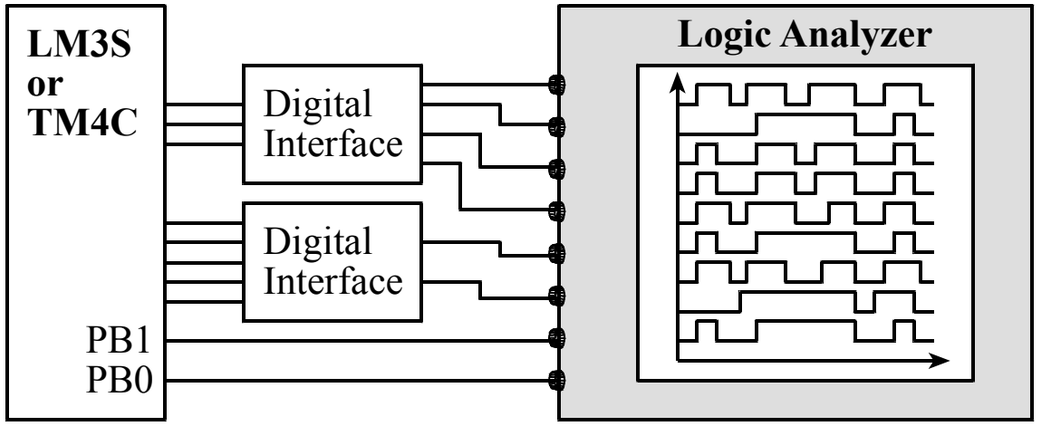
Many open source tools available
Multiple services in the Bayarea produce and assemble boards
Can even self etch PCBs
2-layer copper board
Print Mask (printer)
Etch

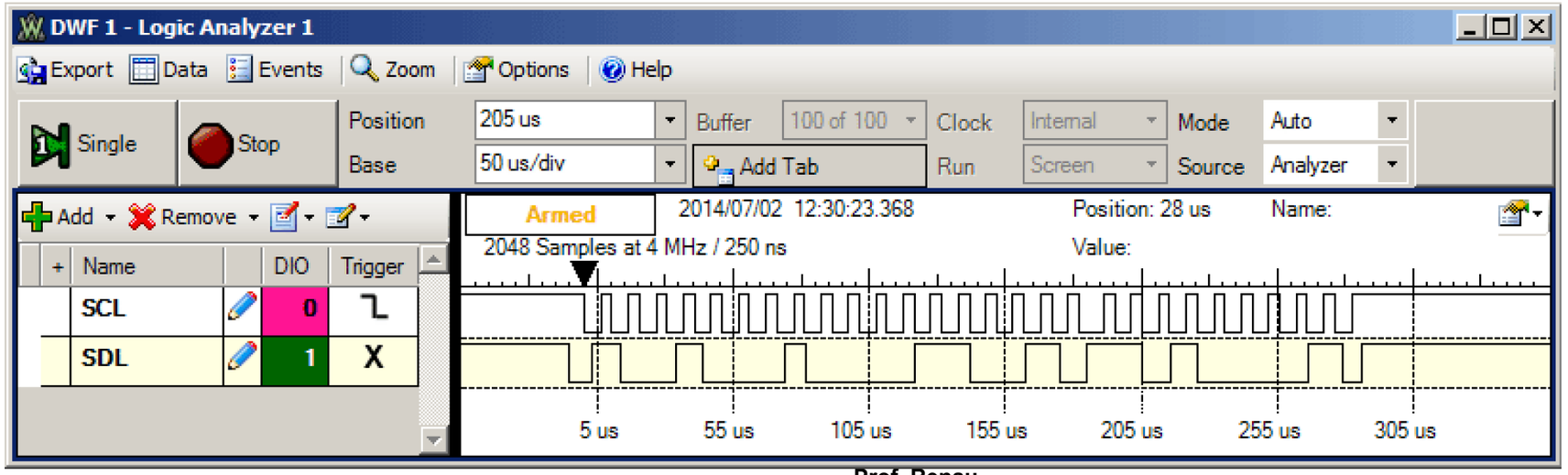
Debugging

- Types
  - performance debugging (timing)
  - functional debugging (data)
- Goal of debugging
  - maintain and improve software
  - remedy faults or to correct errors in a program
  - role of a debugger is to support this endeavor
- The debugging process
  - testing,
  - stabilizing,
  - localizing, and
  - correcting errors.

Hardware debugging tools

- Logic analyzer
  - Multiple channel, digital, storage scope
  - Flexible method of triggering





Next Class

- No lecture, just lab help in class