WELCOME

Embedded System Hardware Architectures, *Introduction*

Lecture 3 May 10th 2024

UCSC Silicon Valley Extension
PROFESSIONAL EDUCATION

Michael Wang

Student Services

E: extension@ucsc.edu
P: 408.861.3860

Schedule

Date:	Start Time:	End Time:	Meeting Type:	Location:
Mon, 04-01-2024	6:30 p.m.	9:30 p.m.	Flexible	SANTA CLARA / REMOTE
Mon, 04-08-2024	6:30 p.m.	9:30 p.m.	Flexible	SANTA CLARA / REMOTE
Mon, 04-15-2024	6:30 p.m.	9:30 p.m.	Flexible	SANTA CLARA / REMOTE
Mon, 04-22-2024	6:30 p.m.	9:30 p.m.	Flexible	SANTA CLARA / REMOTE
Mon, 04-29-2024	6:30 p.m.	9:30 p.m.	Flexible	SANTA CLARA / REMOTE
Mon, 05-06-2024	6:30 p.m.	9:30 p.m.	Flexible	SANTA CLARA / REMOTE
Mon, 05-13-2024	6:30 p.m.	9:30 p.m.	Flexible	SANTA CLARA / REMOTE
Mon, 05-20-2024	6:30 p.m.	9:30 p.m.	Flexible	SANTA CLARA / REMOTE
Mon, 06-03-2024	6:30 p.m.	9:30 p.m.	Flexible	SANTA CLARA / REMOTE
Mon, 06-10-2024	6:30 p.m.	9:30 p.m.	Flexible	SANTA CLARA / REMOTE

Fri 6:30pm May 10th

Fri 6:30pm May 17th

Wed 6:30pm May 22nd

Fri 6:30pm May 31st

(Memorial Day Weekend on May 27th – no class)

Agenda (1)

1. April 1st 6:30pm – Hybrid
   - Tear Down Analysis, Inter-IC communications
   - Basic Concepts (Serial vs Parallel bus)
   - Quiz 1 (closed Notes)

2. May 6th 6:30pm Hybrid

Microcontroller/ Microprocessor Systems / SoC Concepts

   - Quiz 2 (closed Notes)

Agenda (2)

3. May 10th Friday 6:30pm: Hybrid

- Volatile Memories (System and Architectures)
- Quiz 3 (closed Notes)

4. May13th Monday 6:30pm: Hybrid

- *Non-Volatile Memories (System and Architectures)*
- Quiz 4 (closed Notes)

Agenda (3)

5. May 17th Friday 6:30pm: Hybrid

- *Special Functions Circuitry in Embedded Processors ColdFireV1 v S5D9 Synergy v 8051: FPU, DMA*
- Quiz 5 (closed Notes)

6. May 20th Monday 6:30pm: Hybrid

- *Special Function Circuitry: GPIO, UART*
- *Hardware System Design Considerations: IC Packaging, IC Thermal Considerations*
- Quiz 6 (closed Notes)

Agenda (4)

7. May 22nd Wednesday 6:30pm: Hybrid

- *Embedded systems in Makers Faire DIY movement, single board computers, industry trends and best practices.*
- *Guest Speaker 1: Age of AI and the Transformation of Compute Infrastructure"*
- *Project 1 Presentation Due*
- Quiz 7 (Closed Notes)

8. May 31st Friday 6:30pm: Hybrid

- *Special Function Circuitry: PWM, WDT, PMIC*
- *Embedded System Design Methodology: FPGA, ASIC, Full-Custom Design, COTs*
- *Guest Speaker 2: "FPGA and SOMs"*
- Quiz 8 (Closed Notes)

(Memorial Day Weekend on May 27th – no class)

Agenda (5)

9. Jun 3rd Monday 6:30pm: Hybrid

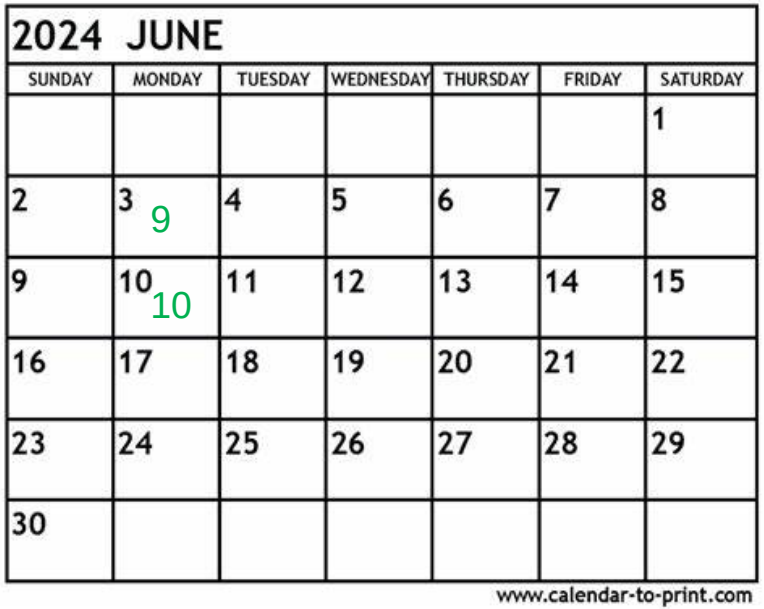
- *Special Function Circuitry: ADC , DAC, RTC*
- *Form Factor, System Benchmarking*
- *Guest Speaker 3: CM, EspressoBin / Dragon Board/ other SBCs “*
- Quiz 9 (Closed Notes)

10 Jun 10th Monday 6:30pm: Hybrid

- *CPU v GPU v TPU v NPU v VPU v XPU v DPU*
- *Software Considerations: OS, RTOS, Baremetal, Middleware*
- *Industry Case Studies*
- ***Project2 + Presentation Due,***
- ***Course Wrap Up***
- **Final Exam (Open Notes)**

ReCap on Schedule of classes

.



Project1 (May 22nd)

Choose one of the following:

1. 4-page (double spaced) minimum Research on the Topic of your choice. Topic should be related to class materials eg Main Memory development over the last 20 years.
2. Read a book on class related material and write a 4-page book review. Review topics should summarize the contents of the book and include your feedback and recommendations.
3. Designing an embedded system on paper - Choose a hardware project of your choice and draft out the system functional block diagram (1 page). Explain why you choose the components, what is the functional purpose of the component (3 page).

Project2 (due June 10th -Last day of class)

Single Board Computer / uC Eval Kit Project:

On week # 7, you will be introduced to several SBC on the market, such as Rpi, Arduino, etc. Earlier on week # 2, you have been briefed on uC Eval kit/ Demo Kit. The purpose of the Project2 is to compare and contrast uC vs SBC requirements. What are the differences in processor performance, mem subsystem requirement, display(?) requirements, OS requirement, pricing, market application etc. Compare and contrast one uC kit vs a SBC.
This can be expanded to compare other topics such as DDR4 vs LPDDR4, etc.

Volatile Memories

Memory Managers 1

How does the CPU interface with the memory?

2 common types of Memory Managers: Memory Controller and Memory Management Unit (MMU)

Memory Controller -

- **Glue-less interface to different kinds of memories eg DRAM, SRAM, cache**
- **Synchronize access and verify integrity of data**

MMU:

- **Translate logical address into physical address**
- **Security, cache control, bus arbitration**
- **Appropriate exceptions**

Memory Managers 2

The CPU “sees” 1 linear physical address

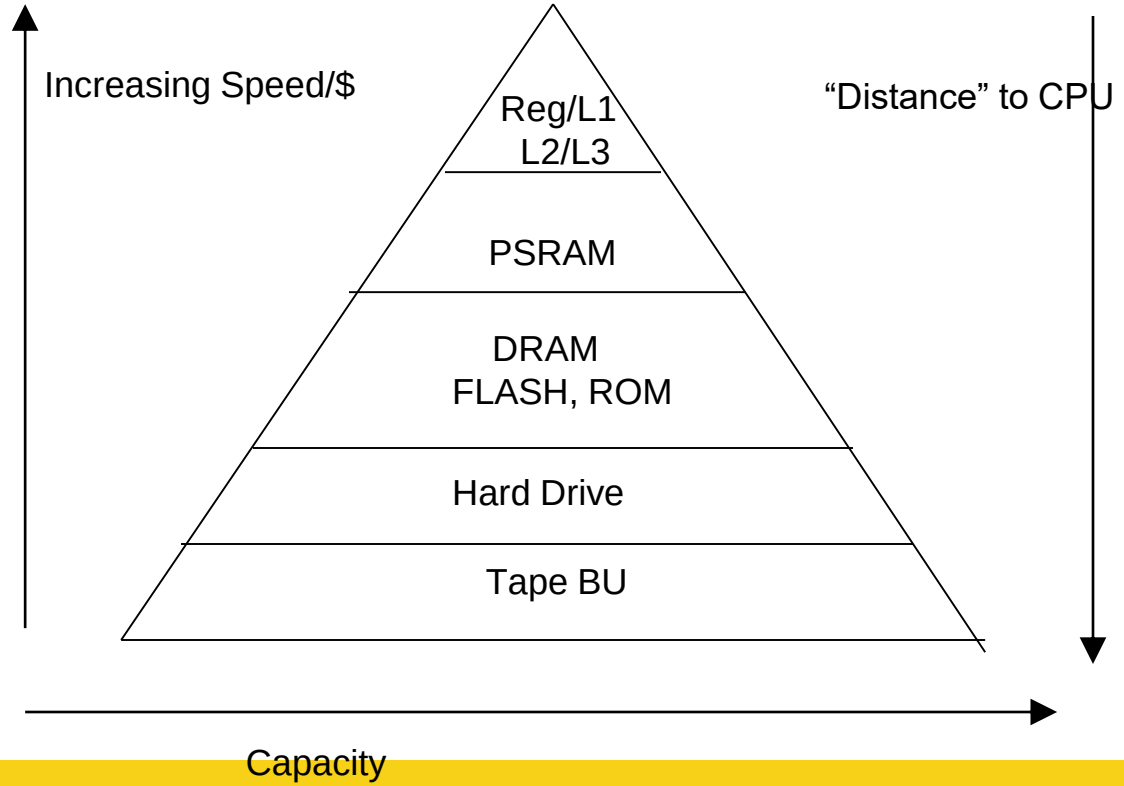
For a 32-bit address this 2^{32} = 4GB of memory
MMU:
Virtual Address → Mapping → Physical Address
(Kernel/ User Space) Flash, SRAM, DRAM, Registers

Mapping is done by Translation Look-aside Buffer (TLB): small cache mechanism in a process known as table-walk

Memory Trends

- Memory Hierarchy
- DRAM: -need to be refreshed
- Early 90s EDO,FPM
- Mid to Late 90s SDRAM
- 2000s DDR, RAMBUS,
- 2006-8 DDR2,
- Now future DDR3, XDR

Memory Hierarchy



Memory Type (1)

RAM- Random Access Memory

DRAM- Dynamic Random Access Memory

SRAM- Static Random Access Memory

Clock = Synchronous

No Clock = Asynchronous

SDRAM

Parity Bit/ ECC

Buffered = registered

Memory Type (2)

ROM – Read Only Memory

- Mask ROM

-EPROM Erasable Programmable

- OTP PROM (EPROM w/o Window)

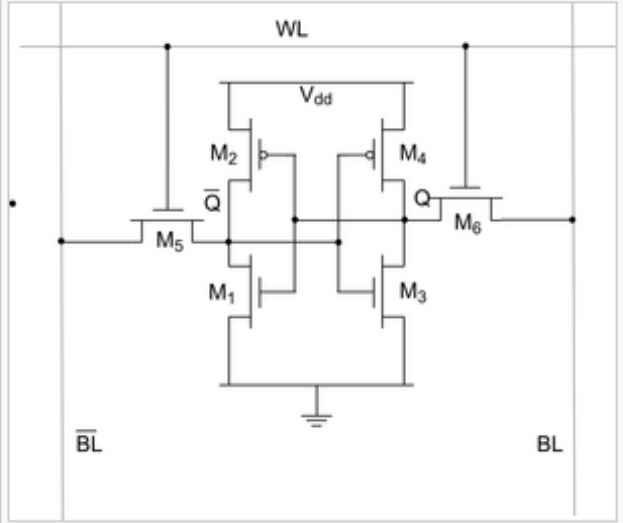
-EEPROM Electrically Erasable

Flash (Block erase)

-NAND Flash

-NOR Flash

SRAM (1)



A six-transistor CMOS SRAM cell.

Source attributed to– wikipedia.com

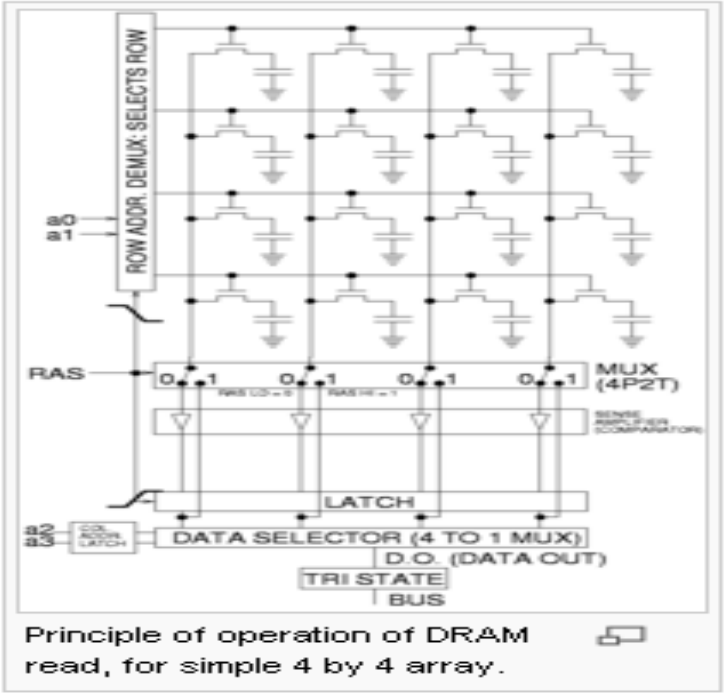
SRAM (2)

- Six transistors for one bit in CMOS
- M address lines, n data lines =2^mxn bits

- PSRAM = Pseudo-static RAM = DRAM with self refreshing circuits.

DRAM (1)

DRAM – Dynamic RAM



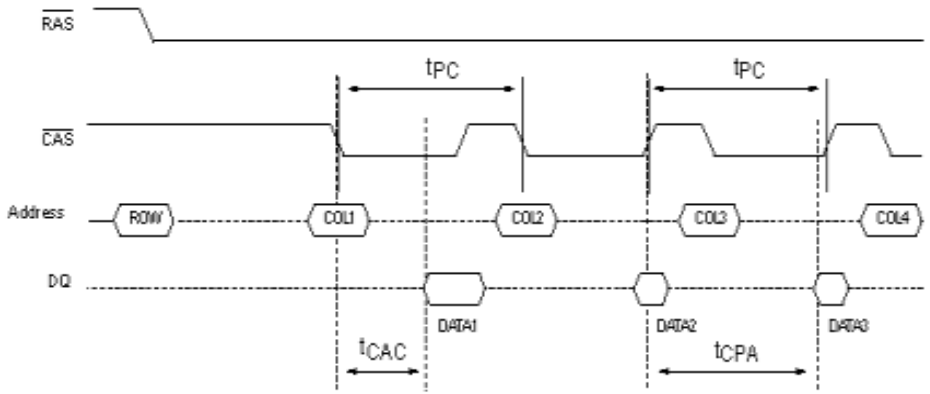
Principle of operation of DRAM read, for simple 4 by 4 array.

Source attributed to– wikipedia.com

DRAM (2)

- DRAM – Dynamic RAM
- FPM, EDO, BEDO

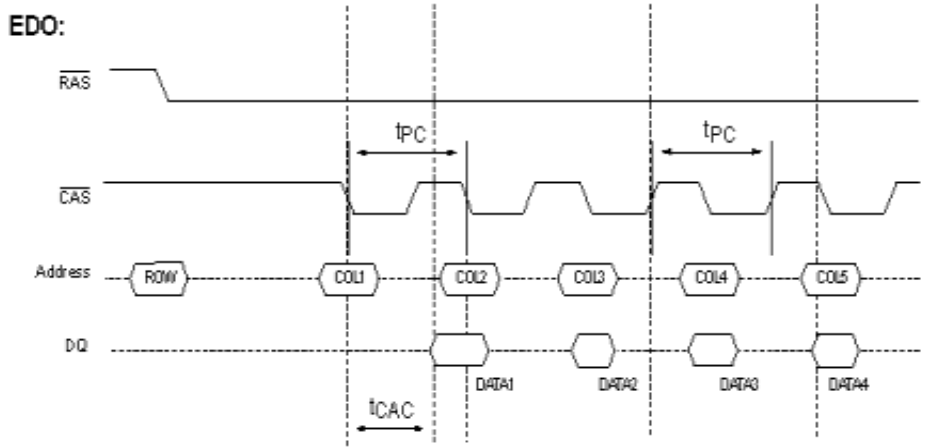
Fast Page Mode:



Source attributed to– wikipedia.com

DRAM (3)

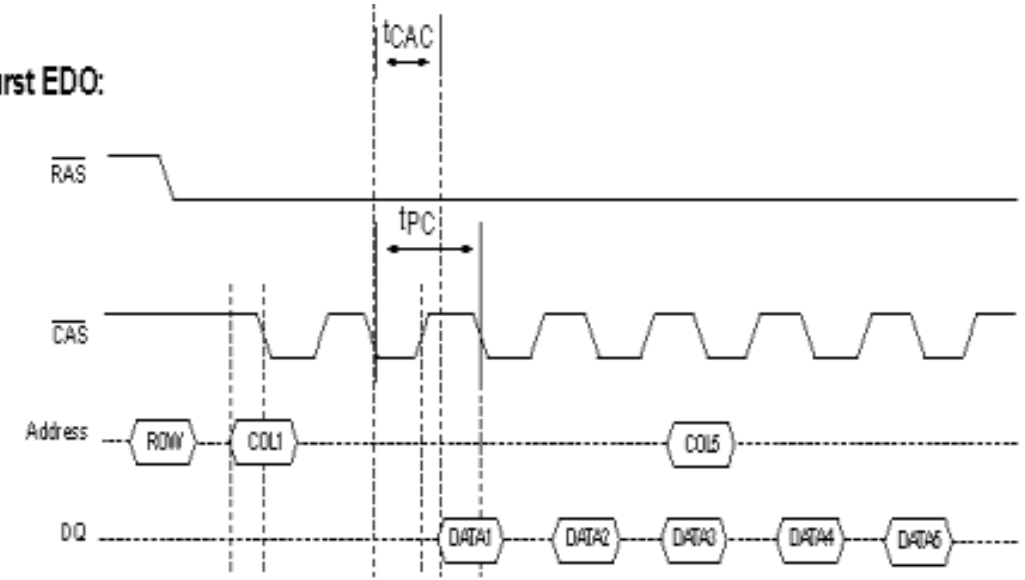
- EDO



Source attributed to– wikipedia.com

DRAM (4)

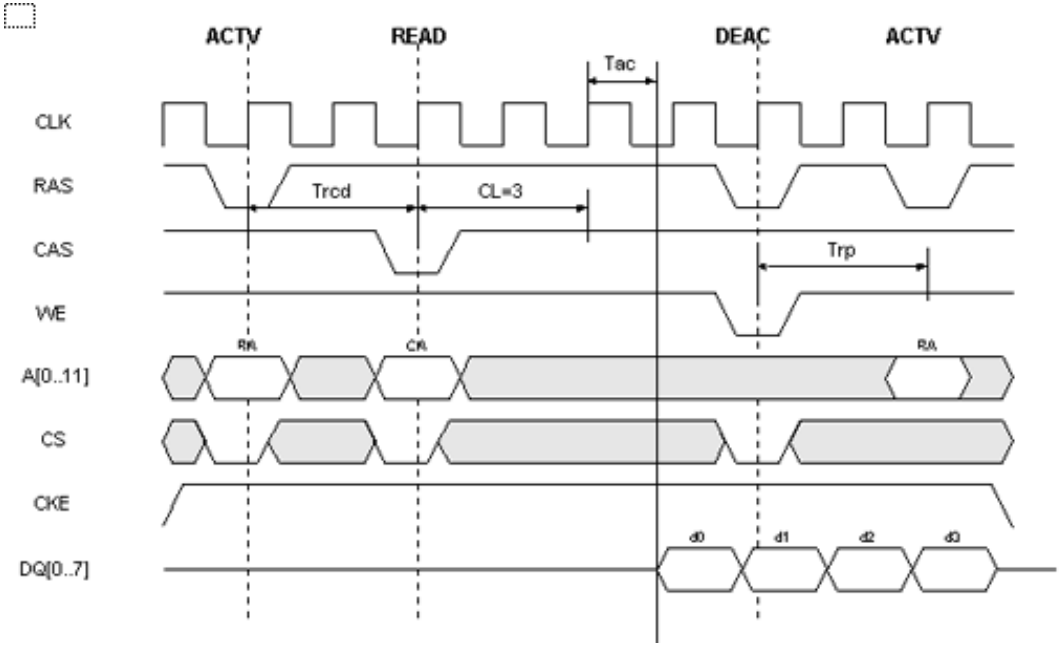
- BEDO



Source attributed to– wikipedia.com

DRAM (5)

- SDRAM



Source attributed to– wikipedia.com

DRAM (6)

- SDRAM 168pin
- What does 2-2-2 SDRAM mean?

- **tRP** - The speed or length of time that it takes DRAM to terminate one Row Access and start another. Switching between memory banks.

- **tRCD** - The time required between /RAS (Row Address Select) and /CAS (Column Address Select) access. Although this is an extreme oversimplification, think of tRCD this way. Picture an Excel chart with number across the top and along the left side. The numbers down the left side represent the Rows and the numbers across the top represents the Columns. The time it would take you to move down to Row 20 and across to Column 20 is RAS to CAS.

- **tCL** - (or **CL**) **CAS** Latency Latency is the number that refers to the ratio between the column access time and the clock cycle time rounded to the next higher whole number. It is derived from dividing the column access time by the clock frequency, and raising the result to the next whole number. **tCL** = **tCAC** / **tCLK**. If you look above at the illustration for SDRAM burst read timing, CAS latency means the length of access time **tAC** is measured from the 2nd clock edge after the "Read" command.

Source attributed to– wikipedia.com

DRAM (7)

DDR(1) Specifications 184 pin Dimm

= 2 bit prefetch buffers, 2.5V

[edit]

Chip specification

- DDR-200: DDR-SDRAM memory chips specified to run at 100 MHz
- DDR-266: DDR-SDRAM memory chips specified to run at 133 MHz
- DDR-333: DDR-SDRAM memory chips specified to run at 166 MHz
- DDR-400: DDR-SDRAM memory chips specified to run at 200 MHz

Stick/module specification

- PC-1600: DDR-SDRAM memory module specified to run at 100 MHz using DDR-200 chips, 1.600 GByte/s bandwidth per channel.
- PC-2100: DDR-SDRAM memory module specified to run at 133 MHz using DDR-266 chips, 2.133 GByte/s bandwidth per channel
- PC-2700: DDR-SDRAM memory module specified to run at 166 MHz using DDR-333 chips, 2.667 GByte/s bandwidth per channel
- PC-3200: DDR-SDRAM memory module specified to run at 200 MHz using DDR-400 chips, 3.200 GByte/s bandwidth per channel

Source attributed to– wikipedia.com

DRAM (8)

DDR2 Specification 240pin Dimm

DDR1 + onchip termination + 4 bit prefetch buffers 1.8V

Chips

- DDR2-400: DDR-SDRAM memory chips specified to run at 100 MHz, I/O clock at 200 MHz
- DDR2-533: DDR-SDRAM memory chips specified to run at 133 MHz, I/O clock at 266 MHz
- DDR2-667: DDR-SDRAM memory chips specified to run at 166 MHz, I/O clock at 333 MHz
- DDR2-800: DDR-SDRAM memory chips specified to run at 200 MHz, I/O clock at 400 MHz

Sticks/Modules

- PC2-3200: DDR2-SDRAM memory stick specified to run at 200 MHz using DDR2-400 chips, 3.200 GB/s bandwidth
- PC2-4200: DDR2-SDRAM memory stick specified to run at 266 MHz using DDR2-533 chips, 4.267 GB/s bandwidth
- PC2-5300: DDR2-SDRAM memory stick specified to run at 333 MHz using DDR2-667 chips, 5.333 GB/s bandwidth
- PC2-6400: DDR2-SDRAM memory stick specified to run at 400 MHz using DDR2-800 chips, 6.400 GB/s bandwidth

Source attributed to– wikipedia.com

DRAM (9)

DDR3 Specification 240 pin Dimm

DDR2 + onchip termination + 8 bit prefetch buffers 1.5V 90nm process

Ad: Higher Bandwidth, Lower Power

Chips

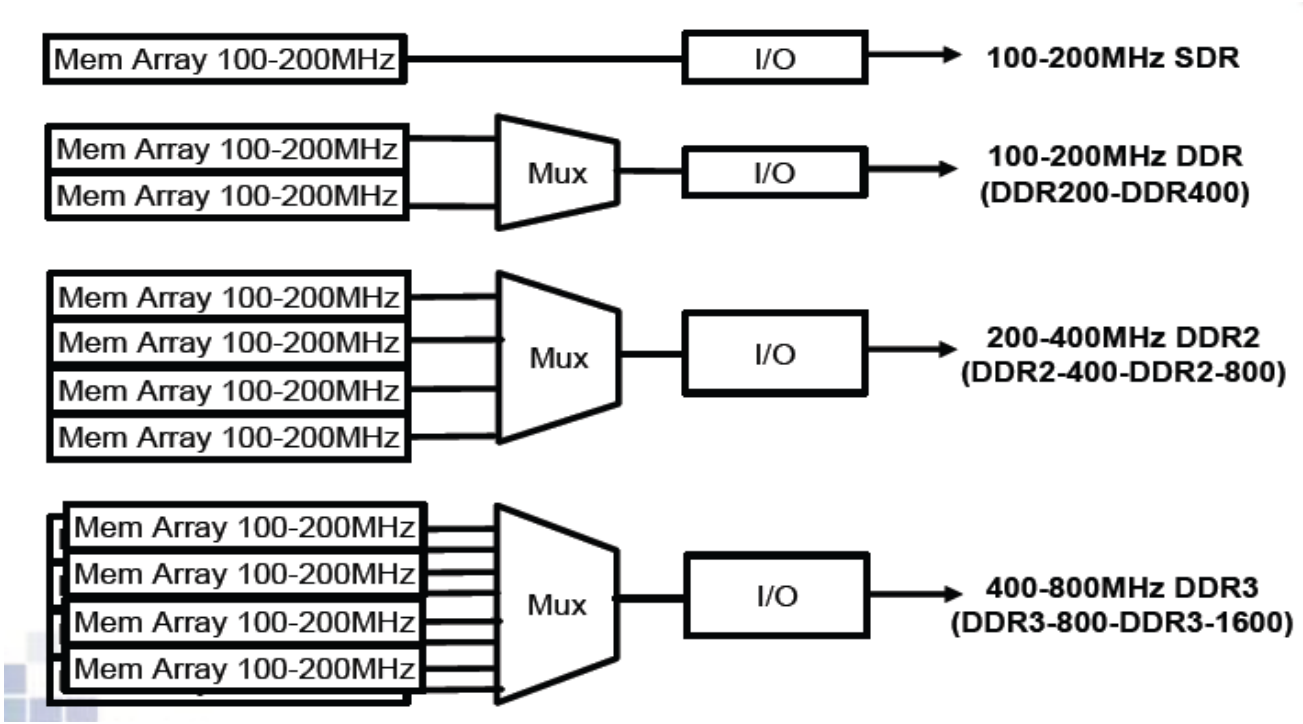
- DDR3-800 : DDR3-SDRAM memory chips specified to run at 100 MHz, I/O clock at 400 MHz
- DDR3-1066: DDR3-SDRAM memory chips specified to run at 133 MHz, I/O clock at 533 MHz

Sticks/Modules

- PC3-6400: DDR3-SDRAM memory stick specified to run at 400 MHz using DDR3-800 chips, 6.40 GB/s bandwidth
- PC3-8500: DDR3-SDRAM memory stick specified to run at 533 MHz using DDR3-1066 chips, 8.53 GB/s bandwidth

Source attributed to– wikipedia.com

DRAM (9)



Source attributed to– wikipedia.com

DRAM (10)

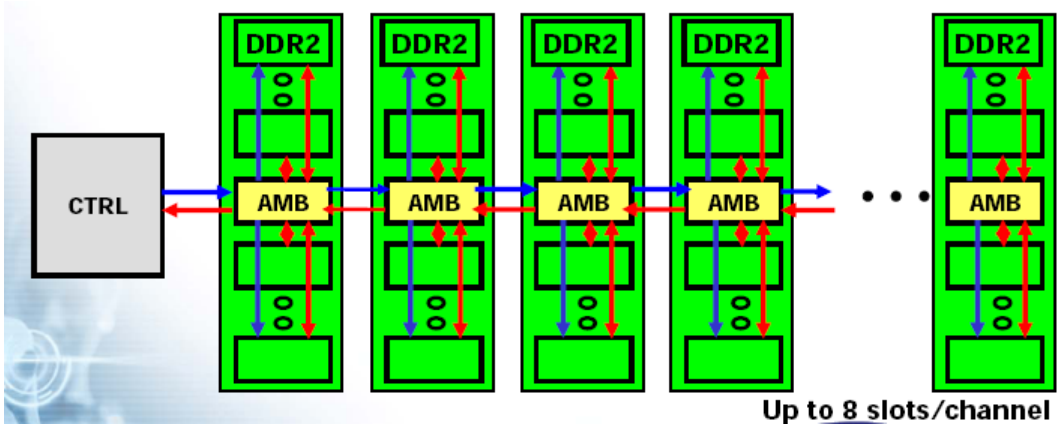
XDR by Rambus

Performance:

- Clock rate at 400 MHz (600, 800 and 1000 MHz planned)
- 8 bits per clock and lane (ODR = Octal Data Rate) gives 3.2 GBit/s (4.8, 6.4 and 8 Gbit/s planned)
- 8 or 16 lanes per chip gives 3.2 to 16 GByte/s

DRAM (11)

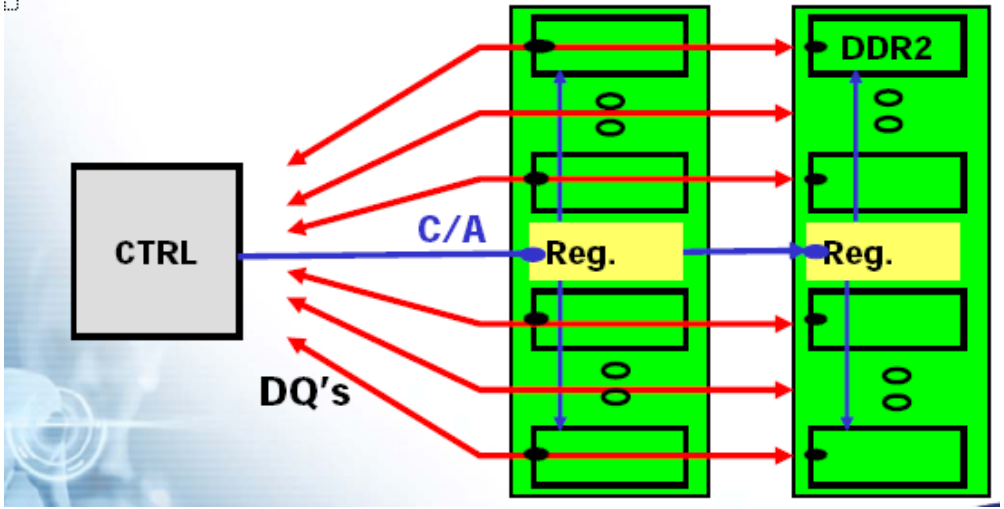
FBDIMM uses AMB (Advanced Mem Buffer) to serialize data between controller and AMB → increases memory width without pin count (downside: latency increases)



Source attributed to– denali.com

DRAM (12)

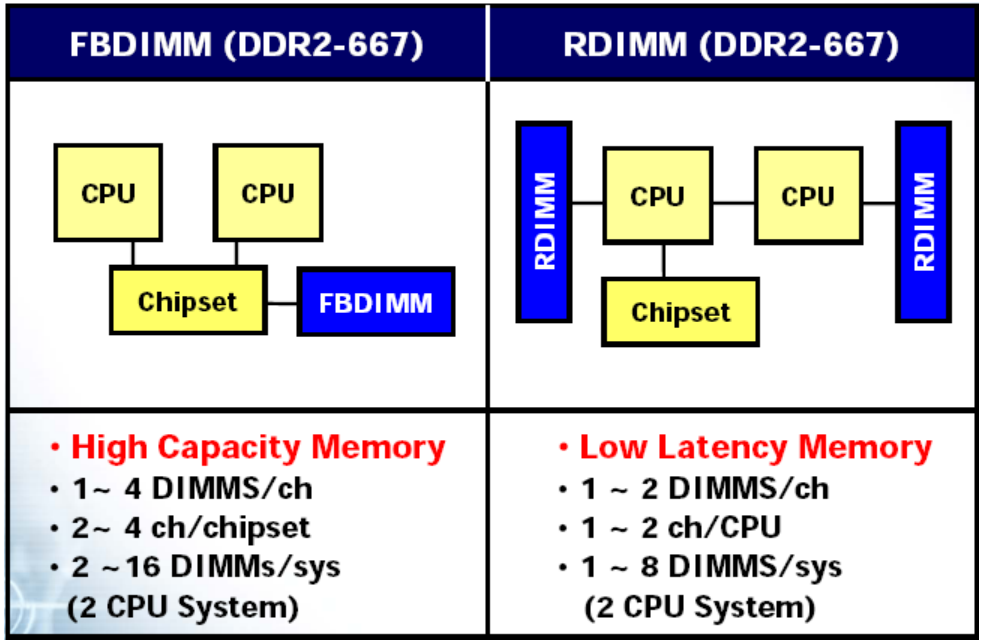
Registered Dimm = use of registers to latch address and control signals to ensure signal integrity



Source attributed to– denali.com

DRAM (13)

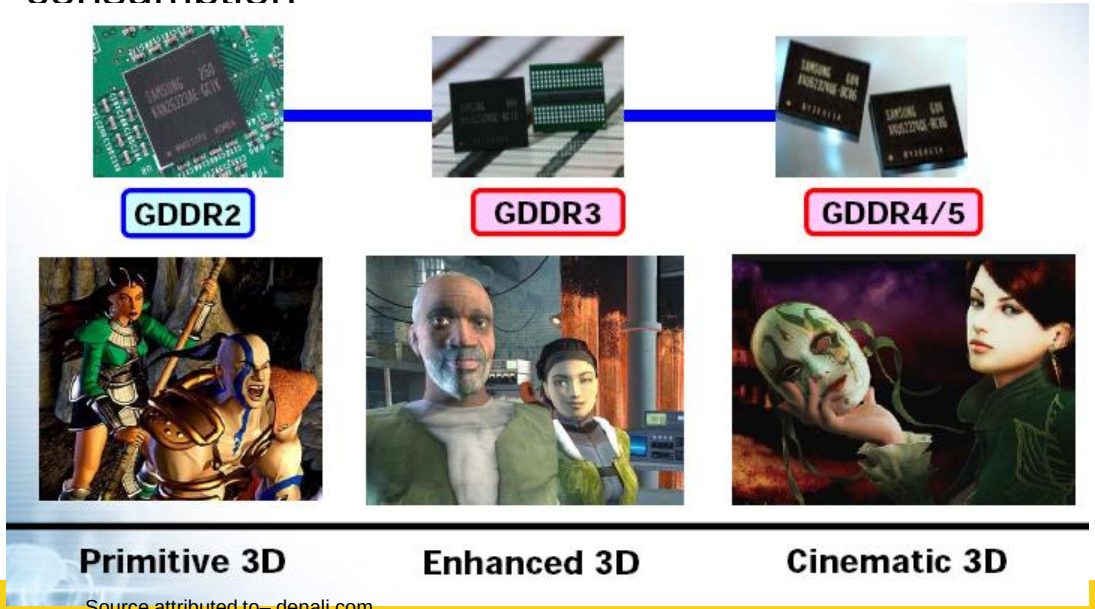
Server Architecture Examples



Source attributed to– denali.com

DRAM (14)

GDDR2 / 3 /4/ 5Graphics DDR
GDDR2 has higher operating voltage than DDR2 (2.5V vs 1.8V) – higher bandwidth, more power consumption



Source attributed to– denali.com

GDDR Comparison

Feature	GDDR5	GDDR5X	GDDR6	GDDR6X
Density	From 512Mb to 8Gb	8Gb	8Gb, 16Gb	8Gb, 16Gb[1]
V_{DD} and V_{DDQ}	Either 1.5V or 1.35V	1.35V	Either 1.35V or 1.25V	Either 1.35V or 1.25V
V_{PP}	N/A	1.8V	1.8V	1.8V
Data rates (per pin)	Up to 8 Gb/s	Up to 12Gb/s	Up to 16 Gb/s	19 Gb/s, 21 Gb/s, >21 Gb/s[1]
Channel count	1	1	2	2
Access granularity	32 bytes	64 bytes 2x 32 bytes in pseudo 32B mode	2 ch x 32 bytes	2 ch x 32 bytes
Burst length	8	16 / 8	16	8 in PAM4 mode[2] 16 in RDQS mode
Signaling	POD15/POD135	POD135	POD135/POD125	PAM4 POD135/POD125
Package	BGA-170 14mm x 12mm 0.8mm ball pitch	BGA-190 14mm x 12mm 0.65mm ball pitch	BGA-180 14mm x 12mm 0.75mm ball pitch	BGA-180 14mm x 12mm 0.75mm ball pitch
I/O width	x32/x16	X32/x16	2 ch x16/x8	2 ch x16/x8[3]
Signal count	61 - 40 DQ, DBI, EDC - 15 CA - 6 CK, WCK	61 - 40 DQ, DBI, EDC - 15 CA - 6 CK, WCK	70 or 74 - 40 DQ, DBI, EDC - 24 CA - 6 or 10 CK, WCK	70 or 74 - 40 DQ, DBI, EDC - 24 CA - 6 or 10 CK, WCK
PLL, DCC	PLL	PLL	PLL, DCC	DCC
CRC	CRC-8	Modified CRC-8	2x CRC-8	2x CRC-8[4]
V_{REFD}	External or internal per 2 bytes	Internal per byte	Internal per pin	Internal per pin 3 sub-receivers per pin
Equalization		RX/TX	RX/TX	RX/TX
V_{REFC}	External	External or Internal	External or Internal	External or Internal
Self refresh (SRF)	Yes Temp. Controlled SRF	Yes Temp. Controlled SRF Hibernate SRF	Yes Temp. Controlled SRF Hibernate SRF VDDQ-off	Yes Temp. Controlled SRF Hibernate SRF VDDQ-off
Scan	SEN	IEEE 1149.1 (JTAG)	IEEE 1149.1 (JTAG)	IEEE 1149.1 (JTAG)

[1] Planned
[2] PAM4 encodes two data bits per UI
[3] Configured at power-up
[4] GDDR6X: half data rate cyclic redundancy check jedec.org scheme

SOURCE: micron.com

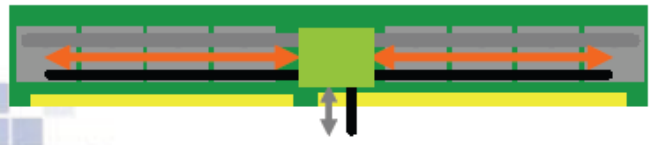
DRAM Module(1)

Terminology: Module Types

DIMM = Dual Inline Memory Module

- **UDIMM** = Unbuffered
  Address bus and clocks connected directly to DRAMs

- **RDIMM** = Registered
  Address bus and clock redriven to DRAMs



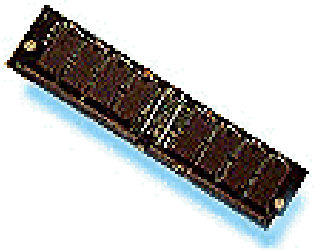
- **FB-DIMM** = Fully Buffered
  Address and data buses packetized and redriven to DRAMs

Source attributed to– denali.com

DRAM Module(2)

32MB SIMM FPM Samsung

- Samsung Memory
- 8x32
- 72pin
- 32 MB
- 60ns
- 4x4 16-chip 2K ref



32MB SIMM EDO Micron

- Micron memory
- 8x32
- 72pin
- 32MB
- 60ns
- 4x4 chips 2K ref

Source attributed to– mal;abs.com

DRAM Module (3)

STT D333 512M 172Pins DIMM

Specification

- Mfr Part Number: D27MA12G
- Type: DDR333 Micro DIMM
- Speed: PC2700 (DDR333)
- Pins: 172-Pin
- Size: 512MB

Samsung 512MB DDR333 64x64/32x16

Specification

- Mfr Part Number: M470L6524BT0-CB300
- Type: SODIMM
- Capacity: 512MB
- Speed: PC2700 DDR333
- Size&Bit: 64Mx64/32Mx16
- Pins: 200pin
- Samsung Original Memory

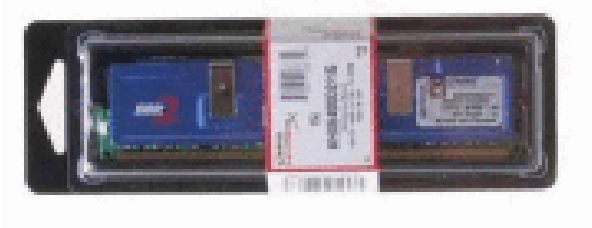
Source attributed to– mal;abs.com

DRAM Module (4)

DRAM Master DDR400 1G/64x8

Specification

- Mfr Part Number: D400/1GSAM
- Type: DDR
- Capacity: 1GB
- Speed: PC3200 DDR400
- Size&Bit: 64x8
- Pins: 184pin
- Samsung Chip
- Single Module



Kingston KHX6400D2/1G D2-800 1GB

Specification

- Mfr Part Number: KHX6400D2/1G
- Type: DDR2
- Capacity: 1 GB
- Speed: PC6400 800MHz
- Size & Bit: 128M x 64
- Pins: 240pin
- ECC: No
- Registered: No
- CL5

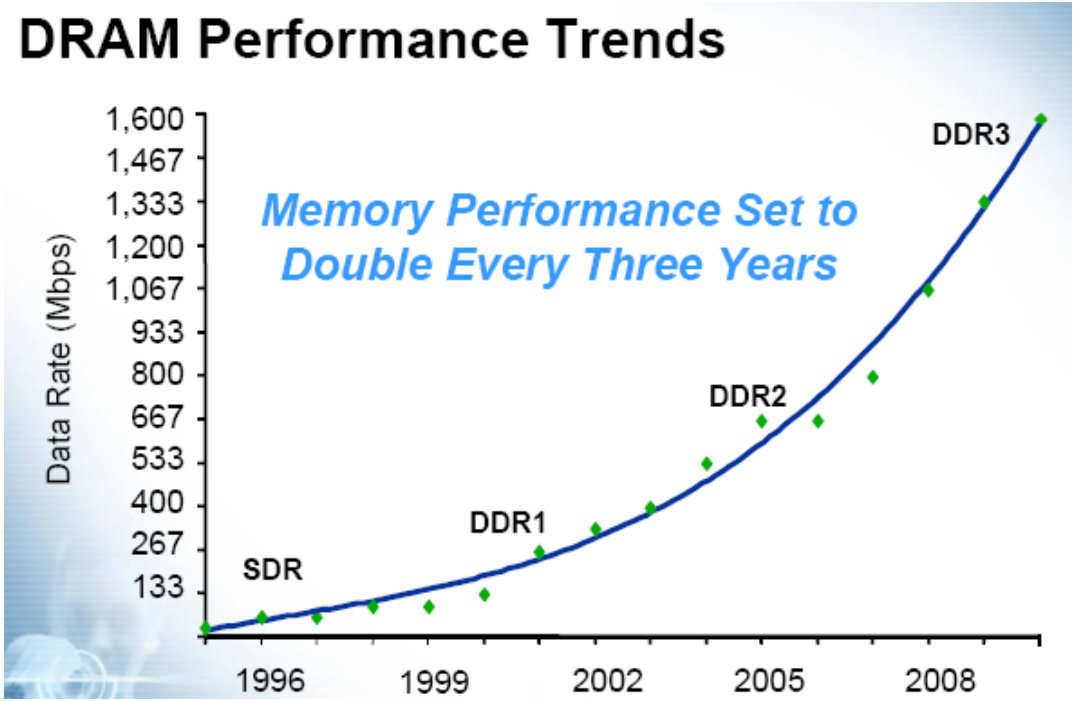
Source attributed to– mal;abs.com

DRAM Module (5)

Infineon FBDIMM

Source attributed to– infineon.com

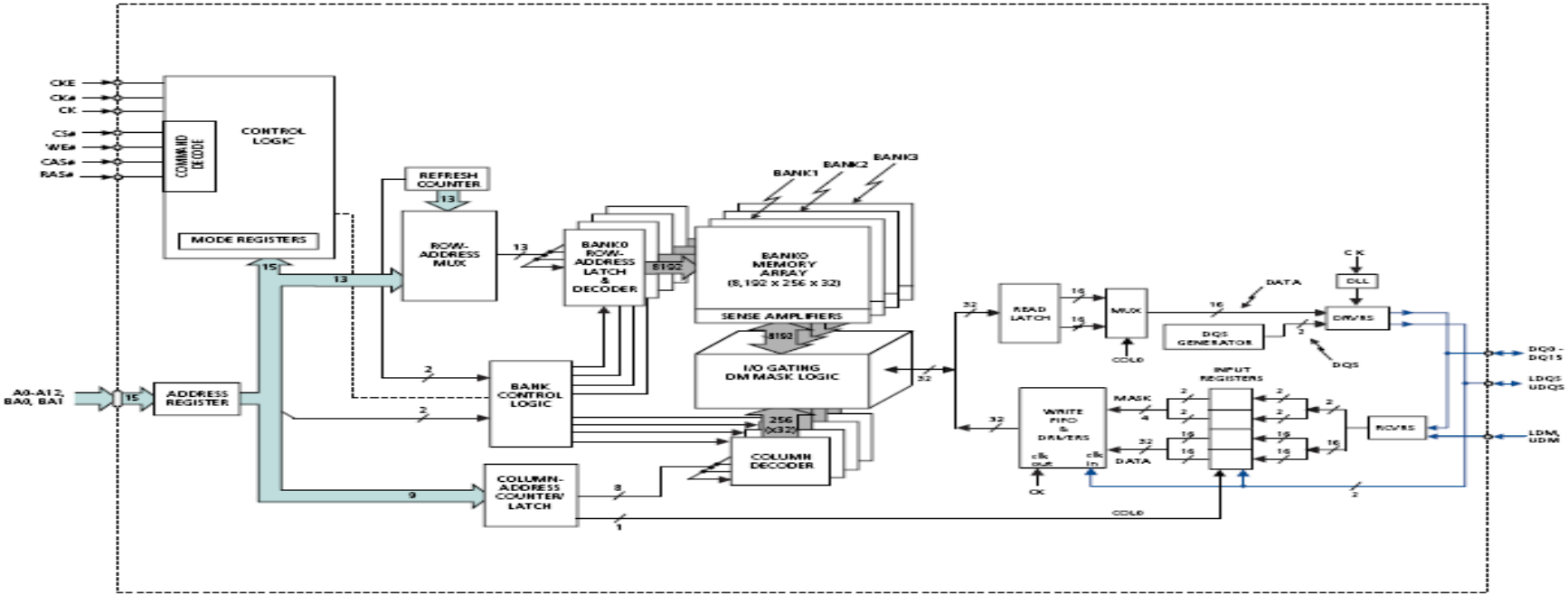
DRAM Module (6)



Source attributed to– denali.com

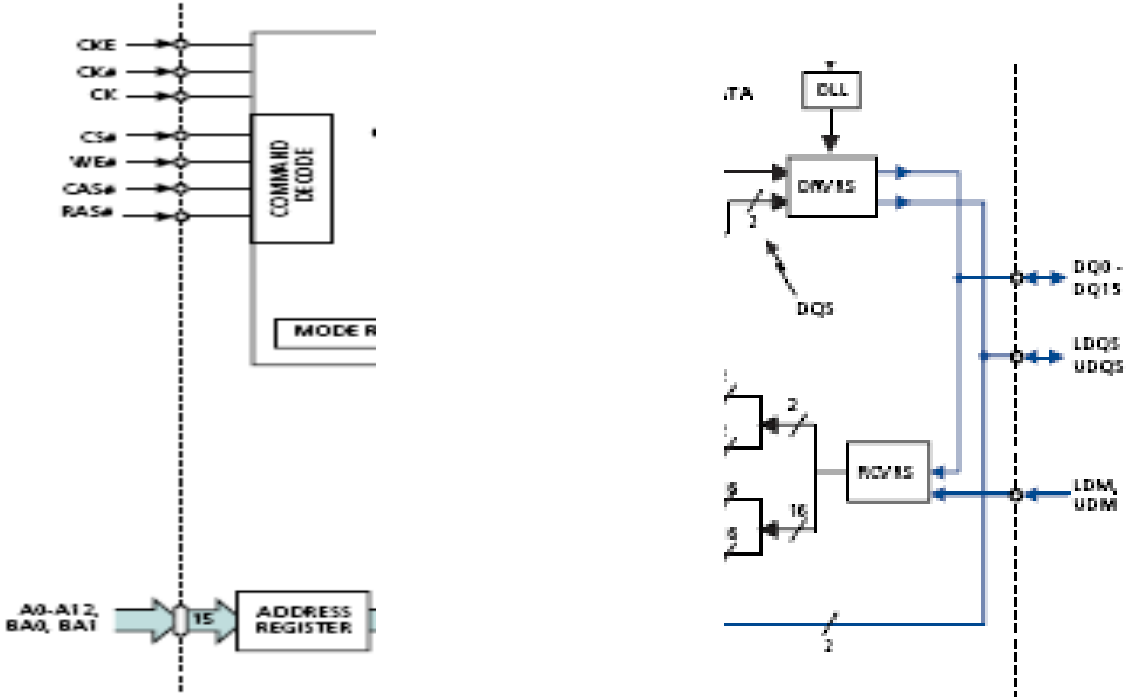
DRAM Module (7)-DDR 256Mb device -16Mx16

Figure 4: Functional Block Diagram: 16 Meg x 16



Source attributed to– micron.com

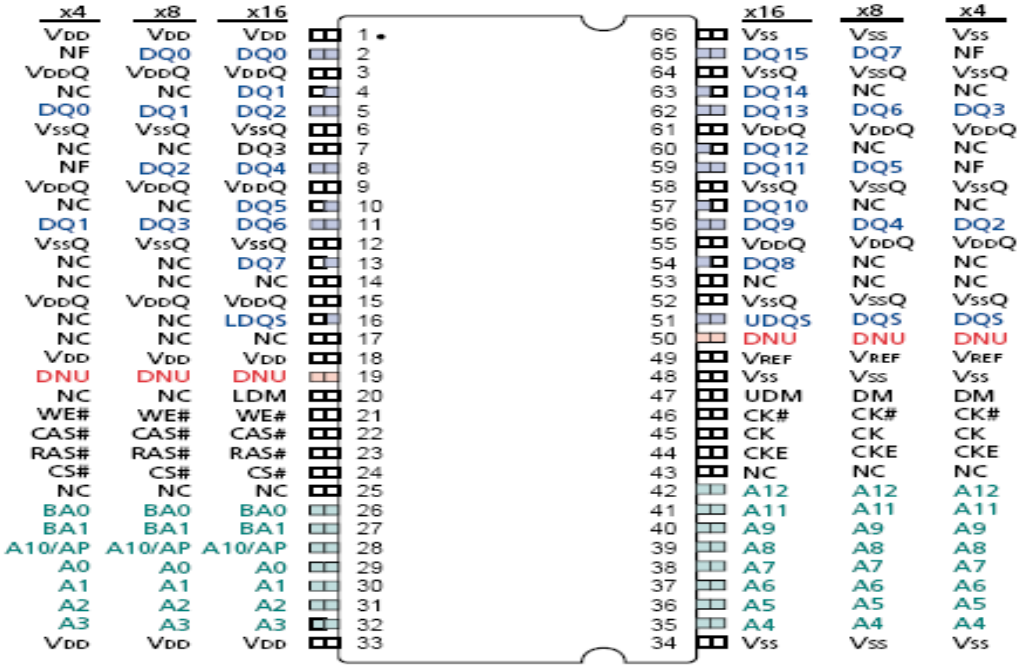
DRAM Module (8)-DDR 256Mb device -16Mx16



Source attributed to– micron.com

DRAM Module (9) Device DDR 256Mb

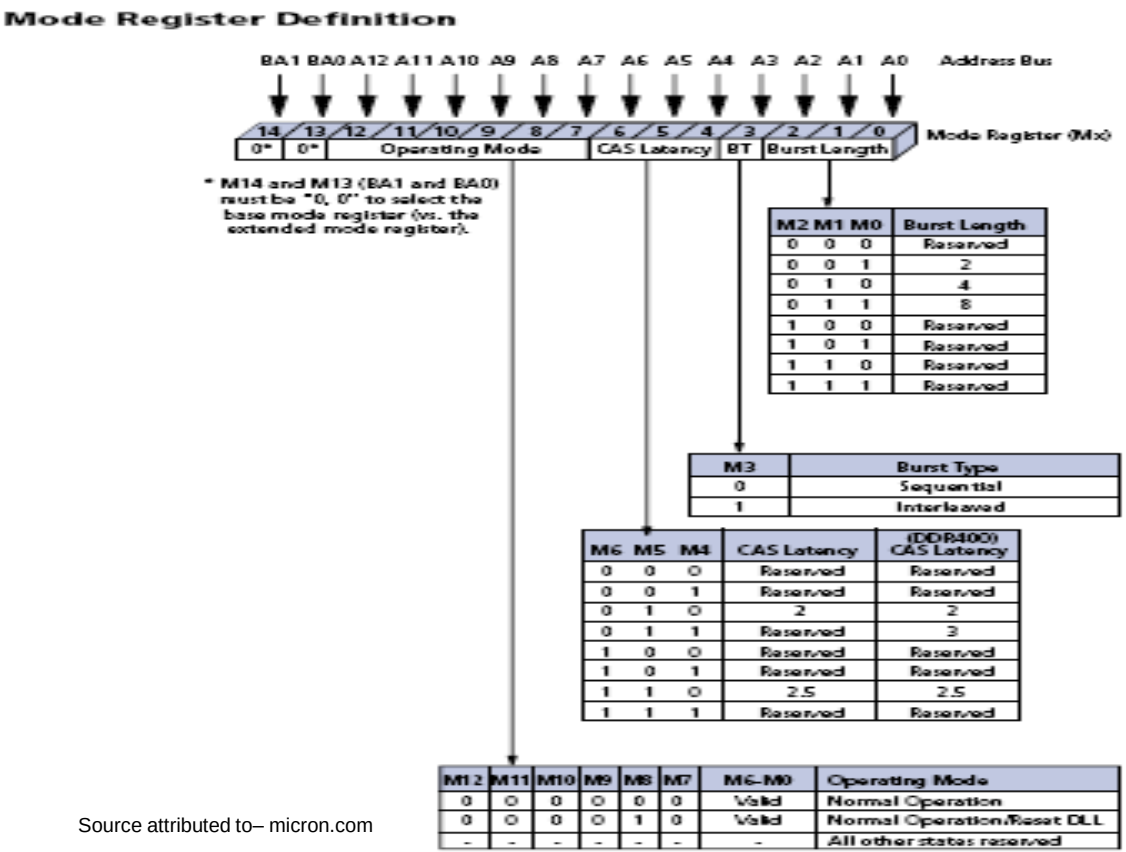
Pin Assignment (Top View) 66-Pin TSOP



x4	x8	x16			x16	x8	x4
VDD	VDD	VDD	1	66	VSS	VSS	VSS
NF	DQ0	DQ0	2	65	DQ15	DQ7	NF
VDDQ	VDDQ	VDDQ	3	64	VSSQ	VSSQ	VSSQ
NC	NC	DQ1	4	63	DQ14	NC	NC
DQ0	DQ1	DQ2	5	62	DQ13	DQ6	DQ3
VSSQ	VSSQ	VSSQ	6	61	VDDQ	VDDQ	VDDQ
NC	NC	DQ3	7	60	DQ12	NC	NC
NF	DQ2	DQ4	8	59	DQ11	DQ5	NF
VDDQ	VDDQ	VDDQ	9	58	VSSQ	VSSQ	VSSQ
NC	NC	DQ5	10	57	DQ10	NC	NC
DQ1	DQ3	DQ6	11	56	DQ9	DQ4	DQ2
VSSQ	VSSQ	VSSQ	12	55	VDDQ	VDDQ	VDDQ
NC	NC	DQ7	13	54	DQ8	NC	NC
NC	NC	NC	14	53	NC	NC	NC
VDDQ	VDDQ	VDDQ	15	52	VSSQ	VSSQ	VSSQ
NC	NC	LDQS	16	51	UDQS	DQS	DQS
NC	NC	NC	17	50	DNU	DNU	DNU
VDD	VDD	VDD	18	49	VREF	VREF	VREF
DNU	DNU	DNU	19	48	VSS	VSS	VSS
NC	NC	LDM	20	47	UDM	DM	DM
WE#	WE#	WE#	21	46	CK#	CK#	CK#
CAS#	CAS#	CAS#	22	45	CK	CK	CK
RAS#	RAS#	RAS#	23	44	CKE	CKE	CKE
CS#	CS#	CS#	24	43	NC	NC	NC
NC	NC	NC	25	42	A12	A12	A12
BA0	BA0	BA0	26	41	A11	A11	A11
BA1	BA1	BA1	27	40	A9	A9	A9
A10/AP	A10/AP	A10/AP	28	39	A8	A8	A8
A0	A0	A0	29	38	A7	A7	A7
A1	A1	A1	30	37	A6	A6	A6
A2	A2	A2	31	36	A5	A5	A5
A3	A3	A3	32	35	A4	A4	A4
VDD	VDD	VDD	33	34	VSS	VSS	VSS

Source attributed to– micron.com

DRAM Module (10)–DDR



Source attributed to– micron.com

DRAM Module(11) Burst Definition

Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2	–	–	A0	–	–
	–	–	0	0-1	0-1
	–	–	1	1-0	1-0
4	–	A1	A0	–	–
	–	0	0	0-1-2-3	0-1-2-3
	–	0	1	1-2-3-0	1-0-3-2
	–	1	0	2-3-0-1	2-3-0-1
	–	1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0	–	–
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Source attributed to– micron.com

DRAM Module (12) Commands

Table 8: Truth Table – Commands

Note 1 applies to all commands.

Name (Function)	CS#	RAS#	CAS#	WE#	Addr	Notes
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER	L	L	L	L	Op-Code	2

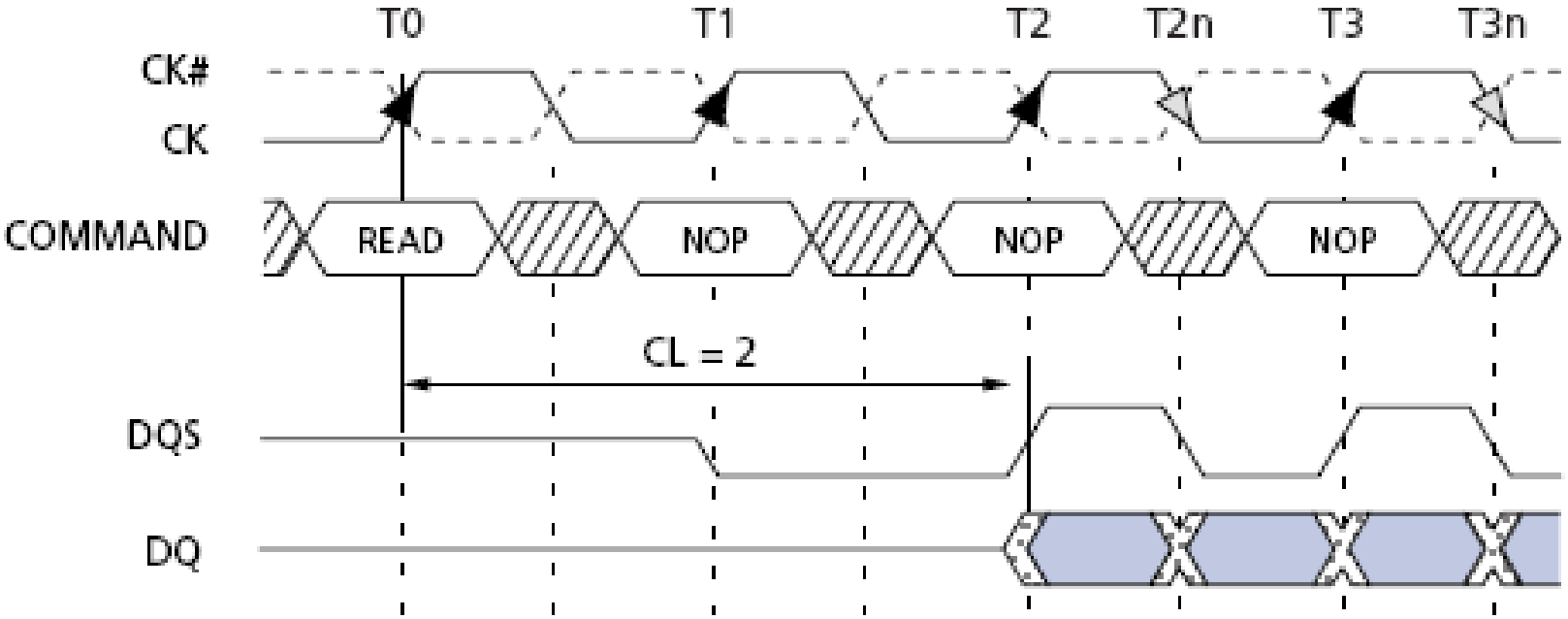
Source attributed to– micron.com

DRAM Module (13), CK and CK#

CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.

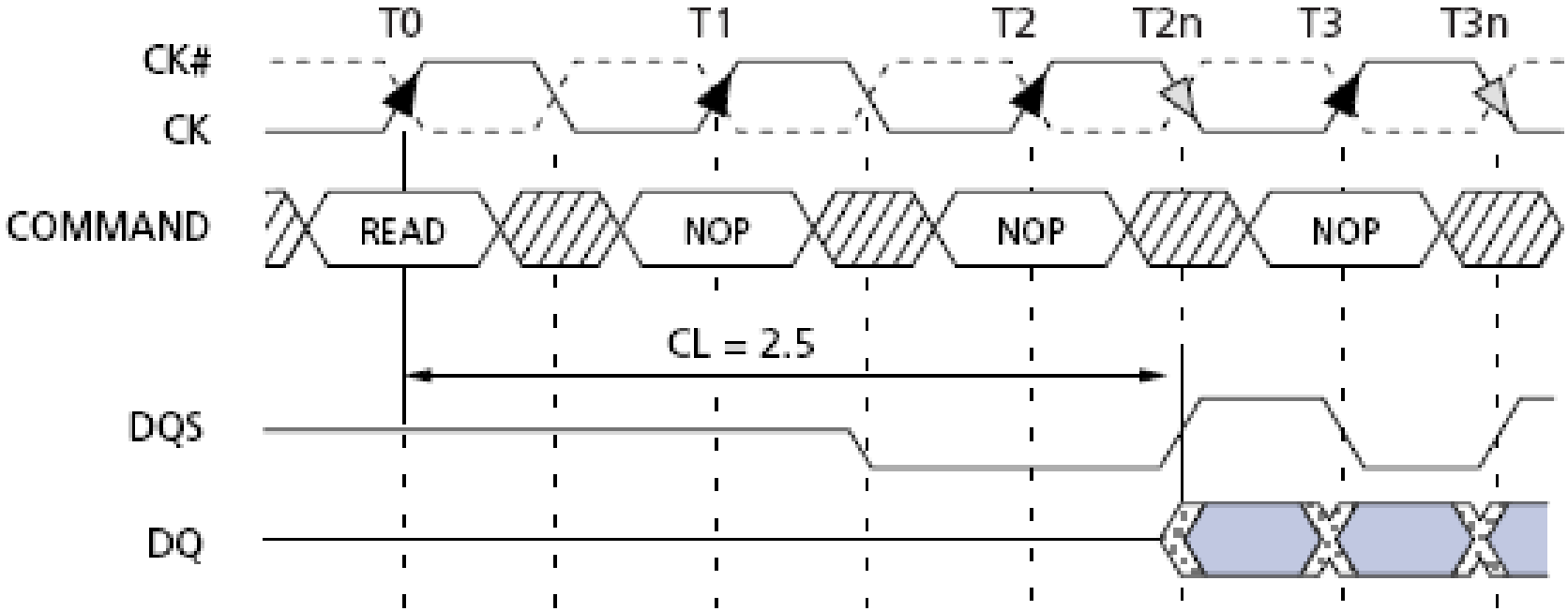
Source attributed to– micron.com

DRAM Module(14) Read CL=2



Source attributed to– micron.com

DRAM Module (15) Read CL =2.5



Source attributed to– micron.com

DRAM Module (16)

DDR2 SDRAM

Features

- RoHS compliant
- V_{DD} = +1.8V ±0.1V, V_{DDQ} = +1.8V ±0.1V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4-bit prefetch architecture
- Duplicate output strobe (RDQS) option for x8
- DLL to align DQ and DQS transitions with CK
- 8 internal banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency – 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Industrial temperature (IT) option
- Supports JEDEC clock jitter specification

Source attributed to– micron.com

DRAM Module (17)

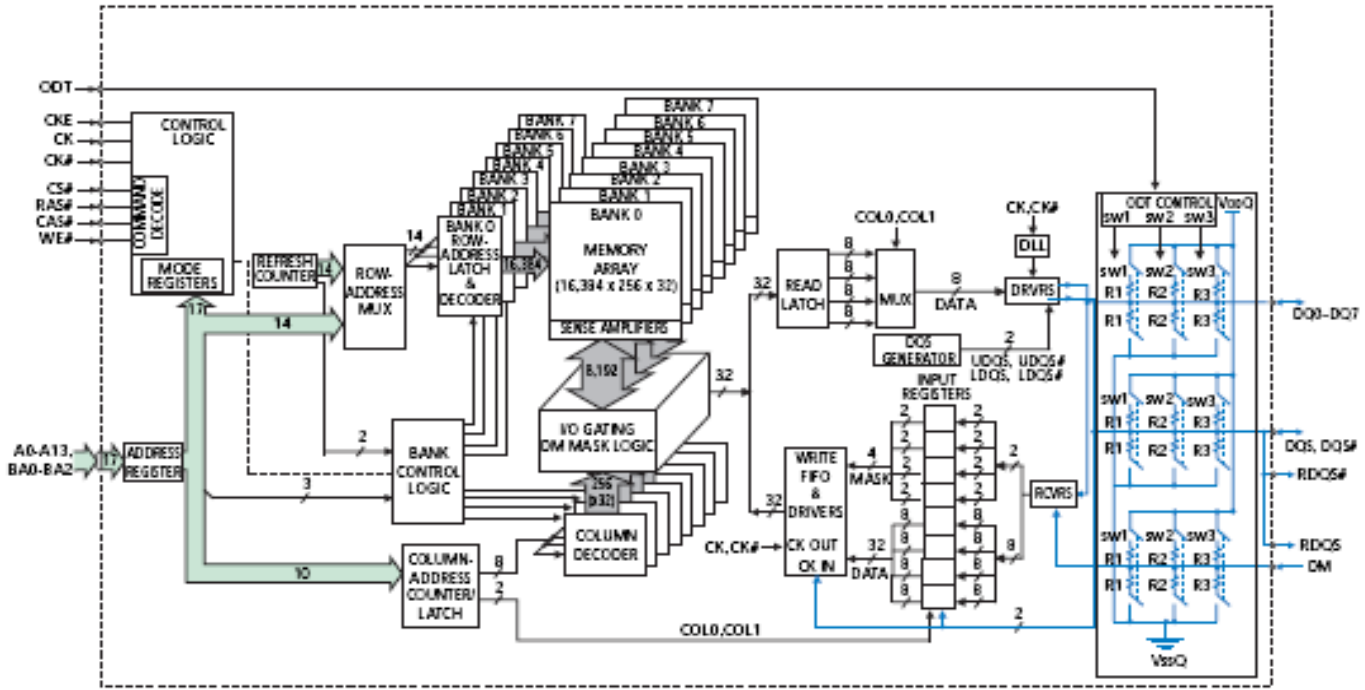
DDR2 Timing

- Timing – cycle time
  5.0ns @ CL = 3 (DDR2-400)
  3.75ns @ CL = 4 (DDR2-533)
  3.0ns @ CL = 5 (DDR2-667)
  3.0ns @ CL = 4 (DDR2-667)
  2.5ns @ CL = 6 (DDR2-800)
  2.5ns @ CL = 5 (DDR2-800)

Source attributed to– micron.com

DRAM Module(18) DDR2

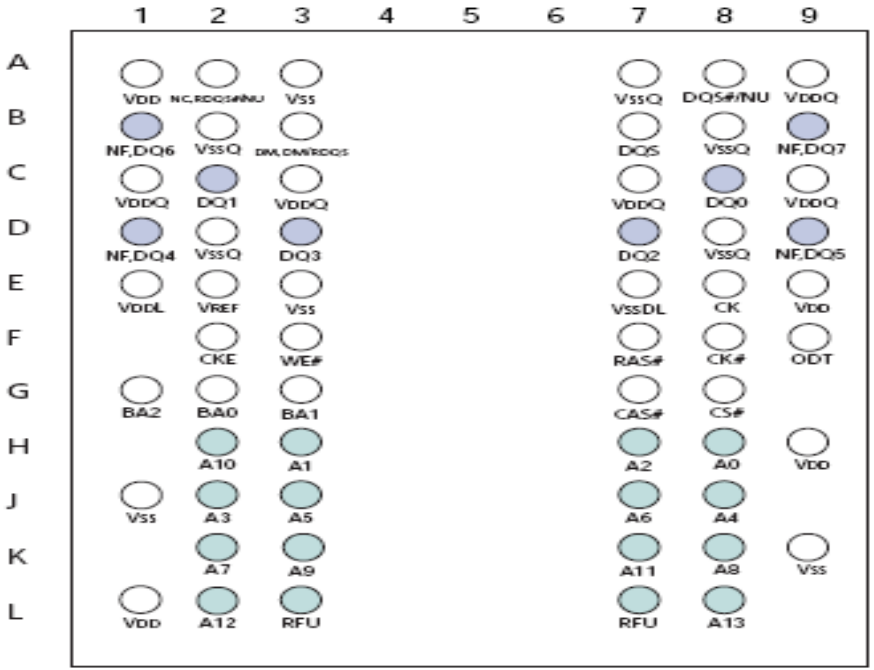
Figure 6: Functional Block Diagram – 128 Meg x 8



Source attributed to– micron.com

DRAM Module (19)

60-Ball FBGA Assignment
Die rev E, HQ marking, top view (8mm x 11.5mm, x4/x8)



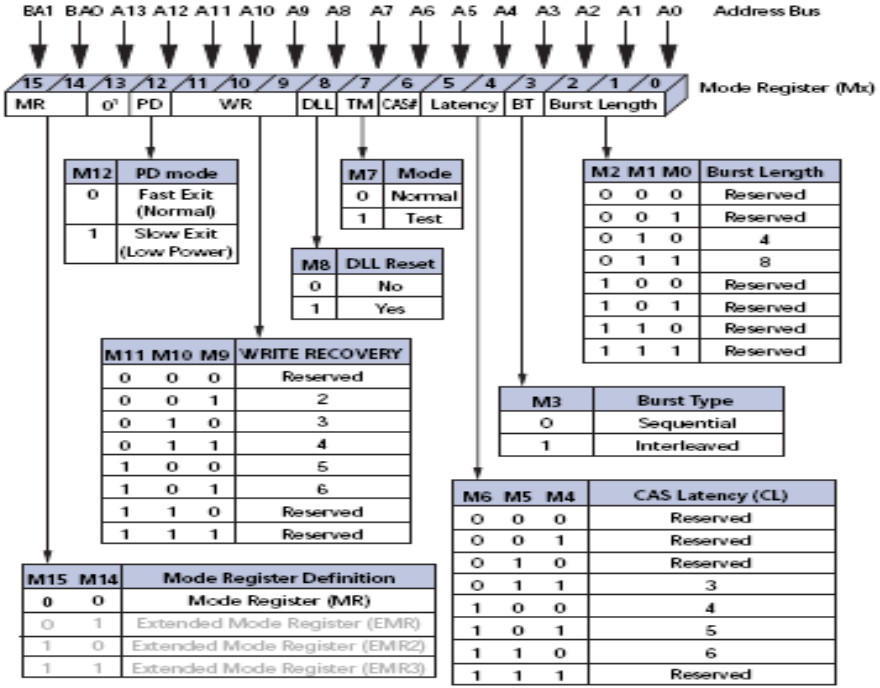
Source attributed to– micron.com

DRAM(20)

Symbol	Type	Description
ODT	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ0–DQ15, LDM, UDM, LDQS, LDQS#, UDQS, and UDQS# for the x16; DQ0–DQ7, DQS, DQS#, RDQS, RDQS#, and DM for the x8; DQ0–DQ3, DQS, DQS#, and DM for the x4. The ODT input will be ignored if disabled via the LOAD MODE command.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides precharge power-down and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry, power-down exit, output disable, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once V_{DD} is applied during first power-up. After V_{REF} has become stable during the power-on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper SELF-REFRESH operation, V_{REF} must be maintained.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple ranks. CS# is considered part of the command code.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered.

Source attributed to– micron.com

DRAM Module(21)



Source attributed to– micron.com

DRAM Module (22)– DDR2 Thermal

Table 19: Thermal Impedance

Die Rev	Package	Substrate	θ JA (°C/W) Airflow = 0m/s	θ JA (°C/W) Airflow = 1m/s	θ JA (°C/W) Airflow = 2m/s	θ JB (°C/W)	θ JC (°C/W)
B[1]	60-ball	2-layer	53.2	40.0	37.2	27.5	2.9
		4-layer	37.4	30.9	27.7	24.2	
	84-ball	2-layer	50.2	36.8	32.1	24.5	3.1
		4-layer	34.9	28.0	25.5	21.3	
C[1]	60-ball	2-layer	56.9	43.6	38.5	30.6	3.8
		4-layer	40.6	34.1	31.3	27.0	
	84-ball	2-layer	56.8	42.8	37.7	24.8	3.9
		4-layer	40.3	33.2	30.4	23.5	
Last shrink target[2]	60-ball	2-layer	60.0	48.0	45.0	32.0	5.0
		4-layer	42.0	36.0	34.0	29.0	
	84-ball	2-layer	59.0	45.0	40.0	27.0	5.2
		4-layer	44.0	35.0	34.0	26.0	

Source attributed to– micron.com

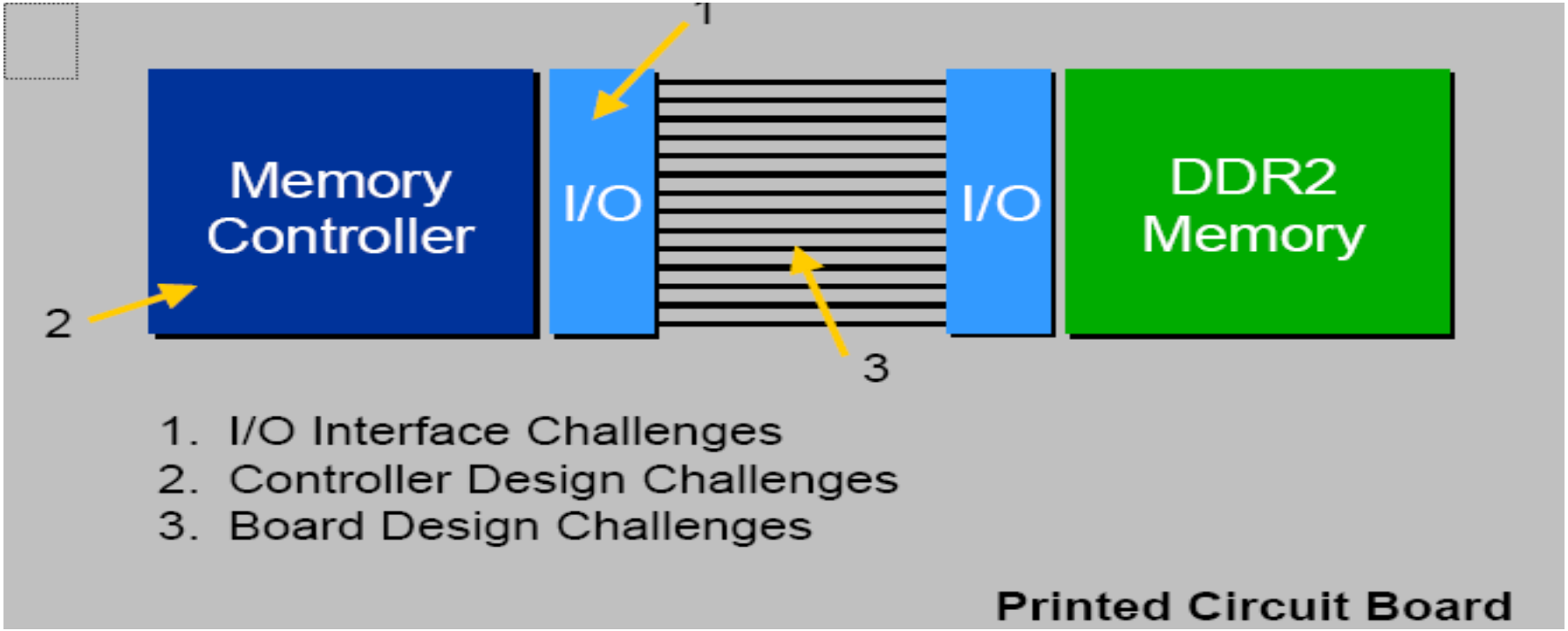
DRAM Module(23) (DDR/DDR2)

DDR -> DDR2

Items	DDR SDRAM	DDR2 SDRAM	Advantages of DDR2
Transfer Rate (Clock Frequency) PreFetch Size Burst Length Data Strobe	200/266/333/400 Mbps (100/133/166/200 MHz) 2-bit 4/8 Single	400/533/667/800 Mbps (200/266/333/400 MHz) 4-bit 2/4/8 Differential	High Speed Operation
Supply Voltage I/O Interface	2.5V (2.6V for DDR 400) SSTL_2	1.8V SSTL_1.8	Power Reduction
Package	TSOP II / FBGA	FBGA	Space Saving
Command Set	-	Same as DDR	Compatibility with DDR
Basic Device Timing	-	Same as DDR	
Other Functions	- - - -	ODT OCD calibration Posted CAS Additive Latency	Bus Utilization & Signal Integrity

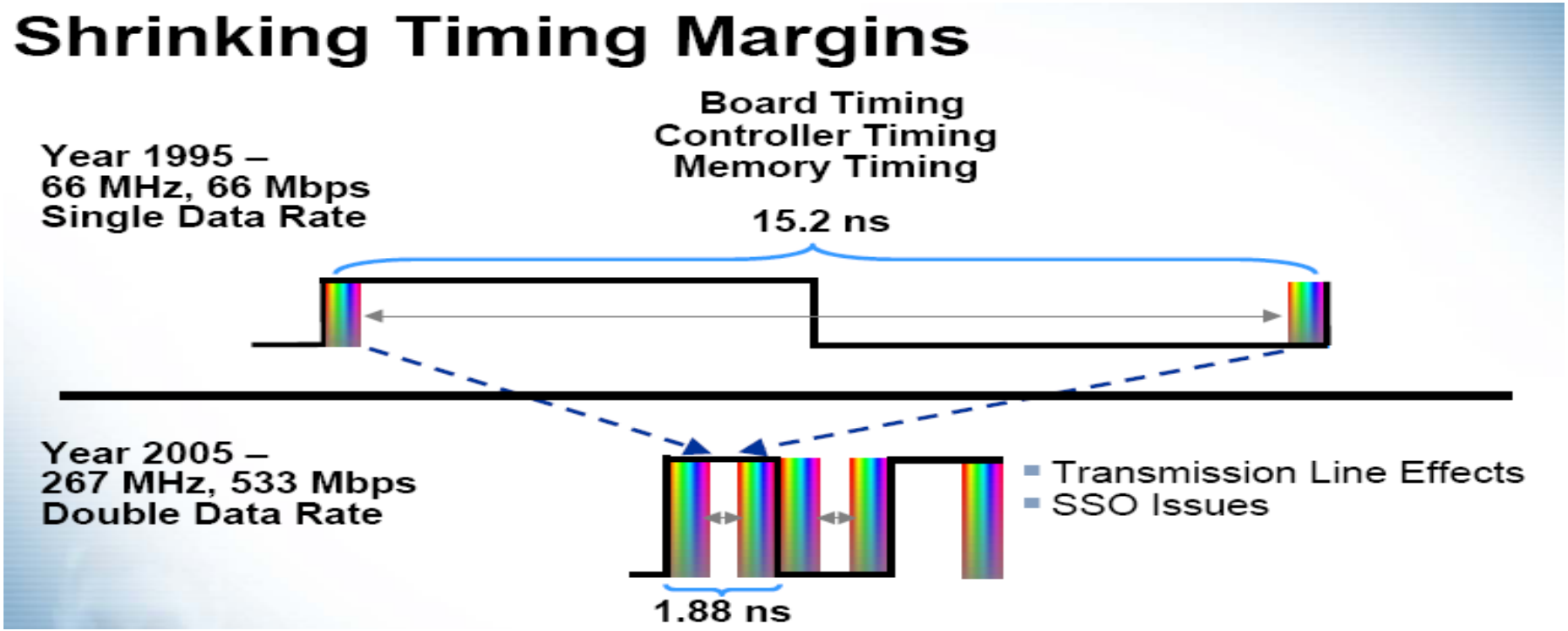
Source attributed to–denali.com

DRAM Module (24): challenges



Source attributed to–denali.com

DRAM Module(25)



Source attributed to–denali.com

DRAM Module(26) – DDR3

Evolution to DDR3

	SDR SDRAM	DDR SDRAM	DDR2	DDR3
Data Rate [Mbps per pin]	PC66, PC100, PC133	DDR200, DDR266, DDR333,	DDR2-400, DDR2-533, DDR2-667 (800?)	DDR3- 800 to DDR3-1600(?)
I/O Organization	x4, x8, x16	x4, x8, x16	x4, x8, x16	x4, x8, x16
VDD = VDDQ / [V]	3.3 (+/- 0.3)	2.5 (+/- 0.2)	1.8 (+/- 0.1)	1.5 (+/-5%)
Interface	LVTTL	SSTL_2	SSTL_18	?
Number of banks	2 / 4	4	4 / 8	8/(?)
Prefetch	1	2	4	8*
Burst Length	1, 2, 4, 8, (page)	2, 4, 8	4, 8	BL8 and BC4
Strobe	No	Single	Single/Differential	Differential
tAC / [ns]	3.0 (tOH) … 5.4	+/- 0.75 (DLL)	DDR-like	DDR-like
DQ driver strength	Wide envelope	Narrow envelope	OCD Calibration	OCD with ZQ Cal
Termination		MoBo	Mobo/ODT	ODT with ZQ Cal
Read Latency Additional Latency	CL=(1), 2, 3 -	CL=(1.5), 2, 2.5, (3) -	CL=(2), 3, 4, 5 AL=0, 1, 2, 3, 4	CL=5,6,7,8,9,10,(11) AL=0,CL-1,CL-2
Write Latency	0	1	RL - 1	5,6,7,8
Data Mask	Yes	Yes	Yes	Yes
Interrupts	Yes	Yes	Wr-Wr, Rd-Rd 4n only	No, BC4 on the fly
DRAM Reset	No	No	No	Yes
Package	TSOP-54	TSOP-66 / BGA	BGA	BGA with Mirroring

Source attributed to–denali.com

DRAM Module(27) – DDR3

Feature/Option	SDRAM	DDR SDRAM	DDR2 SDRAM	DDR3 SDRAM
Density	64Mb – 512Mb	128Mb – 1Gb	256Mb – 4Gb	512Mb – 8Gb
Organization	x4, x8, x16, x32	x4, x8, x16	x4, x8, x16	x4, x8, x16
Data Rate (Mb/s/pin)	100, 133	200, 266, 333, 400	400, 533, 667, 800, 1066	800, 1066, 1333, 1600
VDD / VDDQ	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.1V	1.5V ± 5%
Interface	LVTTL	SSTL_2	SSTL_18	SSTL_15
# Banks	2, 4	4	4, 8	8
Prefetch	1	2	4	8
Burst Length	1, 2, 4, 8, page	2, 4, 8	4, 8	8, 4 with BC
Data Strobe	None	Single ended, Bi-dir.	Single or Diff. RDQS opt.	Differential, Bi-dir. with Write Leveling
DQ Driver Adjust	Wide range	Narrow range	OCD (unused)	ZQ Calibration
Termination	None	Ω on board	Ω on board/ODT	ODT with ZQ, Dynamic ODT
Read DQ Timing	Native tAA	DLL aligns DQ & DQS to CK	DLL aligns DQ, DQS, DQSb, RDQS to CK	DLL aligns DQ, DQS, DQSb to CK
Write DQ Timing	Setup/hold to CK	Setup/hold to DQS	Setup/hold to DQS, DQSb	Setup/hold to DQS, DQSb
CAS Latency (CL)	(1), 2, 3	2, 2.5, 3	(2), 3, 4, 5, 6	5, 6, 7, 8, 9, 10, (11)
Additive Latency (AL)	None	None	0, 1, 2, 3, 4	0, CL-1, CL-2
Read Latency (RL)	CL	CL	CL + AL	CL + AL
Write Latency (WL)	0	1	RL - 1	5, 6, 7, 8
Reset Pin	No	No	No	Yes
Package	TSOP	TSOP/BGA	BGA	BGA with mirroring

Table 1: Feature Comparison of JEDEC SDRAMs

Source: http://www.chipdesignmag.com/print.php?articleId=1446?issueId=0

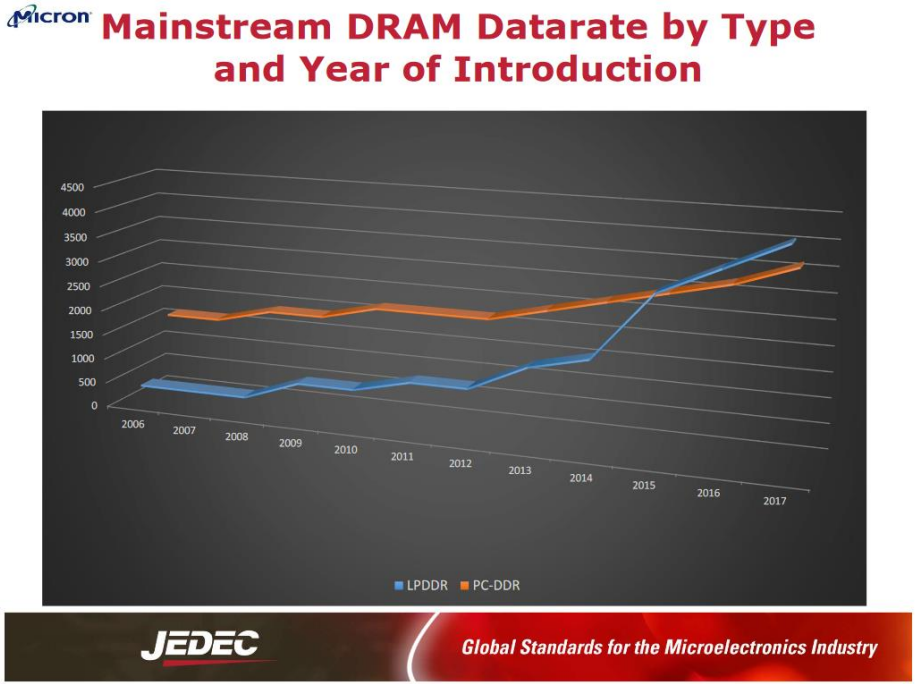
DRAM Module(28) – DDR4

DDR4 vs DDR3

Enhancement	Features	DDR4	DDR3
Performance & Scalability	Transfer Rates	1600MT/s-3200MT/s+	800MT/s-2133MT/s
	Memory Denisty	2Gb-16Gb	512Mb-8Gb
	Internal Banks	16	8
	Bank groups	4	0
	Row Size	0.5K-2K	1K-2K
Power Efficiency	Supply Voltage	1.2V	1.5V
	Signaling Interface	POD with VDDQ termination	SSTL w/ center tapped term.
	Separate VPP Voltage Rail	External VPP supply (2.5V)	On die charge pump
	CAS to Address Latency Mode	Programmable	Fixed
Reliability Accessibility & Serviceability	DRAM Parity	Yes	No
	Register Parity Check	Yes	No
	CRC	Write Only	No
	Mode Register	Read/Write	Write Only
	Boundary Scan	Yes	No

Source:http://http://semiconductorexpert.blogspot.com/2013/10/ddr4-latest-dram-is-here.html

Mobile DRAM(1)



Source:https://www.jedec.org/sites/default/files/Osamu_Nagashima_Mobile_August_2016.pdf

Mobile DRAM(2)

Micron

Evolution of Mainstream DRAM Energy

JEDEC Global Standards for the Microelectronics Industry

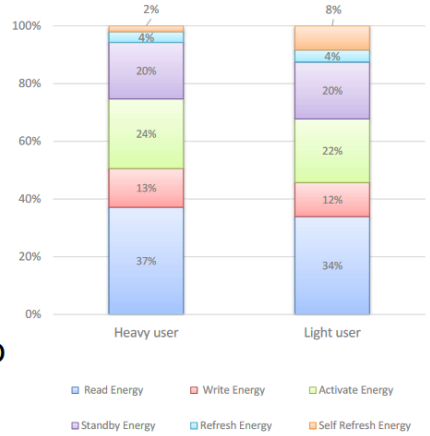
Source:https://www.jedec.org/sites/default/files/Osamu_Nagashima_Mobile_August_2016.pdf

Mobile DRAM(3)

Micron

Typical Mobile Device Usage

- The percentage of active usage has greatly increased in recent years, driving an increase in memory bandwidth
- This has shifted limitations from standby battery life to active battery life and thermal limits



JEDEC Global Standards for the Microelectronics Industry

Source:https://www.jedec.org/sites/default/files/Osamu_Nagashima_Mobile_August_2016.pdf

Mobile DRAM(4)

Micron

Near-Term Future

- This evolution of system limitations is driving future LPDRAM architectures, beginning with the evolution of the LPDDR4 standard
- Responding to the need for lower power, JEDEC is developing a reduced-I/O power version of LPDDR4, called LPDDR4X
- LPDDR4X will reduce the Vddq level from 1.1v to 0.6v
- Signaling swing will remain similar to LPDDR4
  - This allows the same receiver designs and specifications to be used for both LPDDR4 and LPDDR4X

JEDEC Global Standards for the Microelectronics Industry

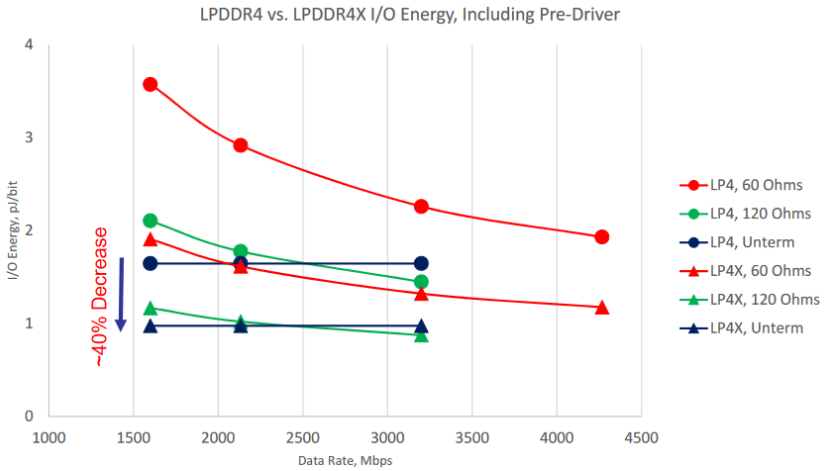
Source:https://www.jedec.org/sites/default/files/Osamu_Nagashima_Mobile_August_2016.pdf

Mobile DRAM(5)

Micron

LPDDR4X: I/O Energy Reduction

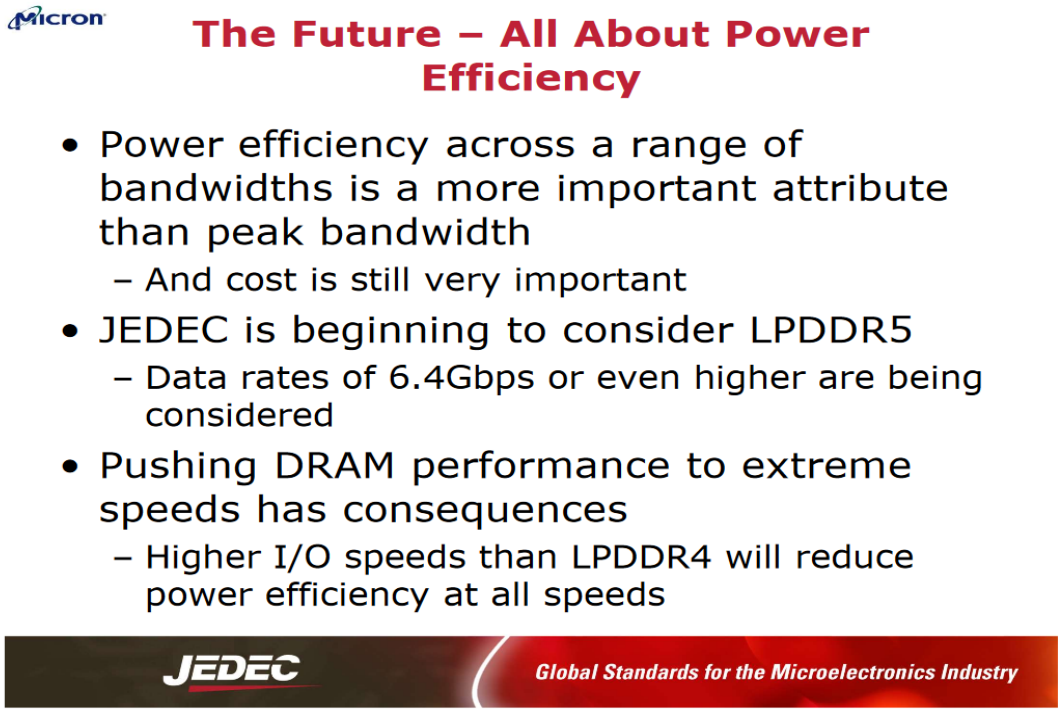
- Reducing Vddq from 1.1v to 0.6v produces about 40% I/O energy savings



JEDEC Global Standards for the Microelectronics Industry

Source:https://www.jedec.org/sites/default/files/Osamu_Nagashima_Mobile_August_2016.pdf

Mobile DRAM(6)



Source:https://www.jedec.org/sites/default/files/Osamu_Nagashima_Mobile_August_2016.pdf

Mobile DRAM(7)

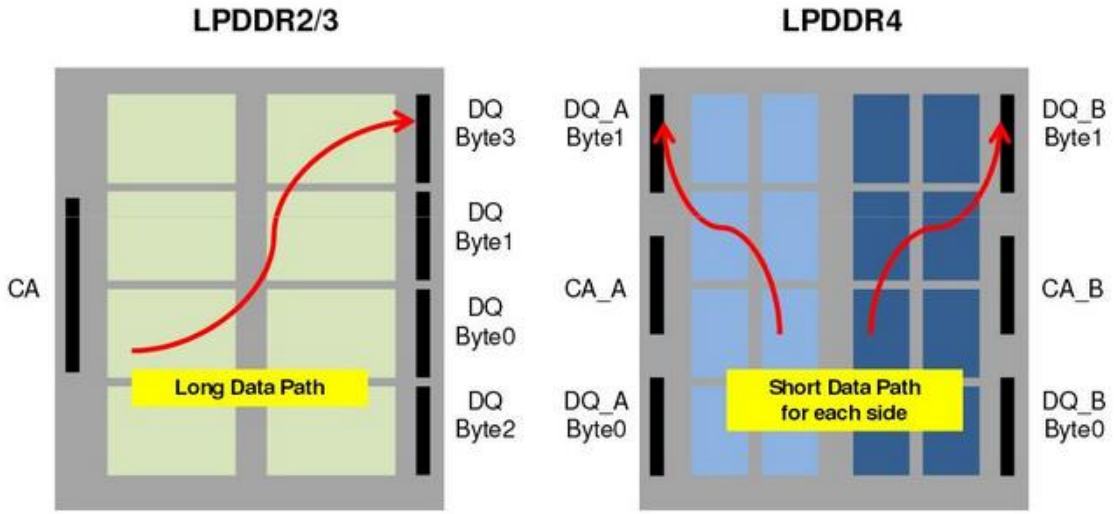
	LPDDR2-S4B	LPDDR3	LPDDR4
Data Rate (per pin)	333~1066 Mbps	800~2133 Mbps	400~3200 Mbps (~4266Mbps)
Density	64 ~ 8Gb	4Gb ~ 32Gb	8Gb ~ 32Gb
Interface	HSUL_12	HSUL_12 w/ optional ODT	LVSTL
Command/Address Bus	DDR	DDR	SDR (Multi cycle command)
Data Bus	DDR	DDR	DDR
Voltage (VDD1/2/CA/Q)	1.8V/1.2V/1.2V/1.2V	1.8V/1.2V/1.2V/1.2V	1.8V/1.1V/1.1V
I/O organization	x16 / x32	x16 / x32	2 ch. x16 (total x32 per die)
Number of Banks	4/8	8	8 / ch. (total 16 banks per die)
Pre-fetch	4	8	16
Burst Length	4/8/16	8	16 / 32 / On the fly
CA ODT	-	-	Supported
DQ ODT	-	Supported (Optional)	Supported
On die ECC	-	-	for future DRAM process (vendor specific / transparent spec)
Package Types	MCP/PoP	MCP/PoP	MCP/PoP

Source:https://www.androidauthority.com/lpddr4-everything-need-know-599759/

Mobile DRAM(8)

Source:https://www.jedec.org/sites/default/files/Osamu_Nagashima_Mobile_August_2016.pdf

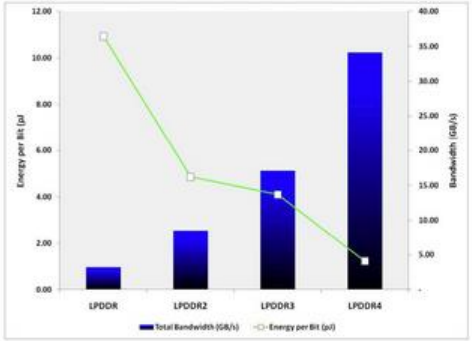
Mobile DRAM(9)



Source:https://www.androidauthority.com/lpddr4-everything-need-know-599759/

Mobile DRAM(10)

- A great user experience requires great power efficiency
  - Tablets – 10 hours active with a 11.5 Ah battery
  - Phones – 8 hours active with a 1.4 Ah battery
- Active and Stand-by power are critical for mobile platforms



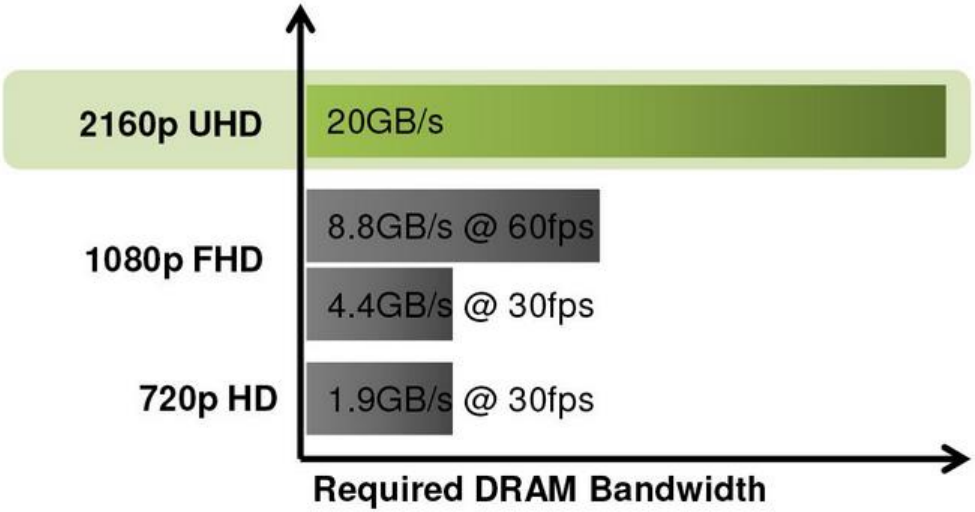
- Phones are targeting 10+ days of standby
- Tablets in “connected standby” targeting 2+ weeks
- Ultrabooks require “always on, always connected” power state, <5% battery drain within 16 hours
- Memory consumes up to 30% of the system power in standby modes

Micron

Low power requirements are essential for mobile and LPDDR4 is the most energy efficient memory yet.

Source:https://www.androidauthority.com/lpddr4-everything-need-know-599759/

Mobile DRAM(11)



Source:https://www.androidauthority.com/lpddr4-everything-need-know-599759/

Closer Look at DDR2/3/4 and LP4

Closer Look at DDR2/3/4 and LP4 (1)

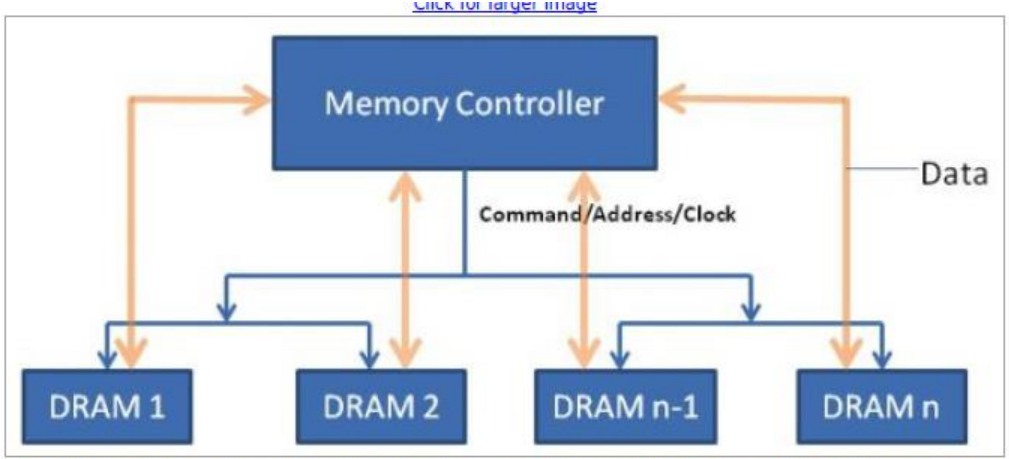


Figure 1. Shows T-topology for connecting memory controller and DDR2 memory modules in which the Command/Address/Clock signals are routed to each memory module in a branched fashion.

SOURCE: https://www.edn.com/design/systems-design/4416627/DDR3--A-comparative-study

Closer Look at DDR2/3/4 and LP4 (1)

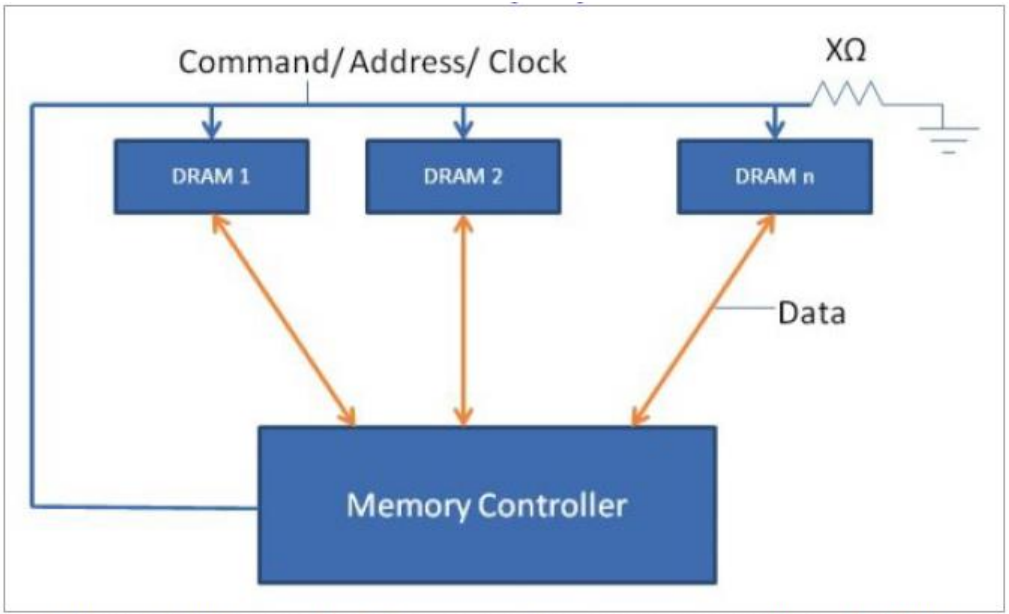


Figure 2. Depicts Fly-by topology for connecting memory controller and DDR3 memory modules in which the memory modules share common Command/Address/Clock lines connected in series.

SOURCE: https://www.edn.com/design/systems-design/4416627/DDR3--A-comparative-study

Closer Look at DDR2/3/4 and LP4 (2)

Fly-By Topology

The higher signaling rates of DDR3 necessitated a new topology for routing the command and control signals to different memory modules. The T- topology, shown in Figure 1, which was adopted for DDR2 couldn't support higher signaling rates and more number of memory modules due to capacitive loading. In a T-topology, the signals are routed to a central node before routing them to individual memory modules, thus limiting the potential variability of trace lengths to shorter paths. But higher signaling rates couldn't be reliably supported over this topology due to multiple stubs and increase in capacitive load seen by the signals when increasing memory capacity.

SOURCE: https://www.edn.com/design/systems-design/4416627/DDR3--A-comparative-study

Closer Look at DDR2/3/4 and LP4 (3)

Write Leveling

Due to the Fly-by topology of DDR3 memories, data and strobes reach different memory modules at different times with respect to command, address and clock signals. To address this situation, DDR3 memories implement leveling techniques, which align the data strobes with clock signal at each memory module interface. Leveling is carried out for each memory module present in a system for each data byte.

Write leveling remedies the skew between data strobes and clock at the memory module boundaries for write data transactions. Before staring the write leveling, the DDR3 memory is placed in the write leveling mode by writing appropriate mode register. After placing the memory in write leveling mode, clock and data strobes are given to the memory module. The memory module samples the clock signal at its boundary with the observed data strobes and the feeds back the sampled value (0/1) on data lines to the driving entity so that it can adjust the delay in the data strobes for next iteration. This process is repeated till a 0 to 1 transition in the feedback value is observed, which indicates the alignment of data strobes with respect to the clock signal at the memory module boundary. The write leveling process is shown in Figure 3 as a waveform diagram.

SOURCE: https://www.edn.com/design/systems-design/4416627/DDR3--A-comparative-study

Closer Look at DDR2/3/4 and LP4 (4)

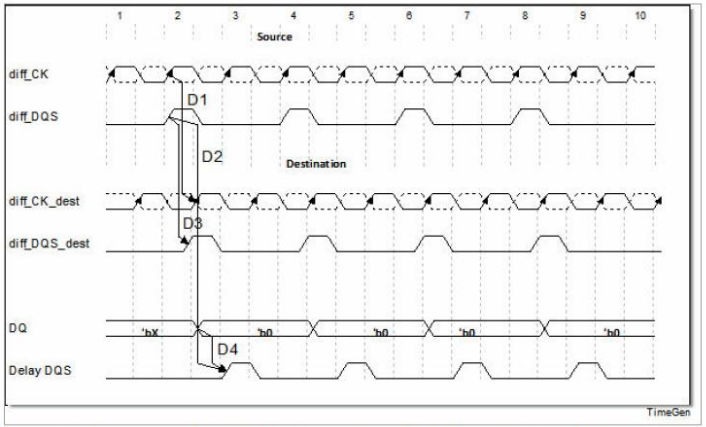


Figure 3. Illustrates the Write Leveling process for adjusting skews at each memory module between data and command/address/clock signals by progressively altering the delay on data strobe line till a 0 to 1 transition in memory clock is sampled at the targeted memory module using the delayed data strobe.

Figure 3 Legend

D1: Delay in the clock observed at the targeted memory module with respect to the clock at the controller end

D2: Delay added to the data strobe at the controller side to observe a 0 to 1 transition in the clock at the targeted memory module

D3: Delay in the data strobe signal observed at the targeted memory module with respect to the data strobe signal at the controller end

D4: Delay between the sampled value of clock at the targeted memory module for previous data strobe adjustment and driving data strobe with new adjustment value

SOURCE: https://www.edn.com/design/systems-design/4416627/DDR3--A-comparative-study

Closer Look at DDR2/3/4 and LP4 (5)

Read Leveling

Read leveling addresses the skew between data and strobes for read data transactions. To support this feature, DDR3 memories incorporate a Multi Purpose Register (MPR) which contains a pre-defined data pattern which, when selected, is output on the data lines, instead of normal data from the memory array. Before starting the read leveling sequence, the MPR data is selected as output by programming appropriate mode register. Thereafter read leveling is initiated by giving READ command to the memory module and trying to capture the pre-defined data by optimally adjusting the internal delays on data strobes. This process is repeated till the internal delays on the data strobes are adjusted to create a proper window for best capture the pre-defined data pattern. The read leveling process is shown as a waveform diagram in Figure 5 and the provision for selecting the Multi Purpose Register (MPR) for read leveling process is depicted by Figure 4.

SOURCE: https://www.edn.com/design/systems-design/4416627/DDR3--A-comparative-study

Closer Look at DDR2/3/4 and LP4 (6)

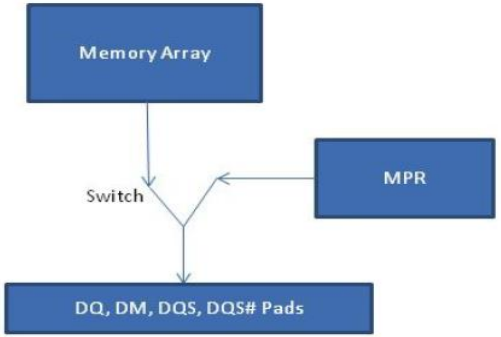


Figure 4. Shows the selectability of Multi-Purpose Register (MPR) for Read Leveling process

Click for larger image

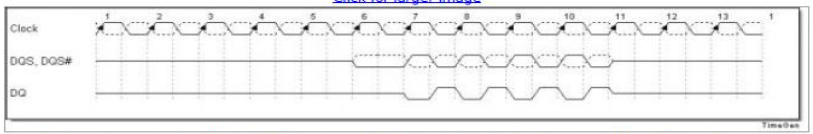


Figure 5. Gives a snapshot of memory interface signals during Read Leveling process

Both Write and Read leveling are relevant for DDR3 memories only. DDR2 memories don't have any such provisions.

SOURCE: https://www.edn.com/design/systems-design/4416627/DDR3--A-comparative-study

Closer Look at DDR2/3/4 and LP4 (7)

ZQ Calibration

To improve signal integrity and boost the output signals DDR memories come with termination resistances and output drivers. Periodic calibration of these termination resistances and output drivers are necessary for maintaining signal integrity across temperature and voltage variations. While uncalibrated termination resistances directly affect the signal quality, improperly adjusted output drivers shift the valid signal transitions from reference level; thus causing skew between data and strobe signals. As shown in Figure 6, this skew reduces the effective valid data window and decreases the reliability of data transfers.

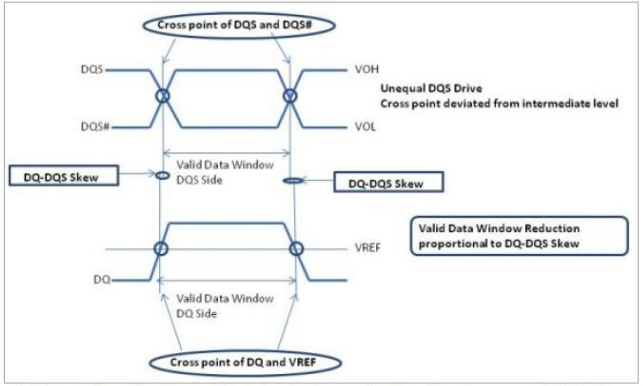


Figure 6. Shows the effective valid data window reduction due to unequal DQS drive which shifts the crossover point from the intermediate level

The output drivers of DDR2 memories are generally present off-chip. These off-chip drivers are optionally calibrated only once during initialization. This calibration sequence, known as Off-Chip Driver calibration, only calibrates the output driver present off-chip. On-die termination calibration doesn't happen for DDR2 memories.

In order to maintain high signal integrity, DDR3 memories incorporate on-die terminations (ODT) and on-chip output drivers. A dedicated pad, known as ZQ pad, is present in the DDR3 memories which facilitates the calibration process through a 240 ohm ± 1% tolerance external resistor between the ZQ pin and ground acting as reference. The calibration sequence is initiated by the on-die calibration engine when the memory module receives a ZQ calibration command. Initial ZQ calibration is done during initialization and short ZQ calibrations are done periodically to compensate variations in operating temperature and voltage drifts.

SOURCE: https://www.edn.com/design/systems-design/4416627/DDR3--A-comparative-study

Closer Look at DDR2/3/4 and LP4 (8)

Dynamic On-Die Termination

DDR3 memories offer a new feature where the on-die termination resistance can be changed without mode register programming in order to improve the signal integrity on the data bus. When this feature is enabled a different value of termination resistance is applied for write data transactions to the memory. Figure 7 represents an abstract arrangement implemented in DDR3 memories which dynamically switches the termination resistance, when enabled, for write transactions; thus eliminating the need of issuing mode register programming command in such cases.

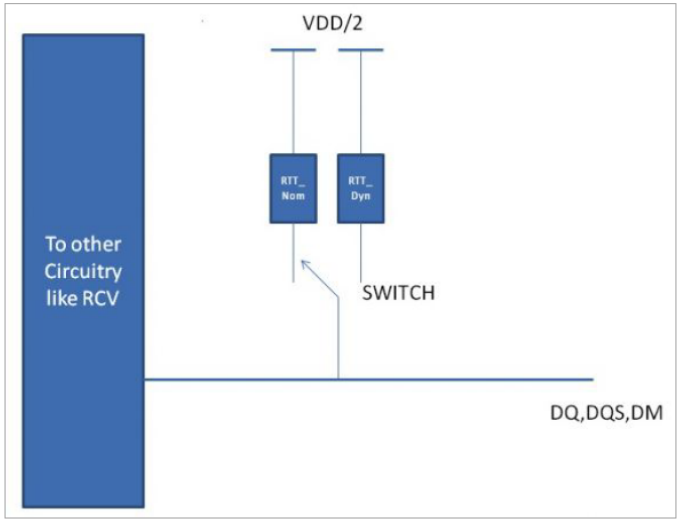


Figure 7. Depicts the Dynamic ODT configuration present in DDR3 memory modules which when enabled, changes the termination resistance to "RTT_Dyn" for write data transactions and reverts it back to "RTT_Nom" at the end of the transaction

SOURCE: https://www.edn.com/design/systems-design/4416627/DDR3--A-comparative-study

Closer Look at DDR2/3/4 and LP4 (9)

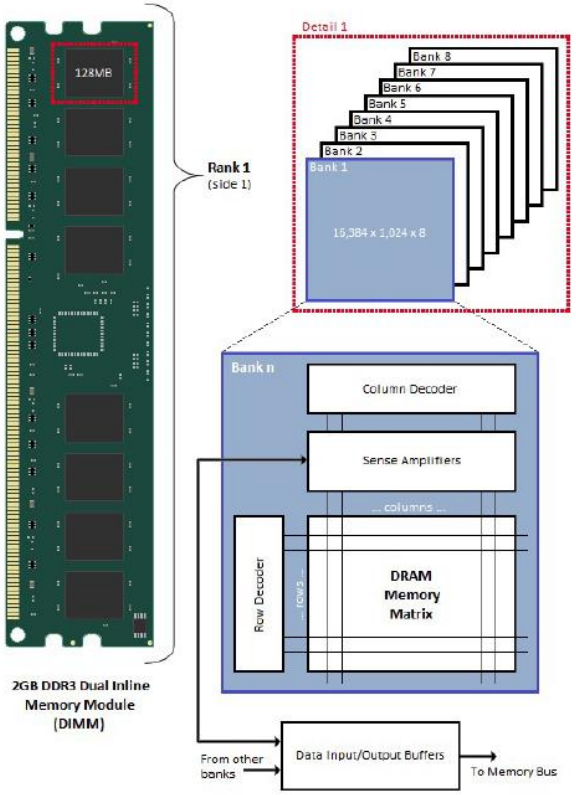


Figure 1. Typical functional arrangement of SDRAM memory space. One Bank only is shown for clarity

SOURCE: https://www.anandtech.com/show/3851/everything-you-always-wanted-to-know-about-sdram-memory-but-were-afraid-to-ask/2

Closer Look at DDR2/3/4 and LP4 (10)

DDR4 – Advantages of Migrating from DDR3

Feature/Option	DDR3	DDR4	DDR4 Advantage
Voltage (core and I/O)	1.5V	1.2V	Reduces memory power demand
V_{REF} inputs	2 – DQs and CMD/ADDR	1 – CMD/ADDR	V_{REFDQ} now internal
Low voltage standard	Yes (DDR3L at 1.35V)	No	Memory power reductions
Data rate (Mb/s)	800, 1066, 1333, 1600, 1866, 2133	1600, 1866, 2133, 2400, 2666, 3200	Migration to higher-speed I/O
Densities	512Mb–8Gb	2Gb–16Gb	Better enablement for large-capacity memory subsystems
Internal banks	8	16	More banks
Bank groups (BG)	0	4	Faster burst accesses
^{t}CK – DLL enabled	300 MHz to 800 MHz	667 MHz to 1.6 GHz	Higher data rates
^{t}CK – DLL disabled	10 MHz to 125 MHz (optional)	Undefined to 125 MHz	DLL-off now fully supported
Read latency	AL + CL	AL + CL	Expanded values
Write latency	AL + CWL	AL + CWL	Expanded values
DQ driver (ALT)	40Ω	48Ω	Optimized for PtP (point-to-point) applications
DQ bus	SSTL15	POD12	Mitigate I/O noise and power
R_{TT} values (in Ω)	120, 60, 40, 30, 20	240, 120, 80, 60, 48, 40, 34	Support higher data rates
R_{TT} not allowed	READ bursts	Disables during READ bursts	Ease-of-use
ODT modes	Nominal, dynamic	Nominal, dynamic, park	Additional control mode; supports OTF value change
ODT control	ODT signaling required	ODT signaling not required	Ease of ODT control, allows non-ODT routing on PtP applications
Multipurpose register (MPR)	Four registers – 1 defined, 3 RFU	Four registers – 3 defined, 1 RFU	Provides additional specialty readout

SOURCE: https://www.micron.com/products/dram/ddr3-to-ddr4

Closer Look at DDR2/3/4 and LP4 (11)

- **Evolutionary DRAM technology enables 3.2Gbps and faster**

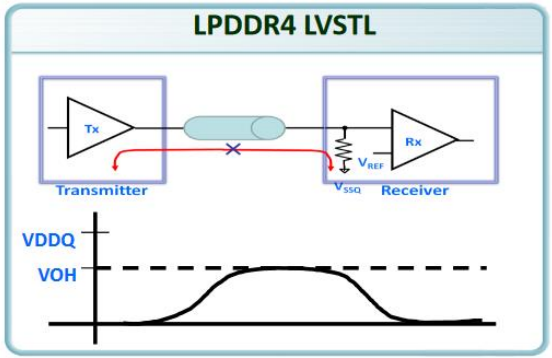
Items		LPDDR3	LPDDR4	Comments
Speed	CLK	400-800MHz (~1066MHz w/ LP3E)	800-1600MHz	2X, Pursues higher speed
	CMD/ADDR	DDR	SDR	-
	DQ	DDR	DDR	
	Band Width	12.8GB/s+ (2ch)	25.6GB/s+ (2ch)	2X
Voltage	VDD2/VDDQ/VDD1	1.2/1.2/1.8	1.1/1.1/1.8	Total Pd 10%↓
Architecture	[# o Ch & DQs]/ Die	x32	2x16	IDD4 20% ↓
	# of Bank/channel	8	8	-
	Page Size	4K	2K	IDD0 10%↓
	BL	8	16	32B/ch
Interface	I/O interface	HSUL	LVSTL	40% I/O power reduction (vs. POD)
	DQ ODT	No term (VDDQterm option)	VSSQ Term	
	CA ODT	No term	VSS term	Optional
	Vref	External	Internal	

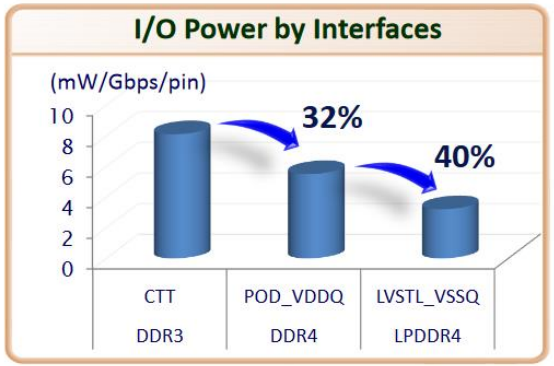
SOURCE: http://www.memcon.com/pdfs/proceedings2013/track1/LPDDR4_Evolution_for_a_New_Mobile_World.pdf

Closer Look at DDR2/3/4 and LP4 (11)

Innovative Low Power Interface - LVSTL

- LVSTL (Low Voltage Swing Terminated Logic)
  - High frequency operation with less IO power consumption
  - No DC power consumption when driving "low"
  - Lower Cio, small Xtalk and SSN, because of small swing
  - Stronger reference plane
  - Easy voltage scaling





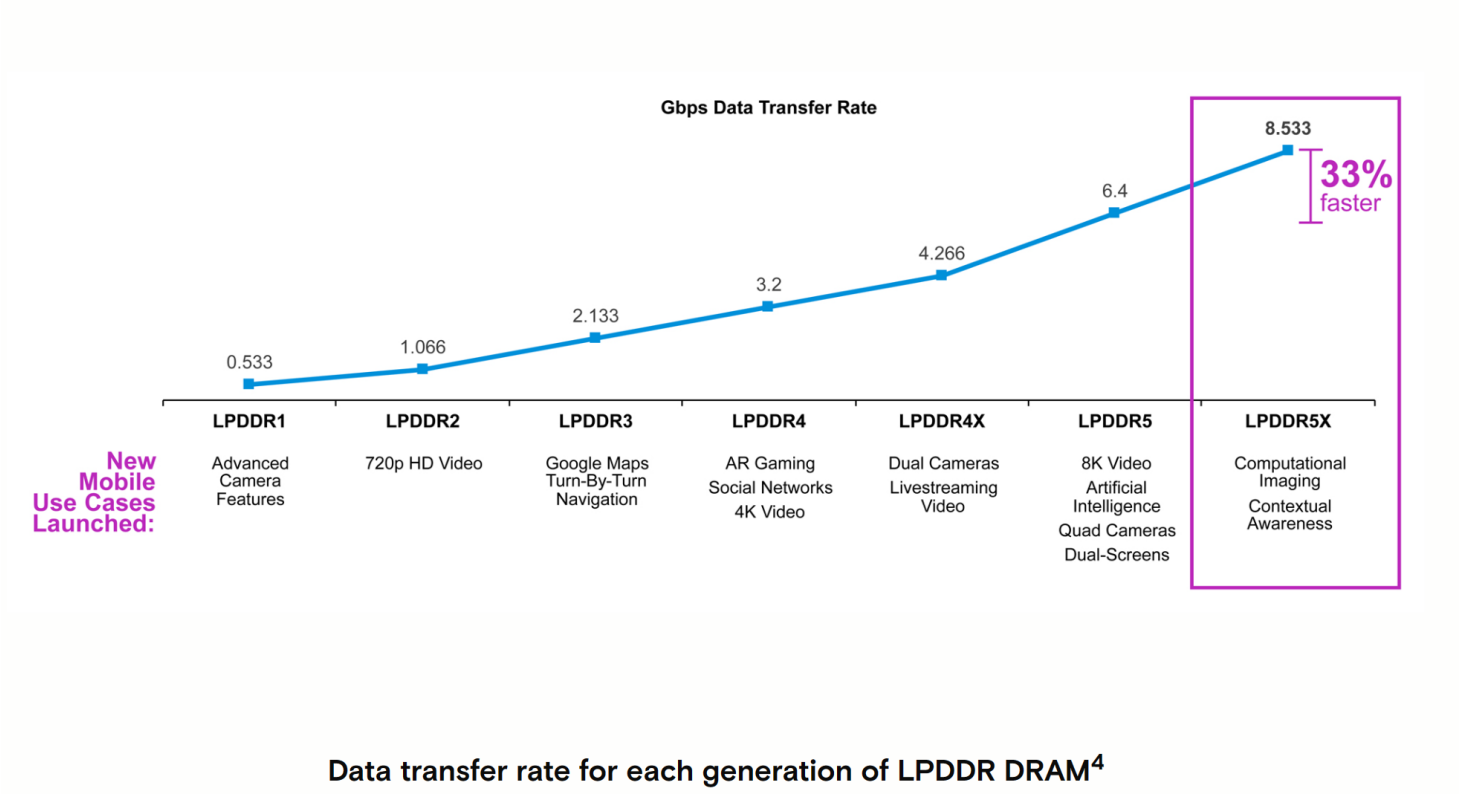
SOURCE: http://www.memcon.com/pdfs/proceedings2013/track1/LPDDR4_Evolution_for_a_New_Mobile_World.pdf

DDR Comparison

	DRAM	DDR	DDR2	DDR3	DDR4	DDR5
Prefetch	1 – Bit	2 - Bit	4 - Bit	8 - Bit	Bit per Bank	16 - Bit
Data Rate (MT/s)	100 - 166	266 - 400	533 - 800	1066 - 1600	2133 - 5100	3200 - 6400
Transfer Rate (GB/s)	0.8 - 1.3	2.1 - 3.2	4.2 - 6.4	8.5 - 14.9	17 - 25.6	38.4 - 51.2
Voltage (V)	3.3	2.5 - 2.6	1.8	1.35 - 1.5	1.2	1.1

Source: https://www.crucial.com/articles/about-memory/difference-among-ddr2-ddr3-ddr4-and-ddr5-memory#

LPDDR Data Rate



Data transfer rate for each generation of LPDDR DRAM[4]

SOURCE: micron.com