A-41 13/07/2020 1 G. H. Raigoni Callege of Engineering Nagpure 2020-2021 CODD Team CAF-1 Examination for Split-II Course Winter-2020 (online mode) Deportment: - Electronics Engineering?.

Semester Section: - VIII m / A

Date of Examination: - 13107/2020 Rall No * :- 41 Design Name: - Himangshy Didip Grabhane Begistration No *: - 2017 AETX 1117103 60.1 1 4 Define DML: Low Moise Morgin & NMH: High NML in defined as the difference in magnifude between the mostimum LOW output voilty of the driving got and the maximum input LOW valtage recognized by the driven got. Thus NM. (Noise Margin low) = Vil-Vail NMH (Noise Margioligh):magnitude between the minimum HIHGE Output vollage of the driving

gate and the minimum input HIGH valtage orecognized by the receiving gate. Thus, 601 If I Drow NAND Gak by using Pull up and Pull down Networks with propos truth Pullo Pull Famo Metrone Combined COPOR Mehoork

COJ Reladionship between vallaged for the three regions operation of a choos Investor. Noos all pmos lin Pmos Prossal Nin Proof lin 10 mos sat pmos. P mas sal 2 proof in 6 was off 2 3 4 5

DFF: V. GateToxouroce < V. Threehold
Linears (Ox OHMTC): O < V. Drain To Louroce < V. Garato Sauro
V. Threshold

Saturation: O < V_Galeto Source-V_Threshold < V_Drain to Source

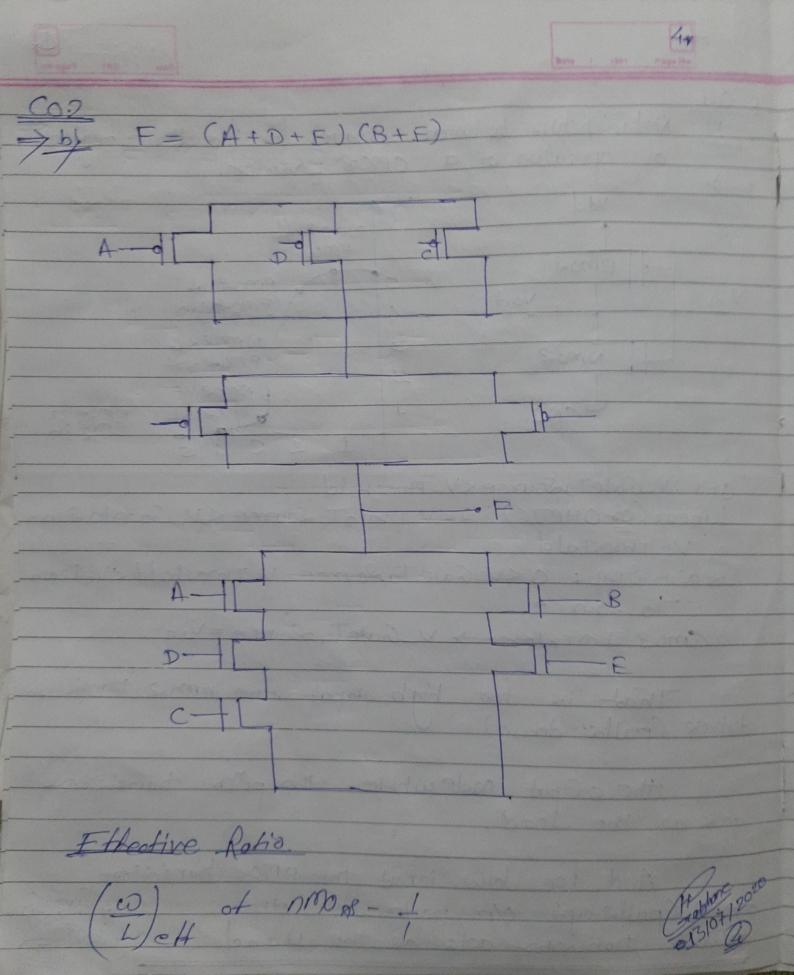
cmas Inventor -> V_GateTa, Source = Vin

drives (palla docon) by hopet the nonce toonich

ack as the load, the phose translator

And for low input the pmos bonsistor drives (pulls up) o/p node with the nmos bonsistor acts as the word

Habbar 12020



7 F=((A+B)(D)' i.e., F = ((A+B).C.D)