Gate Keeper System — Coherent Control, Energy Balancing, and Grounding for Parallel Fiber Computation

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This design document defines the Gate Keeper subsystem that stabilizes a massively parallel fiber/photonic computer. The Gate Keeper maintains phase coherence across channels, balances optical energy, and provides a controlled ground path to dissipate surges so computation can continue without destructive interference or repeated restarts.

# 1. Role of the Gate Keeper

The Gate Keeper is the active control layer between the fiber field (coin-sorter lanes) and the interference logic core. Its mission is threefold: (A) keep all channels phase-aligned for coherent combining, (B) regulate per-lane optical energy so no single lane dominates, and (C) provide a safe ‘ground’ output that dissipates excess energy before it corrupts computations.

# 2. Functional Blocks

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| Block | Function | Typical Implementation |
| Phase Lock Unit (PLU) | Measure phase error and apply corrections per channel. | Pilot tone + photodiode taps + LiNbO₃/SiN phase shifters (PID loop). |
| Amplitude Control Unit (ACU) | Keep optical power balanced; boost or attenuate per lane. | Variable Optical Attenuators (VOAs), Semiconductor Optical Amplifiers (SOAs), EDFAs (with limits). |
| Coherent Combiner | Combine fields (not just intensities) for constructive/destructive interference. | Mach–Zehnder interferometers (MZIs), star couplers. |
| Surge Ground Path (SGP) | Divert excess energy to ground to prevent flow disruption. | High-speed optical dump: MZI-to-dump port, optical isolators, absorber terminations. |
| Health Monitor & Memory | Timestamped logs of ‘solved’ vs ‘error’ results; triggers recalibration. | FPGA/MCU with NVM; majority-vote across replicas. |

# 3. Control Logic — Increase, Hold, or Ground

The Gate Keeper runs a fast feedback loop that decides whether to increase lane energy, hold steady, or ground excess. This loop executes per lane and at the combiner level.

* Decision loop (per lane):
* 1) Sense: Measure phase φ\_i, amplitude A\_i, and coherence metric C\_i (visibility at the combiner).
* 2) Compare: Compute errors e\_φ = φ\_target − φ\_i and e\_A = A\_target − A\_i.
* 3) Act: If A\_i < A\_min and C\_i ≥ C\_min → increase (SOA/EDFA). If A\_i > A\_max or C\_i < C\_min → attenuate or route to ground-dump.

# 4. Text Diagram — Coherent Combine with Ground

[Fiber Lanes] → (PLU) → (ACU) → ┌───────────────┐  
 → │ Coherent │ → [Output Detectors]  
[Fiber Lanes] → (PLU) → (ACU) → │ Combiner (MZI)│  
 → └─────┬─────────┘  
 │  
 [Ground Dump]

In the combiner, any excess or mis-phased energy is steered to the dump port (optical absorber/isolator) to protect the main output from corruption.

# 5. Ground Path Design

* Objectives:
* • Divert excess optical energy in <10 ns to avoid corrupting a compute window.
* • Prevent back-reflections: include optical isolators before the absorber.
* • Convert stray energy to heat safely: use blackened, high-thermal-capacity terminations.
* Implementation options:
* • Fast ‘dump’ arm in each MZI with RF-controlled phase shifter (π shift routes to dump).
* • Dedicated star-coupler port tied to an absorber with an isolator.
* • Overflow detector that trips a fast VOAs-to-zero command on lanes exceeding thresholds.

# 6. Stability Math (Conceptual)

Let E\_i(t) be the complex field in lane i. The Gate Keeper regulates:  
• Phase: minimize J\_φ = Σ\_i |∠E\_i − φ\_target|^2  
• Amplitude: minimize J\_A = Σ\_i | |E\_i| − A\_target |^2  
• Coherence: maximize visibility V = (I\_max − I\_min)/(I\_max + I\_min) at the combiner.  
Control law (concept): Δφ\_i = k\_φ·e\_φ, ΔA\_i = k\_A·e\_A with anti-windup and saturation handling.

# 7. Safety & Energy Policy

* • Upper energy cap per lane: A\_max; trip to ground if exceeded.
* • Global cap: Σ\_i A\_i ≤ A\_total\_max; engage staged dumps to maintain headroom.
* • Watchdog: if coherence V < V\_min across N frames → auto-recalibrate PLU and write ‘error’ with timestamp.
* • Memory policy: store ‘solved/error’ events; on repeated errors suggest missing-input diagnostics to the user.

# 8. MVP Test Plan

* 1) Four-lane demo with a single MZI combiner; add a dump port and VOAs per lane.
* 2) Inject pilot tones; measure phase noise; close the PLL; log visibility V vs time.
* 3) Sweep input power; show Gate Keeper boosting weak lanes, dumping surges, and maintaining BER.
* 4) Scale to 64 lanes; demonstrate majority-vote decoding without restarts.

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