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Mathematics and Computers in Simulation 91 (2013) 249–261

MATHEMATICS AND COMPUTERS IN SIMULATION

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Original article

FPGA-based sliding mode direct control of single phase PWM boost rectifier

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Received 6 March 2012; received in revised form 22 April 2012; accepted 3 May 2012
Available online 7 June 2012

Abstract

In this paper, a Field Programmable Gate Array (FPGA) based controller for single phase PWM boost rectifier is presented. The control is made up of an internal current control loop and external DC-link voltage control loop. The internal control loop allows active shaping of the line current and is synthesized via sliding mode theory. The external control loop is based on a PI controller and allows imposing the shape of the DC-link voltage response. Experimental results carried out on a FPGA-based prototyping platform are presented and discussed in order to illustrate the efficiency of the developed FPGA-based controller.

Keywords: PWM boost rectifier; FPGA; Sliding mode control

1. Introduction

Industrial applications like adjustable speed drives (ASD) require providing DC-link voltage. In general, diode rectifiers are used to this purpose since they present a simple, low cost and robust solution. However, the use of diode rectifiers with the rapid growth of ASD applications exacerbates the problems related to the harmonic pollution of power systems [7]. On the other hand, they are characterized by large distortion in line currents and poor power factor. To cope with these problems, various power factor correction techniques based on active wave shaping of the line current have been proposed [13]. A part from using active filtering solutions, the best solution consists in using PWM rectifiers. Their main advantages [2,1,4,10,6] are:

- Low distortion and harmonic contents of grid line currents.
- Possibility of working at unit power factor.
- Control of the DC link voltage level despite of grid voltage fluctuations.

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0378-4754/$36.00
http://dx.doi.org/10.1016/j.matcom.2012.05.001

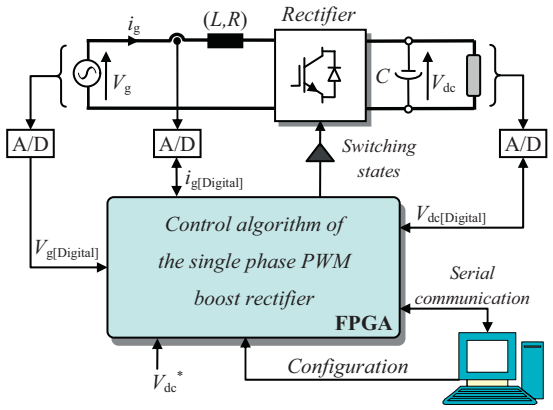

Fig. 1. Single phase PWM boost rectifier control system.

Although PWM rectifiers are more expensive than diode rectifiers, it is expected that their application will increase since reduction of current harmonics is actually strictly enforced.

Nowadays, most of digital control algorithms are implemented based on microcontrollers and Digital Signal Processors (DSPs) solutions. These solutions include dedicated peripherals for controlling electrical systems such as analog-to-digital converters (ADCs), arithmetic logic units, PWM modules. Nevertheless, they are still limited for complex control algorithms and are characterized by a feedback loop delay. In this context, FPGA-based solutions can also be considered as an appropriate solution for the digital implementation of control algorithms [8]. They were used with success for the control of electrical system applications such as control of electrical machines [16,14], wind turbine generators [3]. Moreover, the use of FPGAs allows the design of a dedicated hardware architecture for a given control algorithm with free sampling positions and multi-sampling periods [15,11,5].

So, having in mind to show the efficiency of FPGA solutions, this paper presents the FPGA implementation of a sliding mode control of a single phase PWM boost rectifier. The sliding mode theory is generally associated with variable structure systems such as static converters. The use of this type of control was limited by oscillations caused by sliding effects and limitations on the commutation frequency of power switches. Following advances and performance improvement of electronic power components, the sliding mode control has become more and more effective for electrical systems applications. In this work, the sliding mode theory was used to synthesize the internal current control loop of the single phase PWM boost rectifier. And the external one based on PI controller ensures the control of the DC link voltage. The synthesized control algorithm was experimentally tested on the FPGA-based prototyping platform presented in Fig. 1. Dedicated hardware architecture was designed for the FPGA implementation of the control. The obtained execution time delay, between the sampling of measured current and voltages, and the application of switching states to the converter is only of few microseconds.

This paper is organized as follows. Firstly, the modeling of a single phase PWM boost rectifier is presented in Section 2. Then, in Section 3 the control of a single phase PWM boost rectifier based on sliding mode theory is presented. After that, the FPGA implementation of the considered control algorithm is discussed in Section 4. Finally, experimental results are presented in Section 5 in order to show the effectiveness of the implemented control architecture.

2. Modeling of single phase PWM boost rectifier

Fig. 2 shows the principle of a controlled single phase PWM boost rectifier.

In Fig. 2, u is the switching control signal of the converter, V_{dc} is the capacitor voltage, V_g is the grid voltage, i_g is the grid current, V_{conv} is the converter voltage, i_{conv} is the converter current, i_{dc} the output current of the PWM rectifier, i_c the capacitor current and i_{Load} is the load current.

Based on Fig. 2, we can obtain the following equation

$$V_{conv} = V_g - L\frac{di_g}{dt} - Ri_g \tag{1}$$

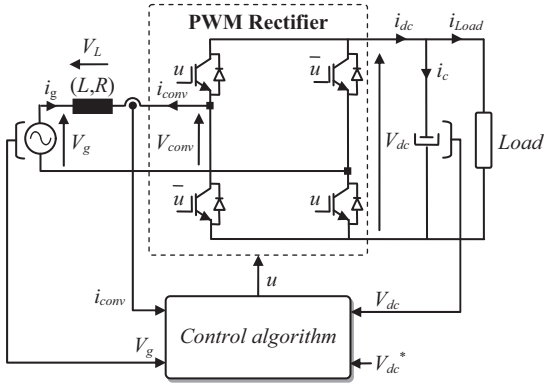

Fig. 2. Controlled single phase PWM boost rectifier.

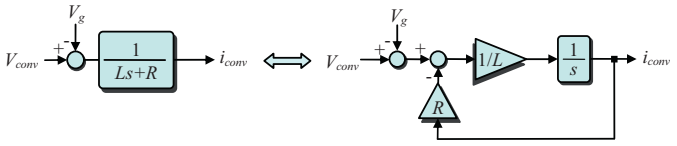

Fig. 3. Bloc diagram model of the inductance winding at the input of the PWM rectifier.

By applying the *Laplace* transform to the electrical Eqs. (1), (2) and bloc diagram models of Fig. 3 are deduced.

$$i_{conv} = \frac{1}{R + Ls}(V_{conv} - V_g) = \frac{1}{Ls}(V_{conv} - V_g - Ri_{conv}) \tag{2}$$

In the complex plane, Eq. (1) becomes

$$\underline{V_{conv}} = \underline{V_g} - jL\omega\underline{i_g} - R\underline{i_g} \tag{3}$$

where ω is the electrical angular frequency of the grid.

Representing voltages and currents as vectors in the complex plane, we obtain the phasor diagram of Fig. 4, which caracterizes standard and unit power factor operations of the single phase PWM boost rectifier.

Based on the vector representation of Fig. 4, the magnitude V_{convm} of the converter input voltage V_{conv} is expressed as in (4), where V_{gm} and I_{gm} are the magnitudes of the grid voltage and grid current, respectively. Note that in this equation, the voltage drop on resistance R can be neglected.

$$V_{convm} = \sqrt{(V_{gm} - RI_{gm})^2 + (L\omega I_{gm})^2} \approx \sqrt{V_{gm}^2 + (L\omega I_{gm})^2} \tag{4}$$

Since the instantaneous values of the voltage V_{conv} can be either $+V_{dc}$ or $-V_{dc}$ (according to the state of the switching control signal u), and based on Eq. (4), the V_{dc} voltage must verify the following equation

$$V_{dc} \geq \sqrt{{V_{gm}}^2 + (L\omega I_{gm})^2} \tag{5}$$

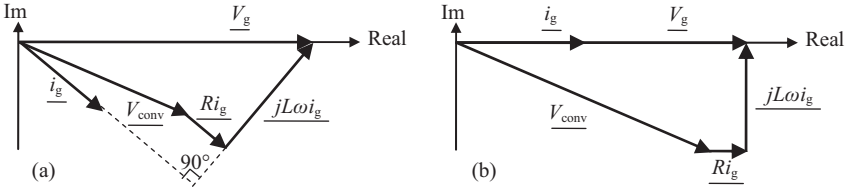

Fig. 4. Phasor diagram of single phase PWM rectifier (a) general case (b) unit power factor operation.

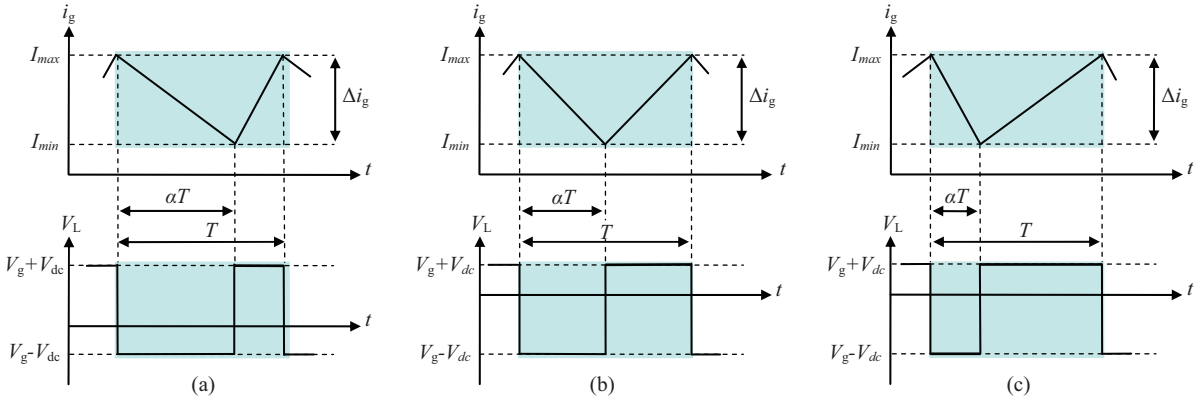

Fig. 5. Evolution of grid current i_g and inductance voltage V_L for (a) V_g positive (b) V_g null (c) V_g negative.

Based on Eq. (1), and neglecting the drop voltage on resistance R, the derivative of grid current can be expressed as follows

$$\frac{di_g}{dt} = \frac{1}{L}(V_g - V_{conv}) \tag{6}$$

Fig. 5 shows an example of the grid current evolution according to the sign of the grid voltage V_g. On this figure, α and T refer to the duty cycle of the switching control signal u and switching period, respectively. So, based on Fig. 5, the grid current can be expressed as in (7) during the [0, αT] interval.

$$i_g(t) = \frac{1}{L}(V_g - V_{dc})t + I_{\max} \tag{7}$$

Based on Eq. (7) and Fig. 5, the current ripple Δi_g^- during the [0, αT] interval can be expressed as follows

$$\Delta i_g^- = I_{\max} - I_{\min} = -\frac{1}{L}(V_g - V_{dc})\alpha T \tag{8}$$

During the interval [αT, T], the grid current can be expressed as follows

$$i_g(t) = \frac{1}{L}(V_g + V_{dc})(t - \alpha T) + I_{\min} \tag{9}$$

Based on Eq. (9) and Fig. 5, the current ripple Δi_g^+ during the [αT, T] interval can be expressed as follows

$$\Delta i_g^+ = I_{\max} - I_{\min} = \frac{1}{L}(V_g + V_{dc})T(1 - \alpha) \tag{10}$$

Supposing that the switching period is very small compared to the grid period, the current ripples Δi_g^+ and Δi_g^- can be considered equals ($\Delta i_g^+ = \Delta i_g^- = \Delta i_g$). In this case, the switching period T can be expressed as in (11).

$$T = \alpha T + (1 - \alpha)T = \frac{2L\Delta i_g V_{dc}}{V_{dc}^2 - V_g^2} \tag{11}$$

Based on Eq. (11), the maximum switching frequency $F_{\max}$ that can be achieved can be expressed as follows

$$F_{\max} = \frac{V_{dc}}{2L\Delta i_g} \tag{12}$$

It should be noted that the module of the current errors Δi_{conv} and Δi_g are equals.

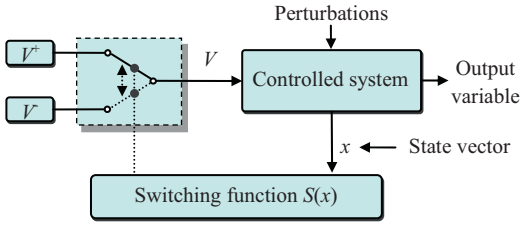

Fig. 6. Direct sliding mode control.

3. Synthesis of the rectifier control

3.1. Sliding mode theory

Let consider the following system

$$\frac{dx}{dt} = f(x) + B(x)V \tag{13}$$

where V is the input vector (m dimensional), x the system state vector (n dimensional), f the function describing the system evolution, and B a ($n \times m$) matrix.

For the synthesize of the sliding mode control, a switching function $S(x)$ (with dimension m) must firstly be defined.

$$S(x) = [S_1(x), \ldots, S_m(x)]^t \tag{14}$$

where $S_k(x)_{(k=1,\ldots,m)}$ is the kth switching function of $S(x)$. Note that there are different ways of defining the switching function $S(x)$. The set of points where the switching function is equal to zero ($S_k(x) = 0$, $k = 1,\ldots, m$) is known as the switching surface or sliding surface. A sliding mode control can then be performed based on the switching function $S(x)$ that has been defined. For the design of the sliding mode control, a given switching function $S(x)$ must verify the following attractivity equations

$$\begin{cases} \dot{S}_k(x) < 0 & \text{if} \quad S_k(x) > 0 \\ \dot{S}_k(x) > 0 & \text{if} \quad S_k(x) < 0 \end{cases} \quad (k = 1, \ldots, m) \tag{15}$$

The attractivity conditions of (15) ensure that each controlled variable approaches and reaches its corresponding sliding surface. In this work, we will focus on direct sliding mode control structure. The principle of this structure is shown in Fig. 6. The sliding mode control enables the structure of the system to be varied by simple commutation of power switches of static converters. The opening and close of power switches is performed according to the sign of the switching function $S(x)$. This type of control is also known as ON–OFF control for static converters. In this case, the switching logic is given by the following equation

$$V = \begin{cases} V^+ & \text{if} \quad S(x) > 0 \\ V^- & \text{if} \quad S(x) < 0 \end{cases} \tag{16}$$

3.2. PWM rectifier control

In the following, we will treat the synthesis of a single phase PWM boost rectifier control by means of sliding mode theory. As mentioned previously, the sliding mode theory was used to synthesize the internal current control loop. To this purpose, a switching function $S(i_{conv})$ is defined.

$$S(i_{conv}) = i^*_{conv} - i_{conv} \tag{17}$$

where $i_{conv}{}^*$ is the converter current reference. The switching function $S(i_{conv})$ defines a sliding surface ($S(i_{conv}) = 0$), where the trajectory of the current i_{conv} reaches its reference $i_{conv}{}^*$. The time derivative of the switching function $S(i_{conv})$

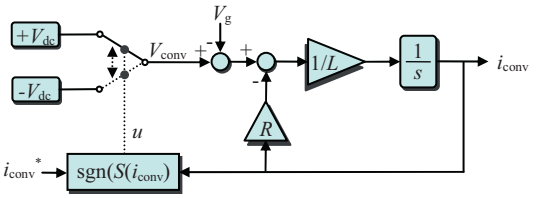

Fig. 7. Block diagram for sliding mode control of direct control of grid current.

can be used to analyze the evolution of the grid current i_{conv}. Since the current reference is considered constant each commutation period, the time derivative of the switching function $S(i_{conv})$ is given by the following equation

$$\dot{S}(i_{conv}) = -\frac{di_{conv}}{dt} = \frac{di_g}{dt} = -\frac{1}{L}(V_{conv} - V_g + Ri_g) \tag{18}$$

In order to ensure attractivity conditions of Eq. (15), the applied voltage V_{conv} is equal to $+V_{dc}$ or $-V_{dc}$ depending on the sign of switching function $S(i_{conv})$. Such control structure can be described by Eq. (19) and Fig. 7.

$$\begin{cases} (u = 1 \Rightarrow V_{conv} = +V_{dc}) & \text{if} \quad S(i_{conv}) < 0 \\ (u = 0 \Rightarrow V_{conv} = -V_{dc}) & \text{if} \quad S(i_{conv}) > 0 \end{cases} \tag{19}$$

Based on Eq. (19), it can be noted that:

- When the switching function $S(i_{conv})$ is negative, the applied V_{conv} voltage is equal to $+V_{dc}$. In this case, based on Eqs. (5) and (18), the time derivative of the switching function $S(i_{conv})$ is positive and attractive conditions of (15) are verified.
- When the switching function $S(i_{conv})$ is positive, the applied V_{conv} voltage is equal to $-V_{dc}$. In this case, based on Eqs. (5) and (18), the time derivative of the switching function $S(i_{conv})$ is negative and attractive conditions of (15) are verified.

A sign comparator allows determining the sign of the switching function $S(i_{conv})$. In practice, an hysteresis controller can be used instead of the sign comparator in order to limit the switching frequency of power switches [17]. As mentioned previously, a PI controller is added for the control of the V_{dc} voltage. The resulting control structure of a single phase PWM boost rectifier is presented in Fig. 8. In this case, for an hysteresis band of the hysteresis controller equal to Δh and based on Eq. (12), the achieved maximum frequency is equal to

$$F_{\max} = \frac{V_{dc}}{2L\Delta h} \tag{20}$$

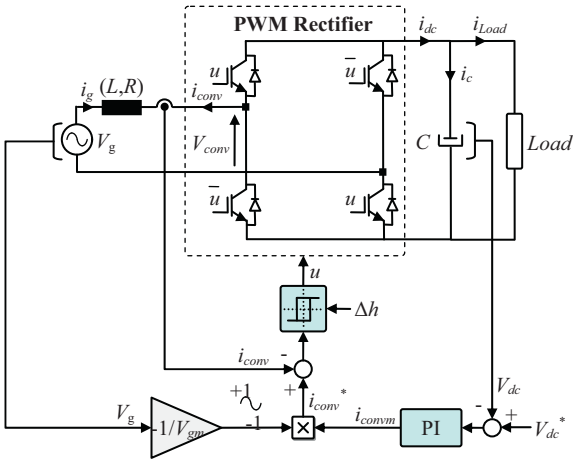

Fig. 8. Sliding mode control of single phase PWM boost rectifier.

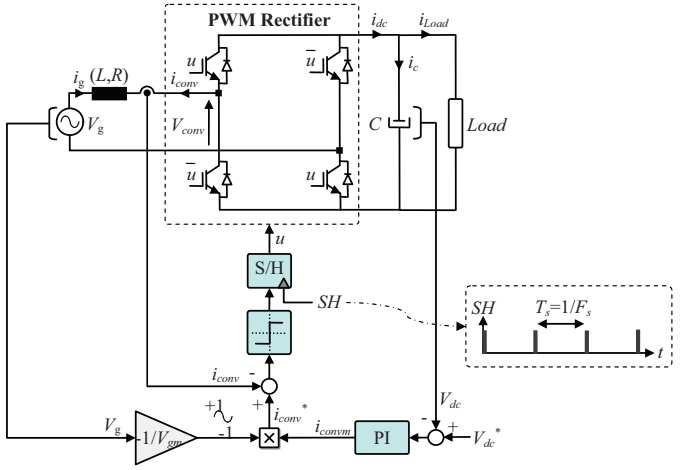

Fig. 9. Delta modulation sliding mode control of single phase PWM boost rectifier.

Another solution to limit the switching frequency of the power switches can be performed using the delta modulation technique [12,9] that replaces the hysteresis controller used for the current control loop by a sign comparator associated with a sample and holder. The principle of this technique is illustrated in Fig. 9. It looks quite similar to that of hysteresis current control, but the operating principle is different. In fact, only the error sign of the converter current error is detected by the sign comparator and the resulting control signal $u(t)$ is sampled at a fixed rate, so that the converter status is kept constant during each sampling period T_s. As a consequence, the switching frequency is limited to the half of the sampling frequency F_s. In this case, the magnitude of current ripples is not constant, it depends on the load parameters, the DC-link voltage and the used sampling frequency.

The i_{dc} current at the output of the PWM rectifier can be expressed as follows

$$i_{dc} = i_c + i_{Load} = C\frac{dV_c}{dt} + i_{Load} \tag{21}$$

By applying the *Laplace* transform to Eq. (21), the following equation is deduced

$$V_c = \frac{1}{Cs}(i_{dc} - i_{Load}) \tag{22}$$

Since the current i_{dc} is instantaneously equal to $\pm i_{conv}$, and considering that the time constant of the current control loop is negligible with regard to the time constant of the DC voltage control loop, the following bloc diagram presents the PI based control of the DC-link voltage.

The PI transfer function is given by the following equation

$$G_{PI}(s) = \frac{i_{dc}^*}{\Delta V_{dc}} = k_{pdc} + \frac{k_{idc}}{s} \tag{23}$$

Based on Fig. 10, and neglecting the load current i_{Load}, the transfer function of the DC-link voltage control loop can be expressed as in Eq. (24).

$$\frac{V_{dc}}{V_{dc}^*} = \frac{(k_{pdc}/C)s + (k_{idc}/C)}{s^2 + (k_{pdc}/C)s + (k_{idc}/C)} = \frac{(k_{pdc}/C)s + (k_{idc}/C)}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{24}$$

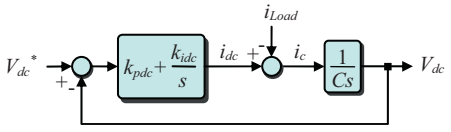

Fig. 10. Simplified block diagram of PI based DC-link voltage control.

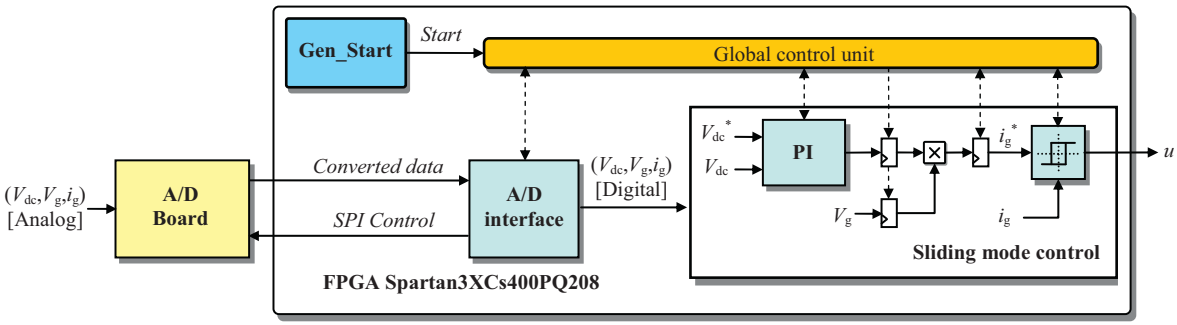

Fig. 11. FPGA-based hardware architecture.

The obtained transfer function of Eq. (24) is a second order system that can be identified to the canonial structure of a second order system (in the left side of Eq. (24)). By identifying terms of (24), the obtained second order system is characterized by a natural frequency of oscillation ω_n and a damping ratio ξ verifying the following equations

$$\begin{aligned} 2\xi\omega_n &= \frac{k_{pdc}}{C} \\ \omega_n^2 &= \frac{k_{idc}}{C} \end{aligned} \tag{25}$$

Then, the shape and the dynamic of the DC-link voltage response are imposed by fixing the natural frequency of oscillation ω_n and the damping ratio ξ. So, the k_{pdc} and k_{idc} gains can be tuned as follows

$$\begin{aligned} k_{pdc} &= 2C\xi\omega_n \\ k_{idc} &= C\omega_n^2 \end{aligned} \tag{26}$$

4. FPGA-based control architecture

The control architecture was implemented on the Spartan3 XC3S400PQ208 from Xilinx Inc. that contains 400,000 logical gates and 50 MHz oscillator. Fig. 11 shows the designed hardware architecture for the sliding mode control of a single phase PWM boost rectifier. In order to perform easier design of the hardware architecture, the control architecture was divided into several modules, which are easier to develop and which make sense from a functional point of view. The different elementary modules are:

- *Gen_Start module*: This module allows the generation of the pulse *Start* signal. It activates the global control unit (which is a finite state machine) each sampling period T_s.
- A/D *interface module*: This module allows the control of the A/D board. It controls the A/D conversion board through SPI (Serial Peripheral Interface) protocol. The computation time $t_{A/D}$ of the A/D interface module is equal to 1.34 μs.
- *Sliding mode control module*: This module includes two different modules. The first module is a PI module, which is used for the control of the DC-link voltage V_{dc}. It generates the magnitude of the converter current reference i_{conv}^* based on the difference between the reference voltage V_{dc}^* and the measured one V_{dc}. The computation time of the PI module is equal to 0.16 μs. The second module is the hysteresis controller module. This module computes the logical level of the switching control signal u according to the sign of the switching function $S(i_{conv})$. It is caracterized by a computation time t_H equal to 0.08 μs.

Table 1 presents the performances of the implemented control architecture. In this table, two execution times T_{ex1} and T_{ex2} are defined for the execution of the current control loop and DC-link voltage control loop, respectively. It can be noted that the obtained execution times are very small and equals to only few micro-seconds.

$$\begin{aligned} T_{ex1} &= t_{A/D} + t_H = 1.42\ \mu s \\ T_{ex2} &= t_{A/D} + t_{PI} + t_H = 1.58\ \mu s \end{aligned} \tag{27}$$

Table 1
Time area performances of the designed hardware architecture.

Module	Latency	Computation time
A/D module	67	$t_{AD} = 1.34\ \mu s$
PI	10	$t_{PI} = 0.16\ \mu s$
Hysteresis	4	$t_{Hyst} = 0.08\ \mu s$
Execution time $T_{ex1} = t_{A/D} + t_H$		$T_{ex1} = 1.58\ \mu s$
$T_{ex2} = t_{A/D} + t_{PI} + t_H$		$T_{ex2} = 1.42\ \mu s$
Consumed resources		4009 tuiles of 13,824 (29%)

- First FPGA implementation method

  Fig. 12 shows the timing diagram corresponding to the first FPGA implementation method, which is aimed to realize an hysteresis based control. Such timing sequences can be easily done by forcing the *Start* signal of the global control unit at a permanent active level in order to activate each computation cycle immediately after the achievement of the previous one. Each computation cycle, the global control unit activates in parallel mode the A/D interface module and the PI module. When the computation cycle of the PI module is achieved, the global control unit activates the hysteresis module that allows the computation of the control signal u. The sum of the computation times of the PI and hysteresis module (t_{PI} and t_H) is lower than the A/D conversion time t_{AD}. For this reason, the global control unit restarts new computation cycle, immediately after the achievement of the A/D conversion process. As a consequence, the sampling period T_s is equal to the A/D conversion time t_{AD} and the execution time is equal to the sum of t_{AD}, t_{PI} and t_{Hyst} as mentioned previously. When associated to fast A/D converters, the high computation capabilities of FPGA solutions allows obtaining very low execution time of only few micro seconds. Thus, the obtained digital feedback loop can be approximated quite closely to an analog one because the effects of sampling and computing delays are very negligible. In order to illustrate the effects of the computation time delays on the performances of the current control, Fig. 13 shows a comparison between performances of hysteresis current control obtained for very low execution time and high execution time. This figure shows that, with a very low execution time, the waveform of the instantaneous current error Δi_{conv} is kept inside the tolerance band imposed by the hysteresis controller, which is not the case for a higher execution time.

  However, the drawback of this method is that very low sampling period is used, which results on increasing the width of the used fixed point format for modules with coefficients that depend on the used sampling period like the case of the PI module.

- Second FPGA implementation method

  The second FPGA implementation method is quite similar to the first one and is also aimed to realize an hysteresis based control. The corresponding timing diagram is presented in Fig. 14. It is characterized by a multi-sampling operating mode, where the internal current control loop and the external DC-link voltage control loop work with different sampling periods. The internal current control loop is still sampled with a very low sampling period T_L equal to the A/D conversion time, which allows keeping the Δi_{conv} current error inside the hysteresis band during

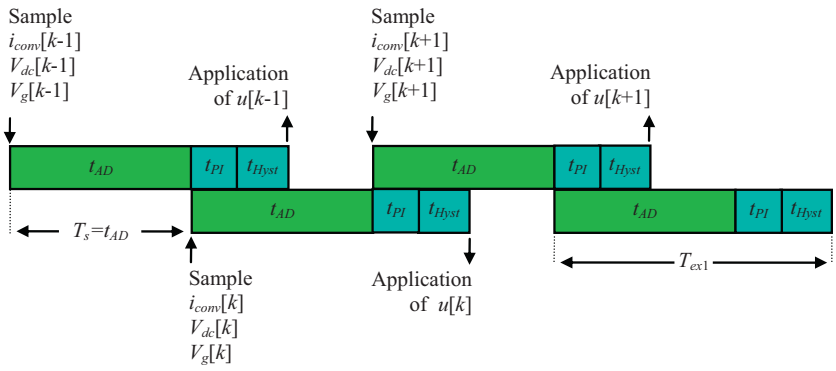

Fig. 12. Timing diagram for the realization of an hysteresis based current control of single phase PWM boost rectifier.

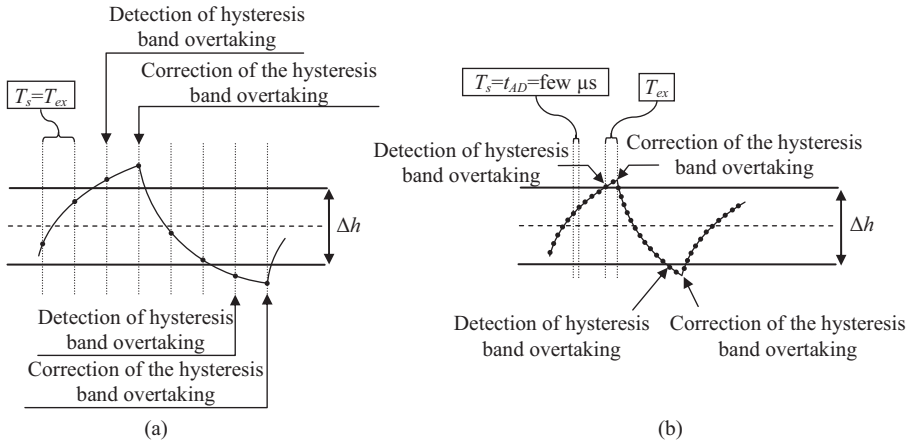

Fig. 13. Instantaneous current error waveform during steady state for an hysteresis based current control with (a) low execution time (b) high execution time.

steady state. The external DC-link voltage control loop is sampled with higher sampling period and consequently there is no need to increase the width of the fixed point format used for the PI module.

- Third FPGA implementation method

The realization of the current control of a single phase PWM boost rectifier based on delta modulation technique can be easily performed based on the same architecture presented in Fig. 11. Only few modifications are required. They consist into fixing the hysteresis band value to zero (in this case the hysteresis comparator becomes equivalent to a sign comparator), changing the global control unit operating mode and changing the activation mode of the *Start* signal. Compared to the case of hysteresis current control, the A/D interface module and the hysteresis module are not activated at the same time but in a sequential mode. The *Start* signal is not yet forced to an active level but it becomes an active pulse signal with a sampling period equal to T_s. This leads to the sequential timing diagram presented in Fig. 15, which characterizes the FPGA implementation of a delta modulation current control technique for the control of a single phase PWM boost rectifier. Based on this figure, it can be noted that the application of the computed logical level of the control signal u is performed every sampling period T_s. Consequently, the switching frequency will be variable without exceeding the half of the sampling frequency F_s.

5. Experimental set up

In order to verify the efficiency of the designed FPGA-based hardware architecture for the control of a single phase PWM boost rectifier, an experimental prototyping platform was developed. The designed architecture of the control algorithm was tested with the experimental set-up presented in Figs. 1 and 16. The power part of this experimental set-up is composed of a single-phase autotransformer, which is used to impose the magnitude of the grid voltage V_g in

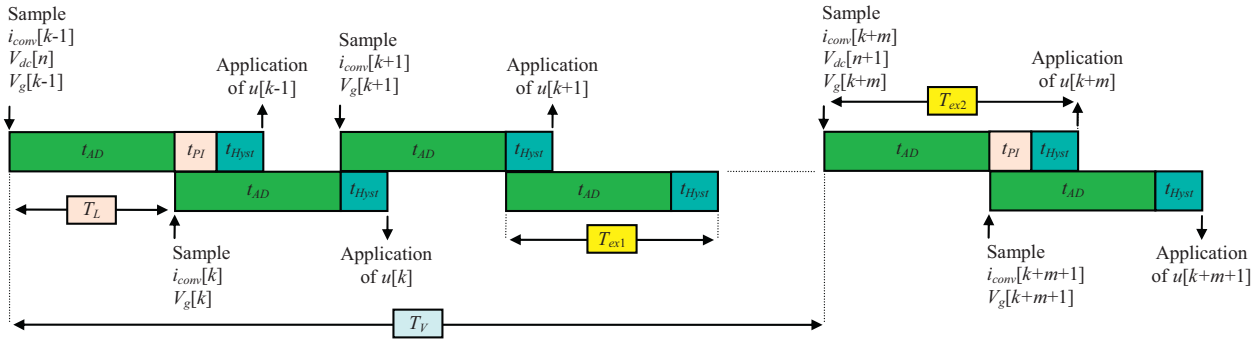

Fig. 14. Timing diagram for the realization of an hysteresis based current control of single phase PWM boost rectifier with multi-sampling periods.

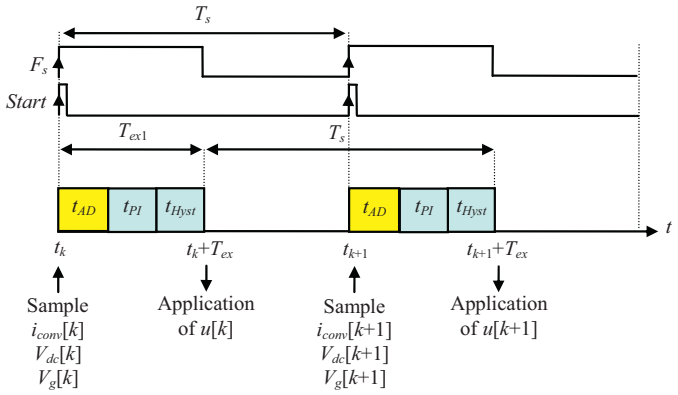

Fig. 15. Timing diagram for the realization of a delta modulation current control of single phase PWM boost rectifier.

the grid side of the single phase PMW boost rectifier. Also, it includes an inductance (20 mH, 20 A) placed between the autotransformer and the single-phase PWM boost rectifier. Finally, a variable resistive load is connected to the DC-link. The interface part is composed of an A/D conversion board based on serial ADCs, converter current sensor (for i_{conv}), two voltage sensors (for V_{dc} and V_g) and an interface circuit board, which provides the voltage level adaptation of the switching control signal between FPGA board and power switches drivers. Not that for the experimental setup, only the third case of FPGA implementation was tested.

The start up of the single phase PWM rectifier was done in three steps. Firstly, the switching states of the PWM rectifier are all set to zero. In this case, the single phase PWM boost rectifier works as a diode rectifier. During this step, the resistive load is disconnected and the DC voltage level was set equal to 100 V. Then, the computed switching control signal u was applied to the PWM rectifier. The $V_{dc}{}^*$ reference voltage was set equal to 200 V. Fig. 17a shows the response of the DC-link voltage V_{dc} and the converter current i_{conv}. It can be noted that the V_{dc} voltage is well controlled and becomes equal to its reference in steady state. The transient state is characterized by an increase of the magnitude of line currents, which becomes again equal to zero in steady state. Finally, the load is connected to the DC link. As shown in Fig. 17b, the V_{dc} voltage decreases slightly at connection of the load, then the control compensate the load disturbance and the V_{dc} voltage level remain equal to its reference. It can be noted also that the magnitude of the current i_{conv} increases. Fig. 17c presents the evolution of the converter current i_{conv} and grid voltage V_g during steady state operation. It can be noted that the single-phase PMW boost rectifier is characterized by a sinusoidal current absorption and unit power factor operation.

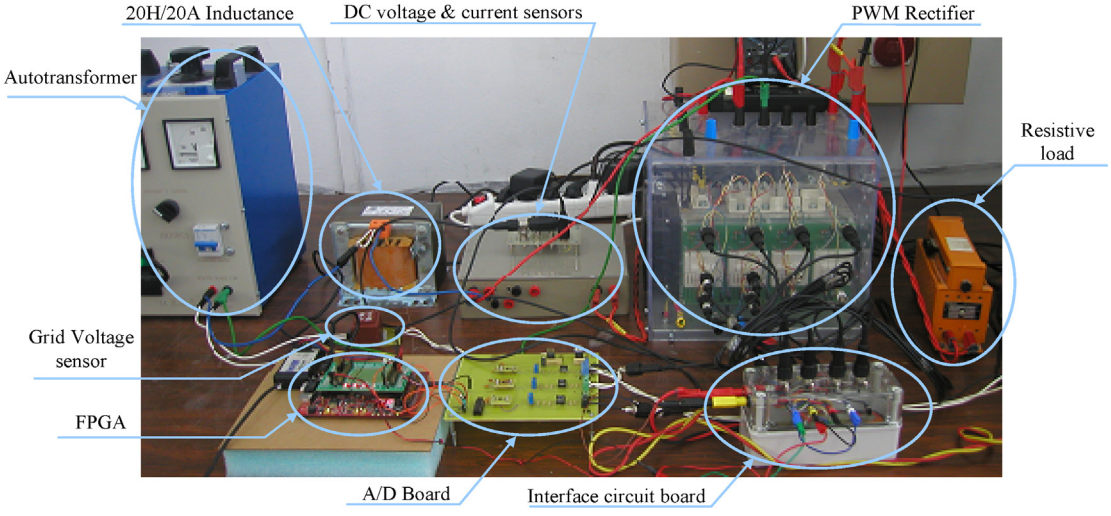

Fig. 16. Experimental setup.

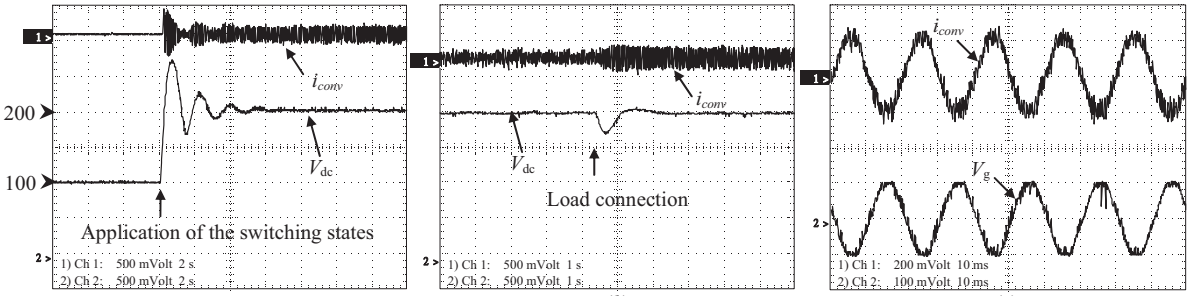

Fig. 17. Experimental results (a) response to 200 V step reference of $V_{dc}{}^{*}$, (b) load connection and (c) grid voltage and converter current.

6. Conclusion

A sliding mode control of single-phase PWM boost rectifier was presented in this paper. The control was made up of an internal current control loop and external DC-link voltage control loop. The current control loop was synthesized via the sliding mode theory, which is characterized by its robustness, disturbance rejection and insensitivity to parameter variations. The external control loop was synthesized based on a PI controller. The control architecture was implemented on a Spartan 3 FPGA target from Xilinx Company with an execution time of only few microseconds. The obtained experimental results validate of the effectiveness of the designed hardware architecture. It was shown that the implemented control allows good regulation of the DC bus, sinusoidal current absorption and unit power factor operation.

Acknowledgment

This work was supported by the Tunisian Ministry of High Education, Research and Technology.

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