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Efficient Design and Fpga Implementation of Digital Controller Using Xilinx SysGen®

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Abstract: The paper explains a method for the design and implementation of digital controller based on Field Programmable Gate Array (FPGA) device. It is more compact, power efficient and provides high speed capabilities as compared to software based PID controllers. The proposed method is based on implementation of Digital controller as digital filters using DSP architectures.. The PID controller is designed using MATLAB and Simulink to generate a set of coefficients associated with the desired controller characteristics. The controller coefficients are then included in VHDL that implements the PID controller on to FPGA. MATLAB program is used to design PID controller to calculate and plot the time response of the control system. The synthesis report conclude the resource utilization of selected FPGA.

Keywords: Digital PID Controller, FPGA, Digital Filter Architecture, Matlab, Simulink, Xilinx ISE, Spartan3

1. INTRODUCTION

A control system is compared of two subsystems, a plant and a controller. The plant is an entity controlled by the controller. The controller can be either analog or digital. Generally, an implementation of digital PID controller includes the use of microprocessors or microcontrollers. The memory holds the application program while the processor fetches, decodes, and executes the program instructions. This method has a disadvantage in speed of operations because the operations depend on software which has a sequence of instructions and commands which needs many machine cycles to execute. Therefore, FPGA-based digital PID controller is proposed because the operations on FPGA are hardware compatible operations. However, FPGA-based digital PID controller still needs multipliers for computation. These multipliers will decrease the speed of processing time because the multiplying stage is a consumption process which introduces propagation delay and uses large part of silicon area. These multiplications are change to Distributed Arithmetic (DA) architecture which was first proposed by Peled and Liu in 1974 [2].

Today's high-speed and high-density FPGA's provide practical design alternatives to ASIC and microprocessor-based implementations.

2. DIGITAL PID CONTROLLER

One of the most powerful but complex controller mode operations combines the proportional, integral, and derivative modes with a control loop feedback mechanism widely used in industrial control system.

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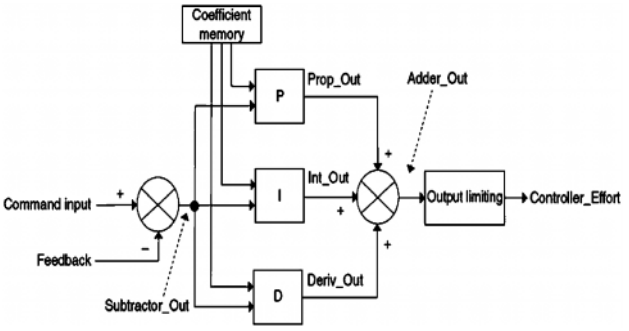

Figure 1: Digital PID Controller [9]

The proportional, integral, and derivative control actions can be brought together to create a PID controller. Fig.1 shows an example of how this can be created. As the design increases in complexity, the need for more additions or subtractions and multiplications or divisions increases. This highlights the need to develop an architecture that uses hardware proficiently and can operate within the time constraints of the design. The arithmetic operations which are to be undertaken can be designed to be either separate actions (each action requiring its own dedicated hardware) or can be shared i.e. each addition, subtraction, multiplication, or division has a single common block, as is typical in the architecture of an arithmetic and logic unit, (ALU). Thus, in order to design digital PID controller we use the above architecture as the base which will improve hardware efficiency [3].

3. PRINCIPLE OF OPERATION

Consider the block diagram of digital control system as shown below.

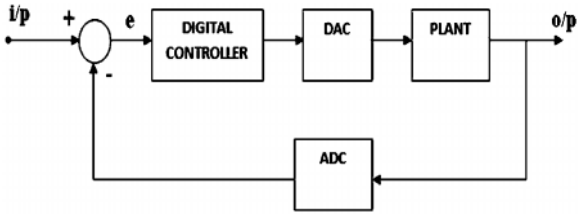

Figure 2: Block Diagram of Digital Control System

The analytical equation is:

$$P = K_p e + K_I \int e dt + K_D (de/dt) + P_I (0) \quad (1)$$

Where,

K_P = proportional gain

K_D = derivative gain

e = error in % of full scale range

K_I = integral gain

$P_I(0)$ = value of integral term at $t = 0$

Taking Laplace transform of equation (1) will result in,

$$P(S) = KpE(S) + \frac{K_I}{s} E(S) + K_D S E(S) \quad (2)$$

Also the transfer function of PID controller is

$$D(S) = K_p + \frac{K_I}{S} + K_D S \quad (3)$$

Where,

$D(S)$ is transfer of PID controller.

Transforming equation (3) into digital domain gives the transfer function of digital PID controller.

$$D(z) = K_p + K_1 \frac{T}{2} \frac{(z+1)}{(z-1)} + \frac{K_D}{T} \frac{(z-1)}{z} \quad (4)$$

Equation (4) can be realized to direct form structure as

$$D(z) = \frac{a_0 + a_1 z^{-1} + a_2 z^{-2}}{1 + b_1 z^{-1} + b_2 z^{-2}} \quad (5)$$

Normally for digital controller $b_2 = 0$ and $b_1 = -1$

Therefore, coefficients a_0, a_1 and a_2 can be given as

$$a_0 = K_p + K_I \frac{T}{2} + \frac{K_D}{T}$$

$$a_1 = K_p + K_I \frac{T}{2} - 2\frac{K_D}{T}$$

$$a_2 = \frac{K_D}{T}$$

Where K_P, K_I and K_D are proportional, integral and derivative parameters respectively of digital PID controller and T is sampling period. Fig. 3 shows the direct form I structure of digital PID controller corresponding to equation (5)

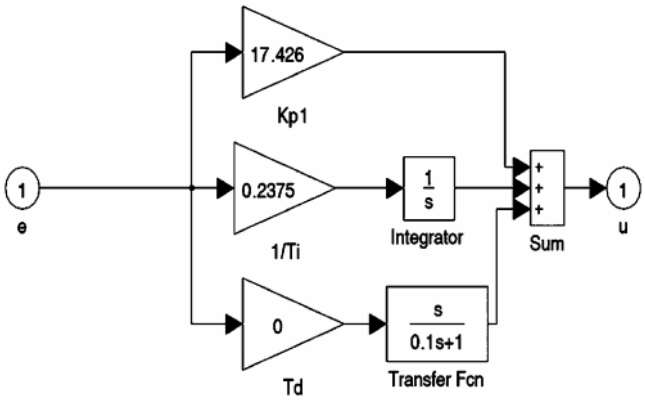

Figure 3: Direct Form I Structure of Digital PID Controller

4. FPGA IMPLEMENTATION

System Generator implements the design by considering the correct hardware platform and also takes care of the synchronization and interfacing problems. [3]

A separate test bench application for hardware (FPGA) verification is also not required. The co-simulation block can be used with the same Simulink test bench apparatuses that were used to test the original System Generator model. Along- disadvantages also, that are associated with the presented co simulation methodology/tools using automatic bit stream generation. With every release of System Generator, the top level output files change.

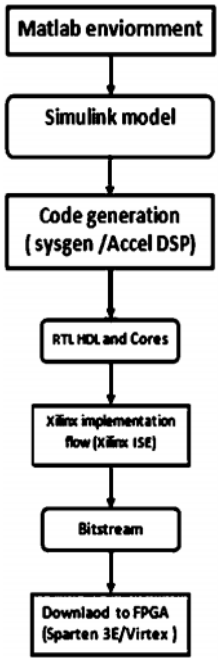

Figure 4: Design Methodology [3]

Fig 4 illustrates the design flow adopted for the design of given PID controller.

The plant under test was a D. C. Motor which is represented by the following transfer function.

The speed sensor has a ratio of 0.2; the input signal was 100 mV, representing a desired output speed of 12.5 rps or 750 rpm. [8]

The PID parameters for this required output speed are shown in Fig 5(a).

By using sampling frequency 10 kHz or $T = 0.0001$ s

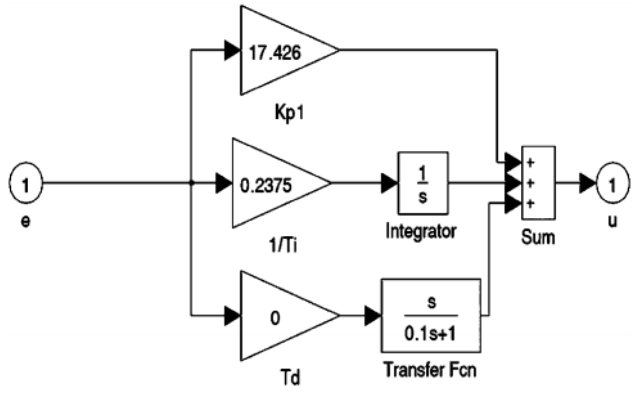

Figure 5(a): Simulink Implementation of PID Controller

The system generator is a Xilins tool box available with MATLAB.

The blocks used for designs are as shown in the fig5(c)

Then the PID controller is implemented in Xilinx Sys gen and simulink as shown in Fig 5(c).

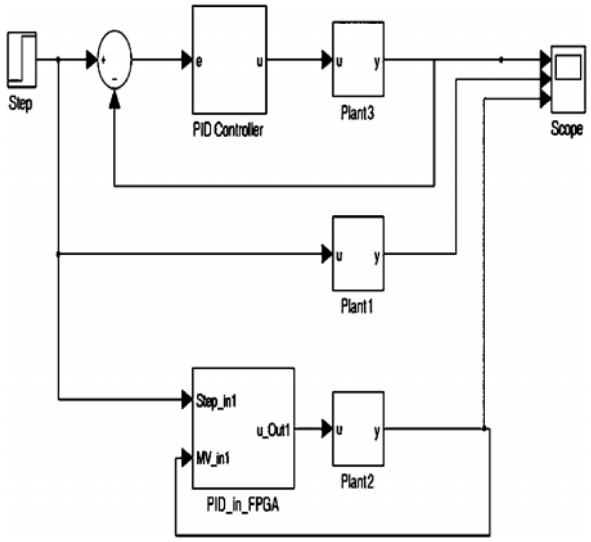

Figure 5(b): Simulink Implementation of Controlled System

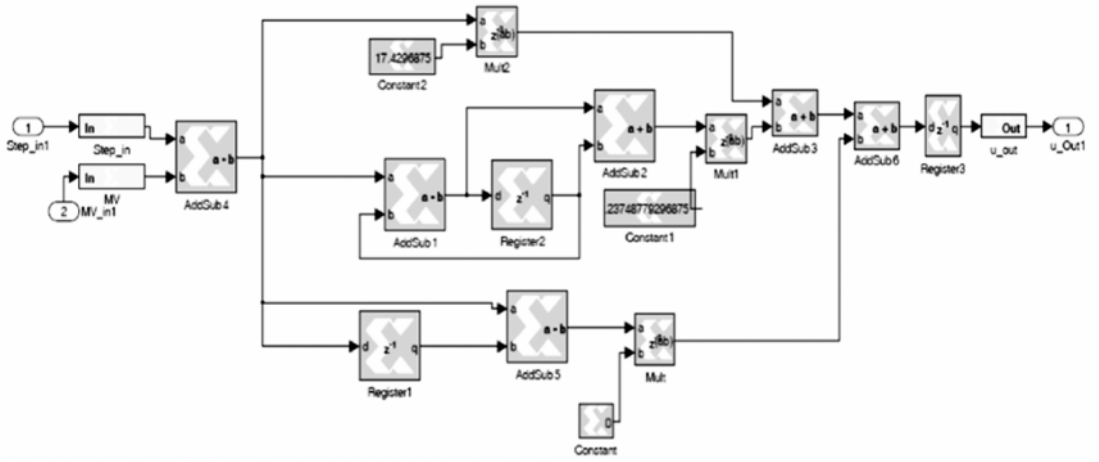

Figure 5(c): SysGen Implementation of PID Controller

5. RESULTS

Here in fig.6 are the simulation results of FPGA based digital PID controller with multiplier. Figure 6(a) gives the comparison between the outputs of simple PID controller, FPGA based digital PID controller. The above figure gives the synthesis report of FPGA based digital PID controller.

The synthesis using Xilinx ISE tools resulted in the following Synthesis report for a Spartan3 as target FPGA. The device utilization summary shown in Table 1 below shows that merely 3% of the total resources/slices are used for the above implementation and a maximum frequency of 37.259 MHz is quiet faster for the control applications.

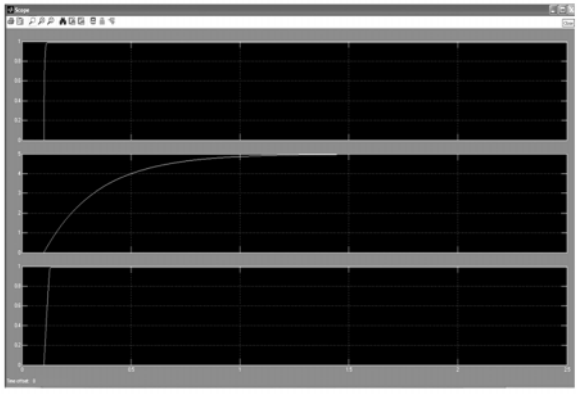

Figure 6(a): Output Comparison of Plant Controlled Variable

Table 1

Device Utilization Summary			
Logic Utilization	*Used*	*Available*	*Utilization*
Number of Slice Flip Flops	240	7,168	3%
Number of 4 input LUTs	236	7,168	3%
Logic Distribution			
Number of occupied Slices	218	3,584	6%
Number of Slices containing only related logic	218	218	100%
Number of Slices containing unrelated logic	0	218	0%
Total Number of 4 input LUTs	278	7,168	3%
Number used as logic	236		
Number used as a route-thru	42		
Number of bonded IOBs	49	141	34%
Number of MULT18X18s	3	16	18%
Number of BUFGMUXs	1	8	12%
Number of RPM macros	6		

Design statistics: Minimum period: 26.839ns (Maximum frequency: 37.259MHz)

6. CONCLUSION

Implementing the digital PID controller on FPGA gives better rise time as well as settling time as seen in the results. In designing and implementing the digital PID controller one major thing which affects the performance of controller and its effects on plant is the effective hardware utilization. Also implementing PID controller on FPGA features speed, accuracy, power, compactness, and cost improvement. In future work we plan to investigate implementation of multiplierless digital PID controller using distributed arithmetic architecture. The advantages are high processing speed, reduced power consumption and hardware compatibility for implementing on FPGA.

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