Measuring Hardware Counters for HPC Application Phase Detection

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Introduction

`Motivation`:

- Memory-bound: programs with misses cache rate considerable (e.g. Breadth-First Search)
- CPU-bound: programs limited by processing (e.g. Matrices Multiplication)
- Programs can have fragments more Memory-bound than others more CPU-bound (e.g. Fourier Transform)

`Objective`:

- Measure hardware counters at every given time interval to discover memory-bound regions

Related Works

`Spiliopoulos et al` [1]:

- Tool that analyzes the behavior of sequential application (the concept of phases);
- Based on cache misses of different caches' levels.

`Laurenzano et al` [2]:

- Finer granularity for each application loop.

Related Works

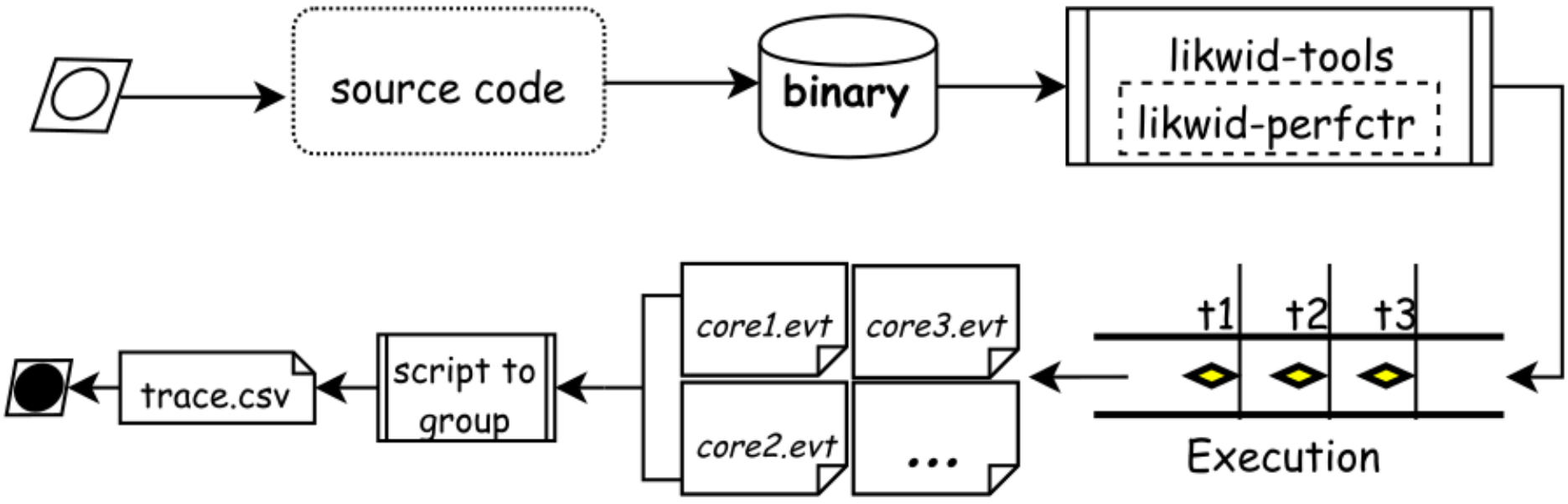
`Freeh et al.`[3]:

- Define the most suitable frequency for each phase of MPI applications;
- Analyse of the best frequency for each node.

`Millani and Schnorr` [4]:

- OpenMP applications
- Analyse of parallel regions of programs
- Manual instrumentation of code to identify

Methodology



Preliminary Results : NPB-FT, B Class

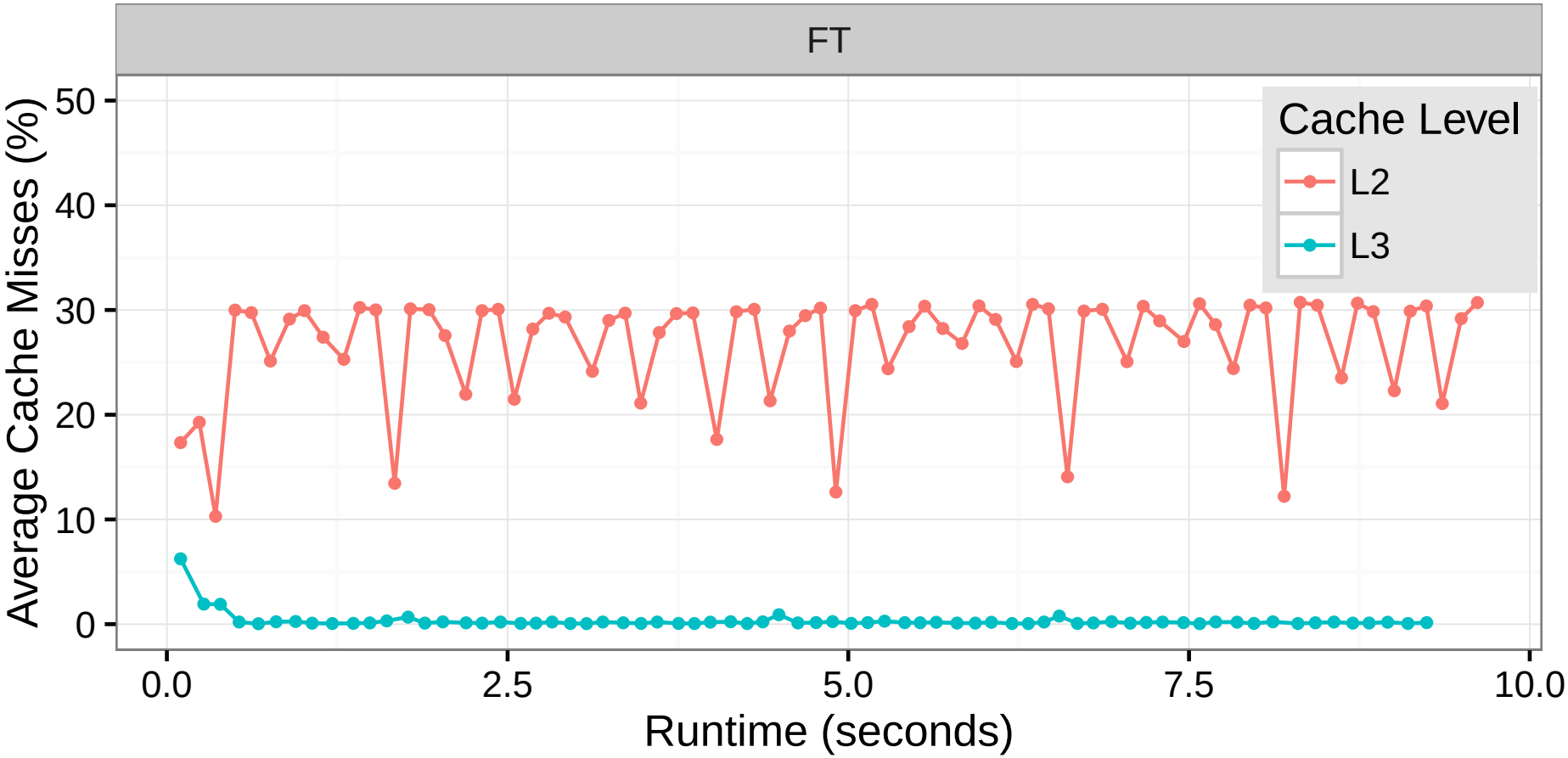


Figure : Sampling interval - 100 milliseconds.

Preliminary Results : NPB-LU, B Class

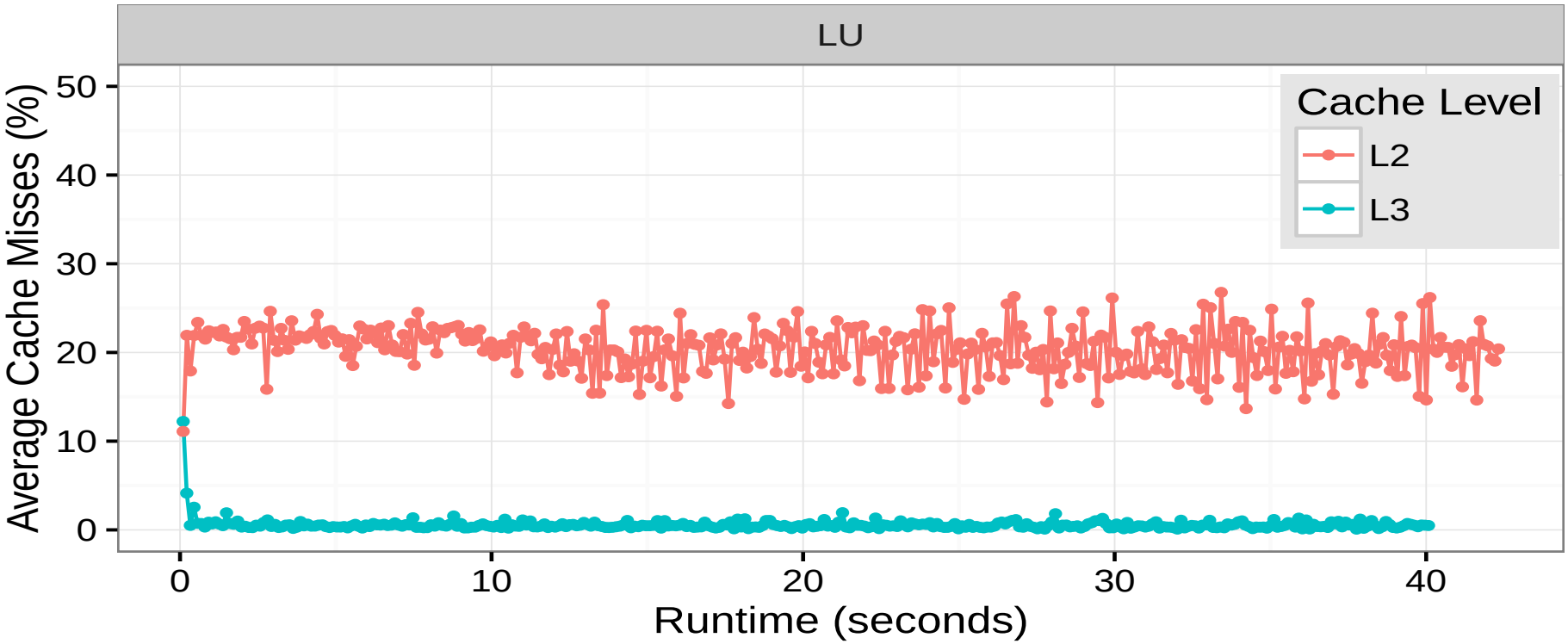


Figure : Sampling interval - 100 milliseconds.

Preliminary Results : NPB-CG, B Class

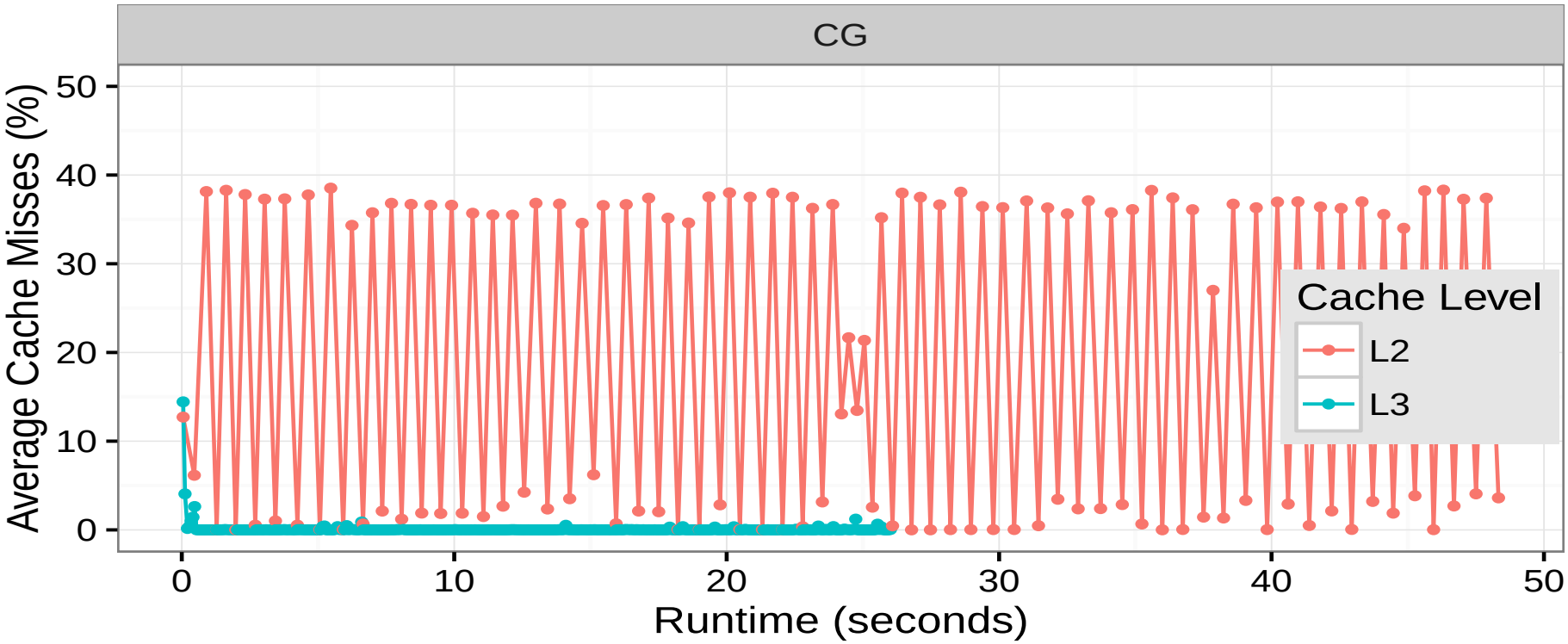


Figure : Sampling interval - 50 milliseconds.

Conclusion

`Contributions`:

- Fine-granularity to identify the memory-bound regions of parallel application several timestamps;
- Lower overhead of measurement.

`Future work`:

- Automatically identify the memory-bound regions based on the hardware counters
- Reducing the power consumption of parallel applications (use of DVFS approach)

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Thank you for your attention!