Project 1 Documentation

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Documentation Video Link
https://drive.google.com/file/d/1q4xw2F2tjG0houzouMsQrapHAjkyyq4a/view?usp=share_link

Documentation Outline
This Project 1 documentation shall be divided into three subsections:

I. Adder
II. Two seven-segment displays
III. Divisibility lights

I. Adder

For the adder part, the circuit uses two 4-input pins which are both connected to an Adder component from the *Arithmetic* folder in Logisim. Then, a splitter with a fan out of four bits is connected to the main output of the Adder—the single output on the right—to *split* the 4-bit output into single bits.

The four resulting outputs of the splitter, and the *carry out* output of the Adder, are then connected to a splitter with a fan in of five bits, whose output is the sum of the two 4-bit numbers. This is to combine the carry out with the four adder bits and to make the main circuit cleaner. The output from the 5-fan in splitter will then be used as input to the subcircuits of the 7-segment displays and the divisibility indicator LEDs, as seen below in Figure 1.

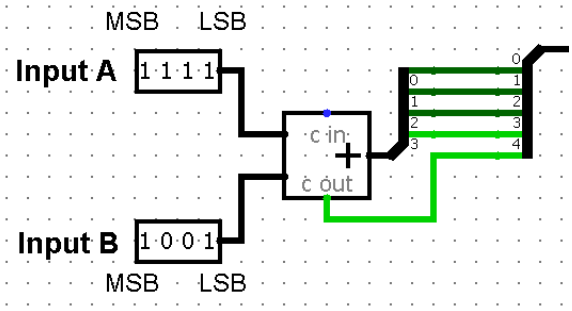


Figure 1. Two 4-bit inputs with the Adder Component

II. Two 7-segment displays

Table 1 and 2 are truth tables of the two 7-segment displays, with the lowercase letters corresponding to the segments in the following configuration in Figure 2. We call the left 7-segment display as the *Tens 7-segment*, and the right 7-segment display as the *Ones 7-segment.*

I based the Boolean values of each segment on its visual representation of each number. For example, to represent a zero, segments *a, b, c, d, e,* and *f* should light up, which means segments *a* to *f* must be a 1 in the truth table, except segment *g*. This will be done for possible sum from 0-31. Then, the resulting SOP from the K-maps of each segment will be simplified using axioms and theorems to make the implementation easier, and to lessen the number of gates used. The last expression in bold shall be the ones implemented in Logisim. A screenshot of the resulting subcircuit will then be shown. Note that there shall be one subcircuit per segment

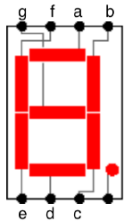


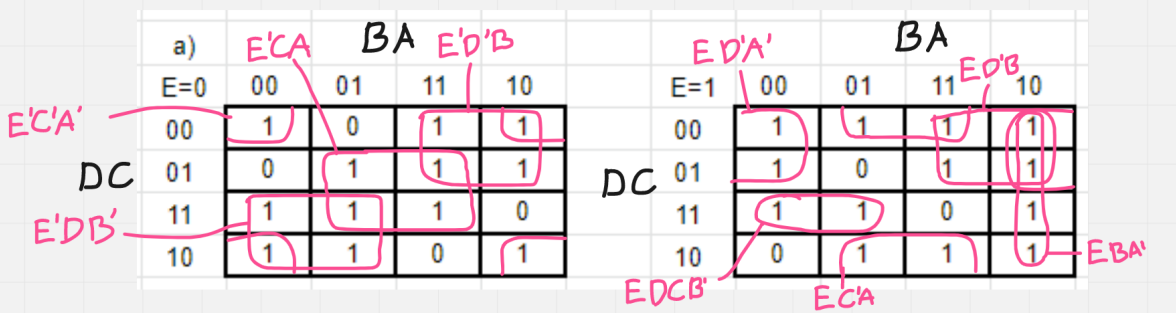
Figure 2. 7-segment display input configuration

of the two 7-segment displays. This is so that the logic gates of each segment are abstracted in the final circuit, resulting in a cleaner main circuit.

Dec.	E	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	0	1	0	1	1	0	0	0	0
2	0	0	0	1	0	1	1	0	1	1	0	1
3	0	0	0	1	1	1	1	1	1	0	0	1
4	0	0	1	0	0	0	1	1	0	0	1	1
5	0	0	1	0	1	1	0	1	1	0	1	1
6	0	0	1	1	0	1	0	1	1	1	1	1
7	0	0	1	1	1	1	1	1	0	0	0	0
8	0	1	0	0	0	1	1	1	1	1	1	1
9	0	1	0	0	1	1	1	1	1	0	1	1
10	0	1	0	1	0	1	1	1	1	1	1	0
11	0	1	0	1	1	0	1	1	0	0	0	0
12	0	1	1	0	0	1	1	0	1	1	0	1
13	0	1	1	0	1	1	1	1	1	0	0	1
14	0	1	1	1	0	0	1	1	0	0	1	1
15	0	1	1	1	1	1	0	1	1	0	1	1
16	1	0	0	0	0	1	0	1	1	1	1	1
17	1	0	0	0	1	1	1	1	0	0	0	0
18	1	0	0	1	0	1	1	1	1	1	1	1
19	1	0	0	1	1	1	1	1	1	0	1	1
20	1	0	1	0	0	1	1	1	1	1	1	0
21	1	0	1	0	1	0	1	1	0	0	0	0
22	1	0	1	1	0	1	1	0	1	1	0	1
23	1	0	1	1	1	1	1	1	1	0	0	1
24	1	1	0	0	0	0	1	1	0	0	1	1
25	1	1	0	0	1	1	0	1	1	0	1	1
26	1	1	0	1	0	1	0	1	1	1	1	1
27	1	1	0	1	1	1	1	1	0	0	0	0
28	1	1	1	0	0	1	1	1	1	1	1	1
29	1	1	1	0	1	1	1	1	1	0	1	1
30	1	1	1	1	0	1	1	1	1	1	1	0
31	1	1	1	1	1	0	1	1	0	0	0	0

Table 1. Truth table of Ones 7-segment

(a) SOP of *a* (Ones 7-segment)



Expression	**Theorem/Axiom**
E'C'A'+E'DB'+E'CA+E'D'B+EDCB'+ED'A'+EC'A+ED'B+EBA'	Given
E'(C'A'+DB'+CA+D'B)+EDCB'+ED'A'+EC'A+ED'B+EBA'	Distributivity
E'(C'A'+DB'+CA+D'B)+E(DCB'+D'A'+C'A+D'B+BA')	Distributivity

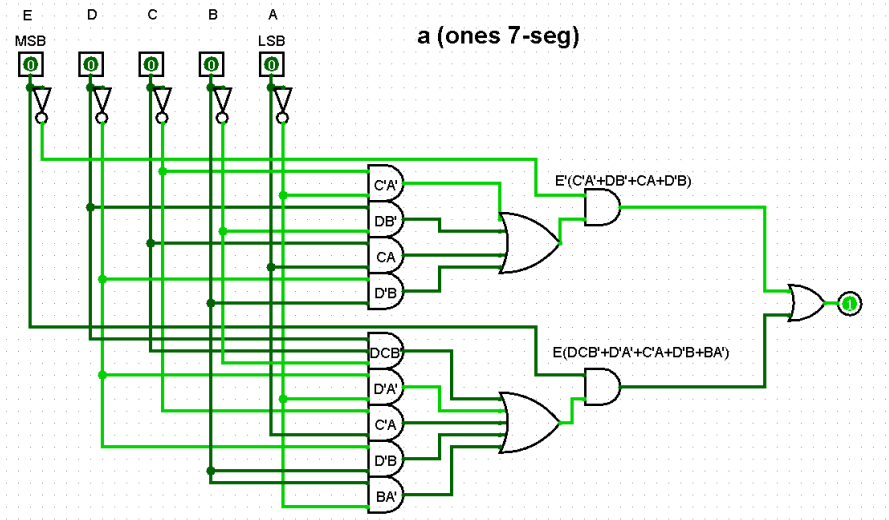
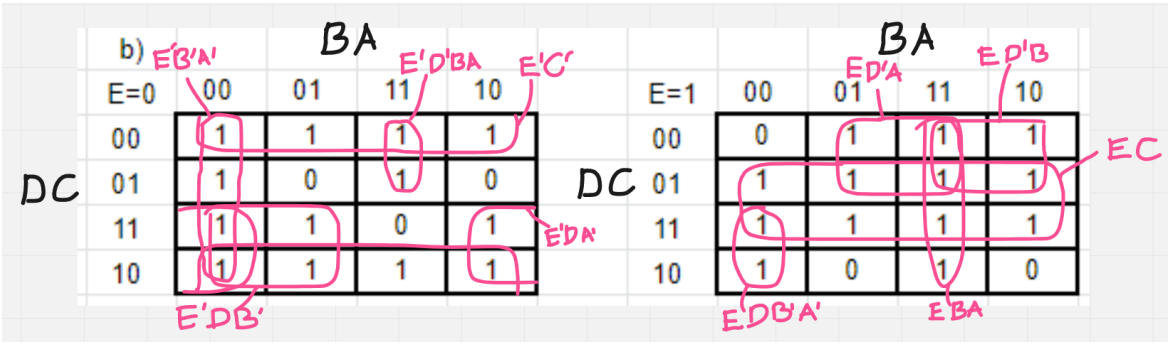


Figure 3. Subcircuit of segment *a* of the Ones 7-segment

(b) SOP of *b* (Ones 7-segment)



Expression	**Theorem/Axiom**
E'B'A'+E'D'BA+E'C'+E'DB'+E'DA'+ED'A+ED'B+EC+EDB'A'+EBA	Given
E'(B'A'+D'BA+C'+DB'+DA')+ED'A+ED'B+EC+EDB'A'+EBA	Distributivity
E'(B'A'+D'BA+C'+DB'+DA')+E(D'A+D'B+C+DB'A'+BA)	Distributivity

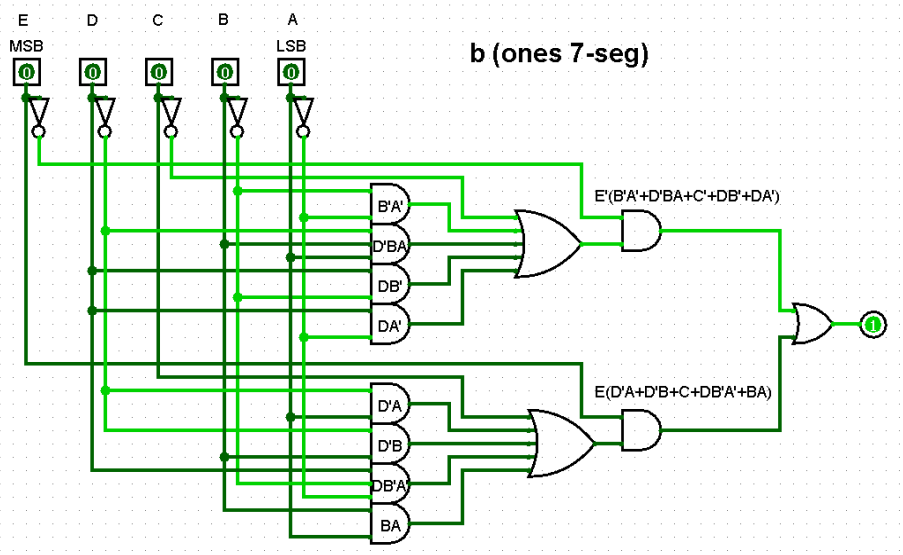
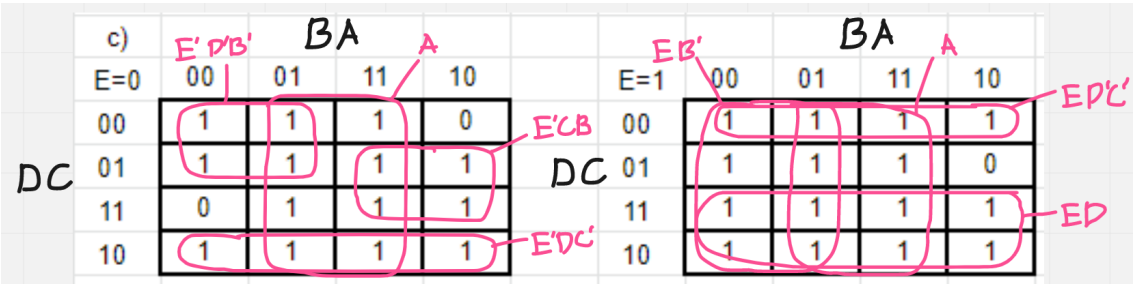


Figure 4. Subcircuit of segment *b* of the Ones 7-segment

(c) SOP of *c* (Ones 7-segment)



Expression	**Theorem/Axiom**
E’D’B’+E’CB+E’DC’+EB’+ED’C’+ED+A	Given
E’(D’B’+CB+DC’)+EB’+ED’C’+ED+A	Distributivity
E’(D’B’+CB+DC’)+E(B’+D’C’+D)+A	Distributivity

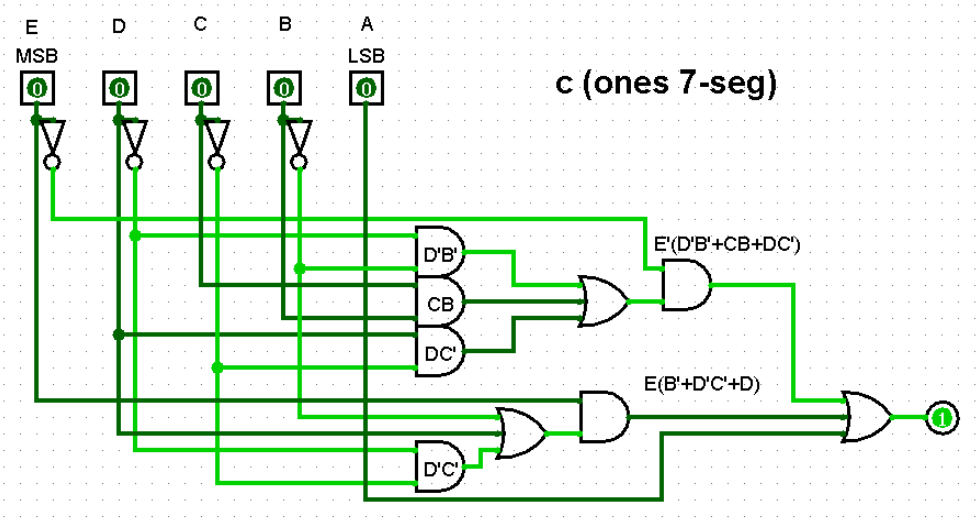
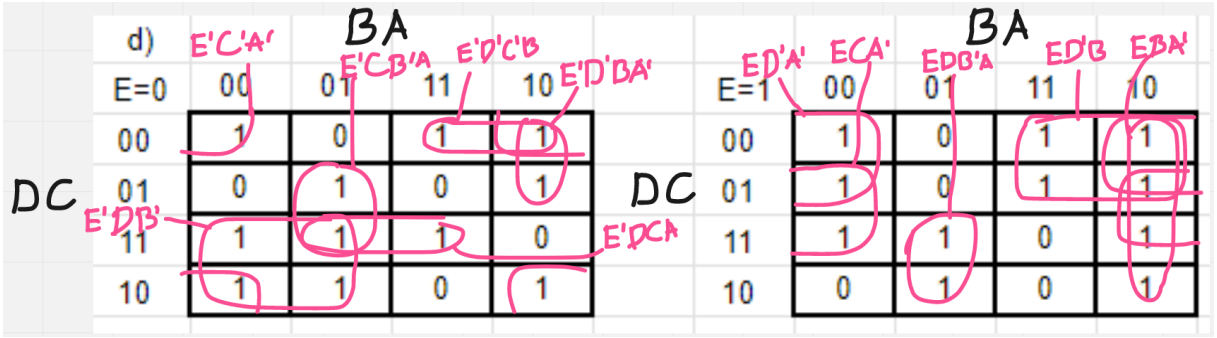


Figure 5. Subcircuit of segment *c* of the Ones 7-segment

(d) SOP of *d* (Ones 7-segment)



Expression	Theorem/Axiom
E'DB'+E'C'A'+E'CB'A+E'D'C'B+E'D'BA'+E'DCA+ED'A'+ECA'+EDB'A+ED'B+EBA'	Given
E'(DB'+C'A'+CB'A+D'C'B+D'BA'+DCA)+ED'A'+ECA'+EDB'A+ED'B+EBA'	Distributivity
E'(DB'+C'A'+CB'A+D'C'B+D'BA'+DCA)+E(D'A'+CA'+DB'A+D'B+BA')	Distributivity

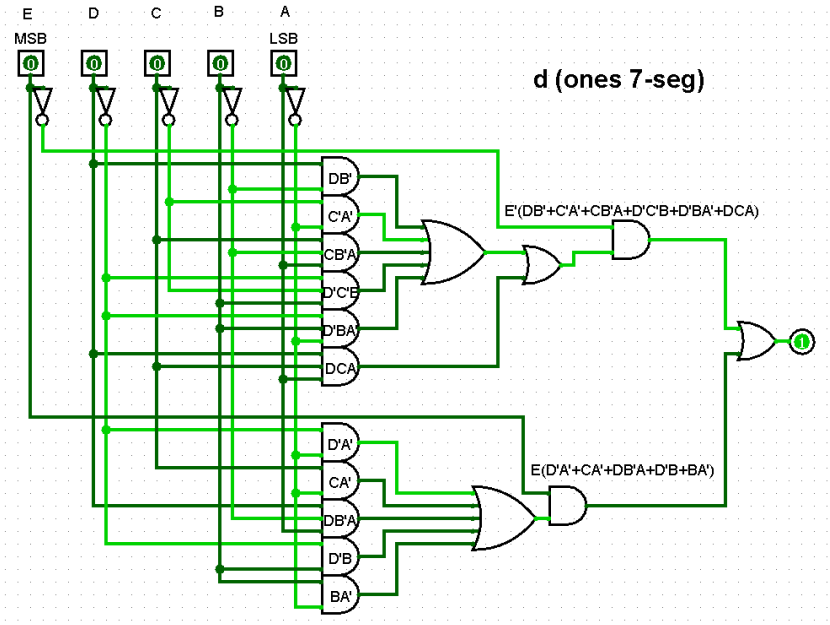
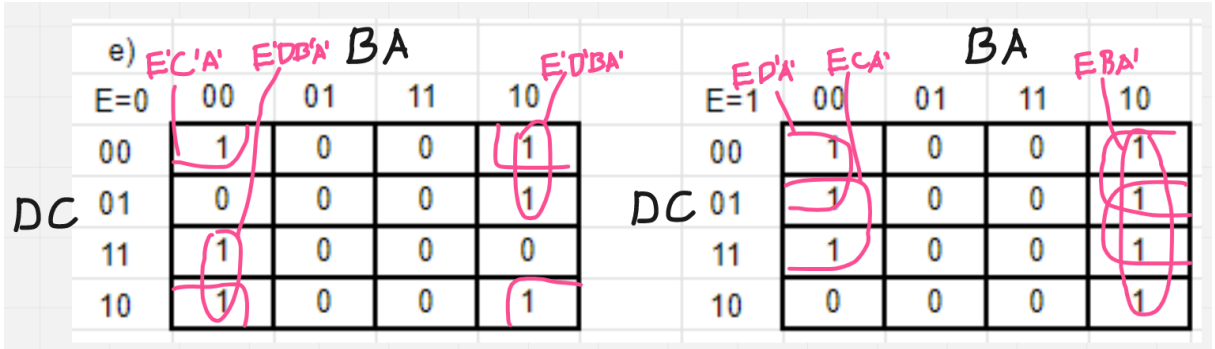


Figure 6. Subcircuit of segment *d* of the Ones 7-segment

(e) SOP of *e* (Ones 7-segment)



Expression	Theorem/Axiom
E’C’A’+E’DB’A’+E’D’BA’+ED’A’+ECA’+EBA’	Given
E’A’(C’+DB’+D’B)+ED’A’+ECA’+EBA’	Distributivity
E’A’(C’+DB’+D’B)+EA’(D’+EC+EB)	Distributivity

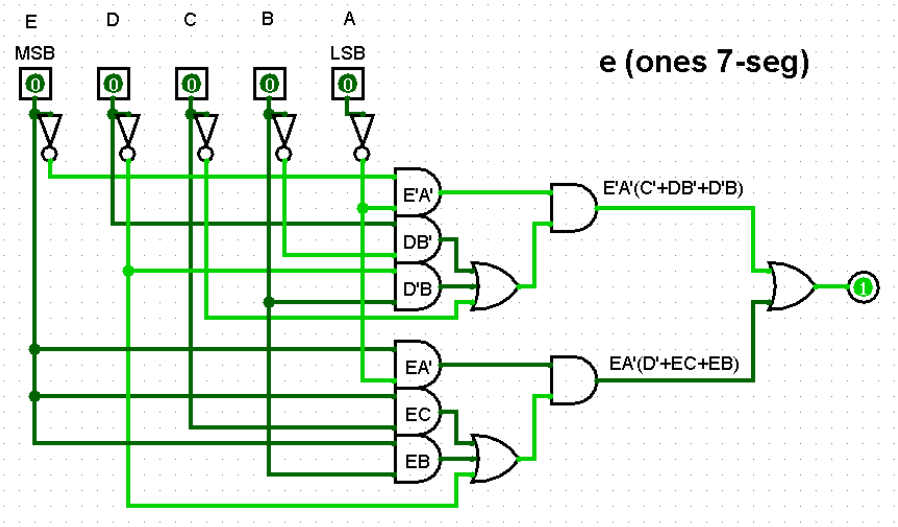
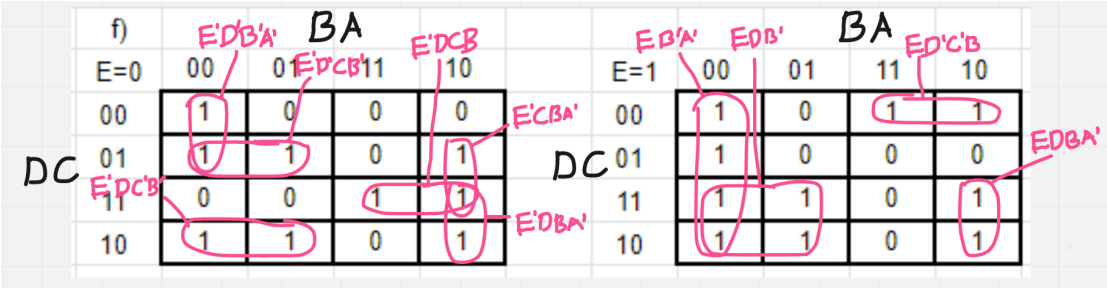


Figure 7. Subcircuit of segment *e* of the Ones 7-segment

(f) SOP of *f* (Ones 7-segment)



Expression	Theorem/Axiom
E’DC’B’+E’D’B’A’+E’D’CB’+E’DCB+E’CBA’+E’DBA’+EB’A’+EDB’+ED’C’B+EDBA’	Given
E’(DC’B’+D’B’A’+D’CB’+DCB+CBA’+DBA’)+EB’A’+EDB’+ED’C’B+EDBA’	Distributivity
E’(DC’B’+D’B’A’+D’CB’+DCB+CBA’+DBA’)+E(B’A’+DB’+D’C’B+DBA’)	Distributivity

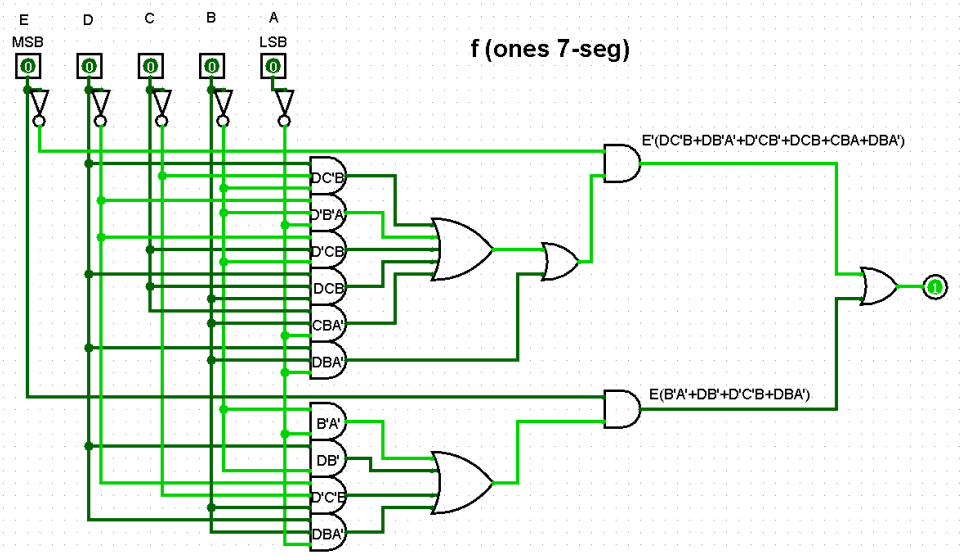
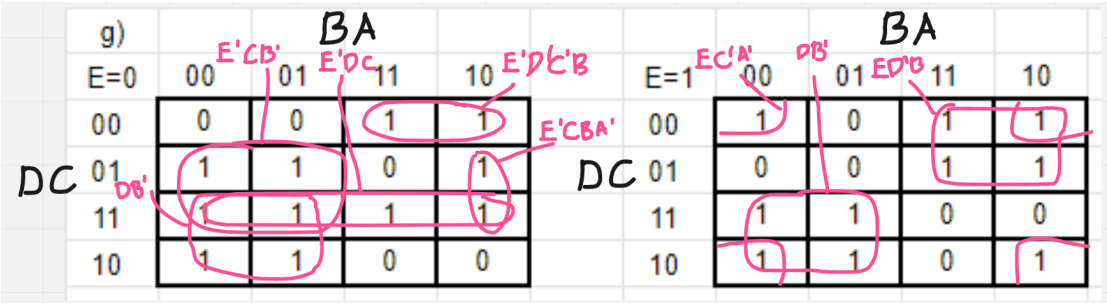


Figure 8. Subcircuit of segment *f* of the Ones 7-segment

(g) SOP of *g* (ones 7-segment)



Expression	Theorem/Axiom
DB'+E'CB'+E'DC+E'D'C'B+E'CBA'+EC'A'+ED'B	Given
DB'+E'(CB'+DC+D'C'B+CBA')+EC'A'+ED'B	Distributivity
DB'+E'(CB'+DC+D'C'B+CBA')+E(C'A'+D'B)	Distributivity

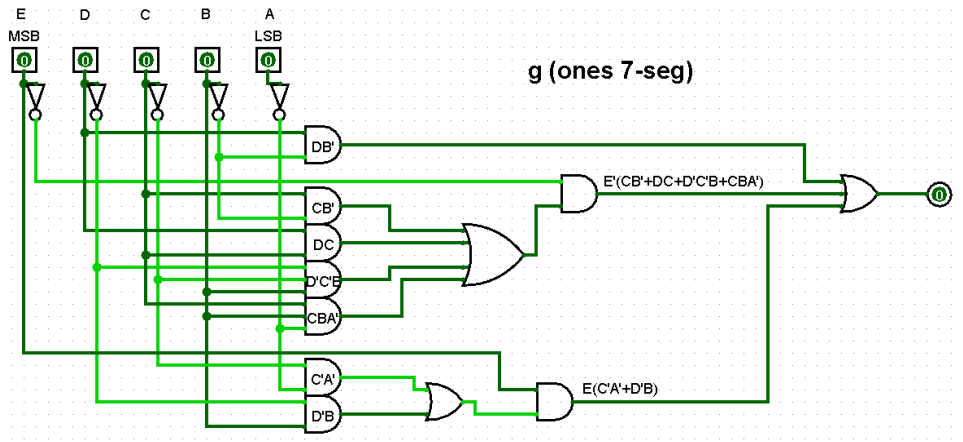


Figure 9. Subcircuit of segment *g* of the Ones 7-segment

Figure 10 shows the subcircuit of the Ones 7-segment comprised of the previously shown subcircuits of each segment.

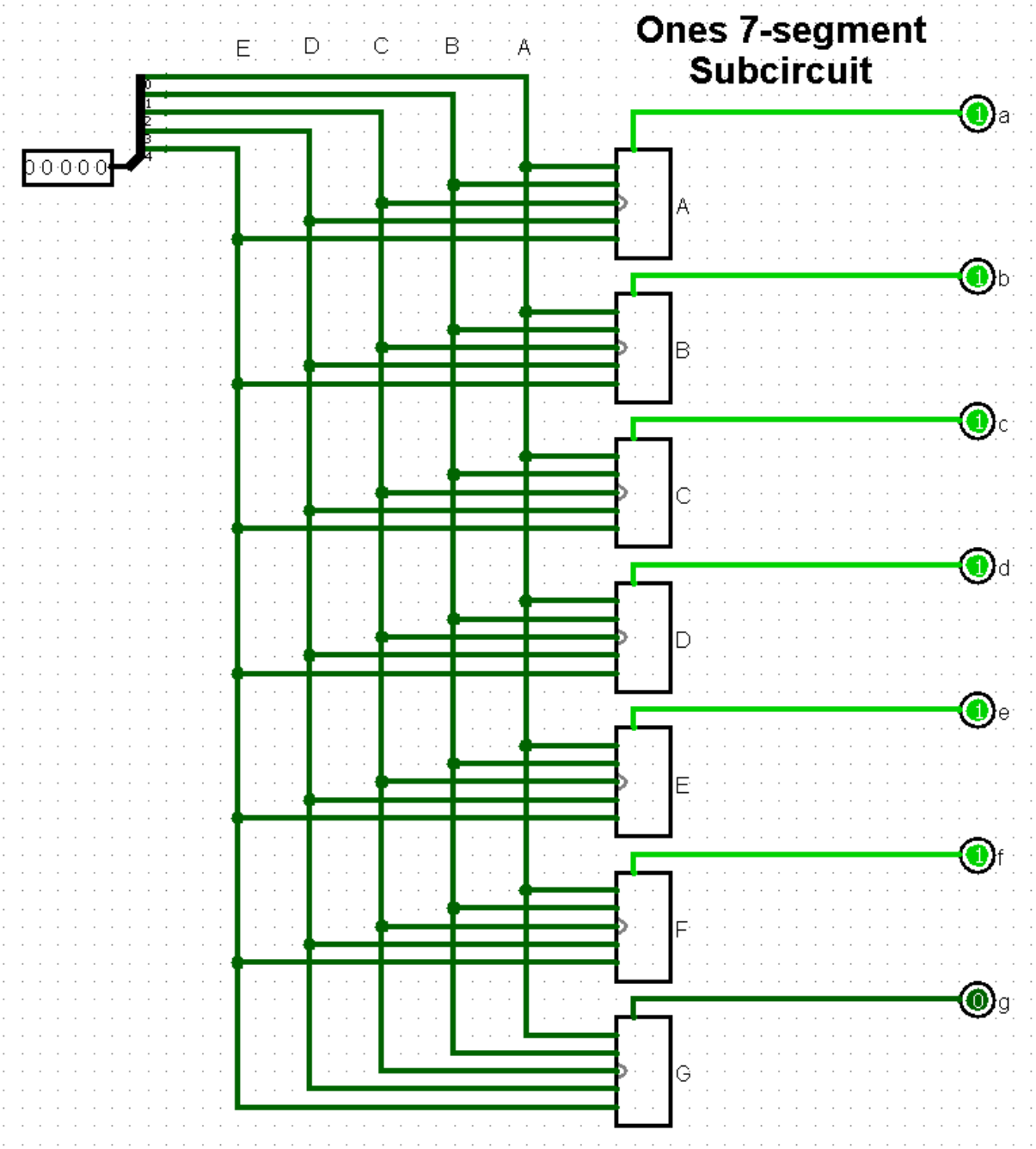
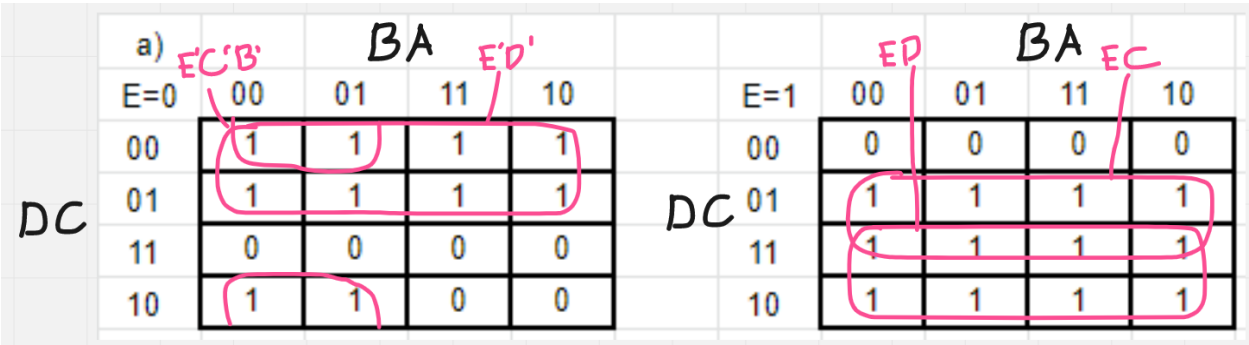


Figure 10. Subcircuit of the Ones 7-segment display

Dec.	E	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	0	1	1	1	1	1	1	1	0
2	0	0	0	1	0	1	1	1	1	1	1	0
3	0	0	0	1	1	1	1	1	1	1	1	0
4	0	0	1	0	0	1	1	1	1	1	1	0
5	0	0	1	0	1	1	1	1	1	1	1	0
6	0	0	1	1	0	1	1	1	1	1	1	0
7	0	0	1	1	1	1	1	1	1	1	1	0
8	0	1	0	0	0	1	1	1	1	1	1	0
9	0	1	0	0	1	1	1	1	1	1	1	0
10	0	1	0	1	0	0	1	1	0	0	0	0
11	0	1	0	1	1	0	1	1	0	0	0	0
12	0	1	1	0	0	0	1	1	0	0	0	0
13	0	1	1	0	1	0	1	1	0	0	0	0
14	0	1	1	1	0	0	1	1	0	0	0	0
15	0	1	1	1	1	0	1	1	0	0	0	0
16	1	0	0	0	0	0	1	1	0	0	0	0
17	1	0	0	0	1	0	1	1	0	0	0	0
18	1	0	0	1	0	0	1	1	0	0	0	0
19	1	0	0	1	1	0	1	1	0	0	0	0
20	1	0	1	0	0	1	1	0	1	1	0	1
21	1	0	1	0	1	1	1	0	1	1	0	1
22	1	0	1	1	0	1	1	0	1	1	0	1
23	1	0	1	1	1	1	1	0	1	1	0	1
24	1	1	0	0	0	1	1	0	1	1	0	1
25	1	1	0	0	1	1	1	0	1	1	0	1
26	1	1	0	1	0	1	1	0	1	1	0	1
27	1	1	0	1	1	1	1	0	1	1	0	1
28	1	1	1	0	0	1	1	0	1	1	0	1
29	1	1	1	0	1	1	1	0	1	1	0	1
30	1	1	1	1	0	1	1	1	1	0	0	1
31	1	1	1	1	1	1	1	1	1	0	0	1

Table 2. Truth table of Tens 7-segment display

(a) SOP of *a* (Tens 7-segment)



Expression	Theorem/Axiom
E’C’B’+E’D’+ED+EC	Given
E’(C’B’+D’)+ED+EC	Distributivity
E’(C’B’+D’)+E(D+C)	Distributivity

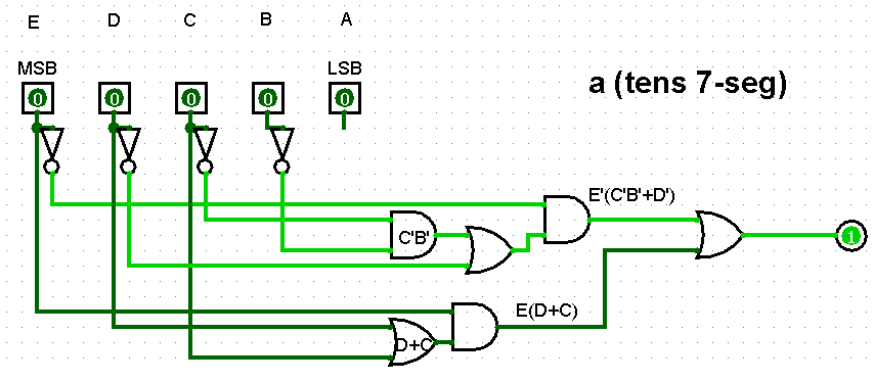
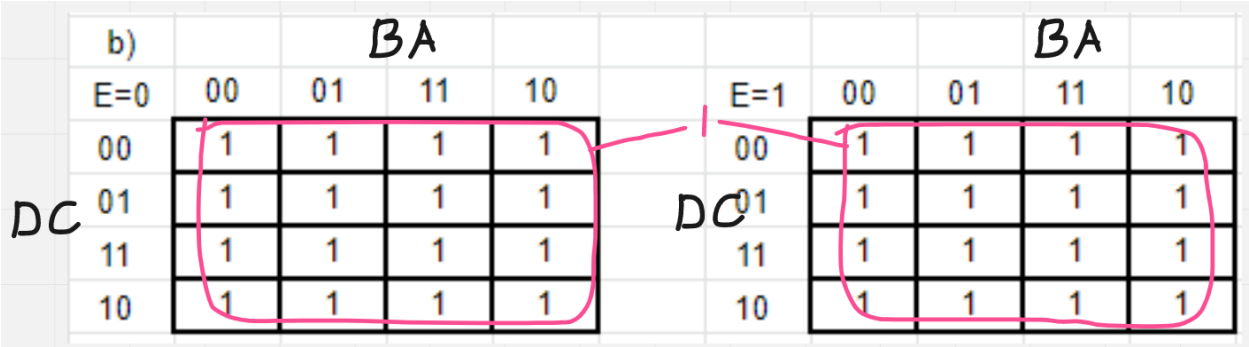


Figure 11. Subcircuit of segment *a* of the Tens 7-segment

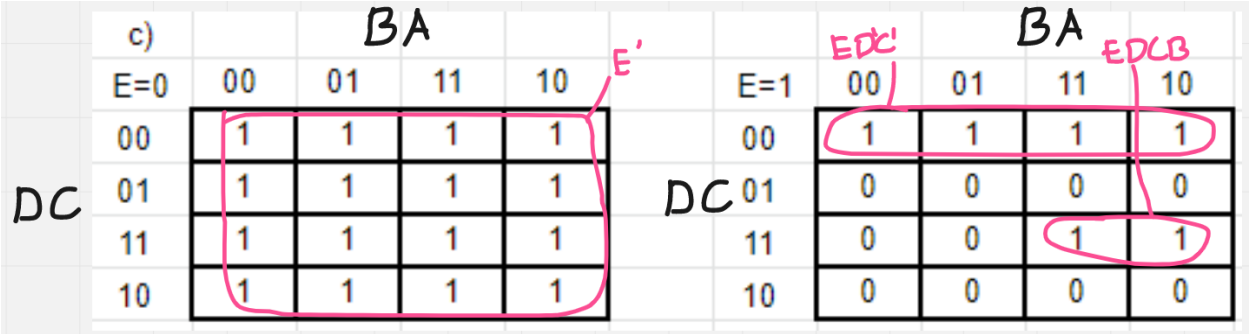
(b) SOP of *b* (Tens 7-segment)



Expression	Theorem/Axiom
1	Given

Since the SOP of b only yields 1, only a constant pin—with 1 as its output—is needed instead of its own subcircuit. See Figure 17 to see how is implemented.

(c) SOP of *c* (Tens 7-segment)



Expression **E'+ED'C'+EDCB**	**Theorem/Axiom** Given

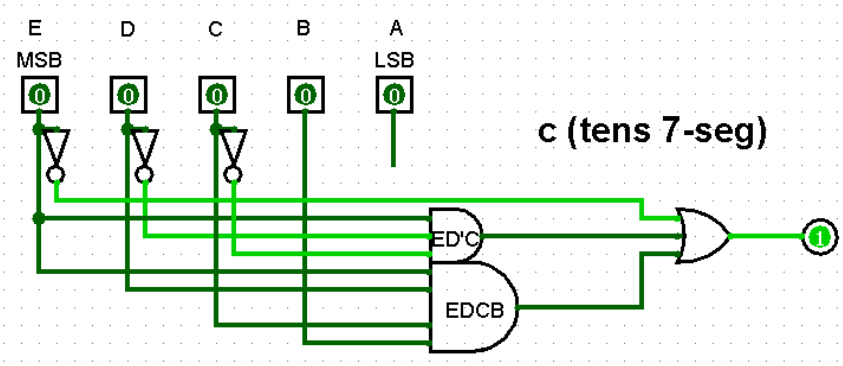
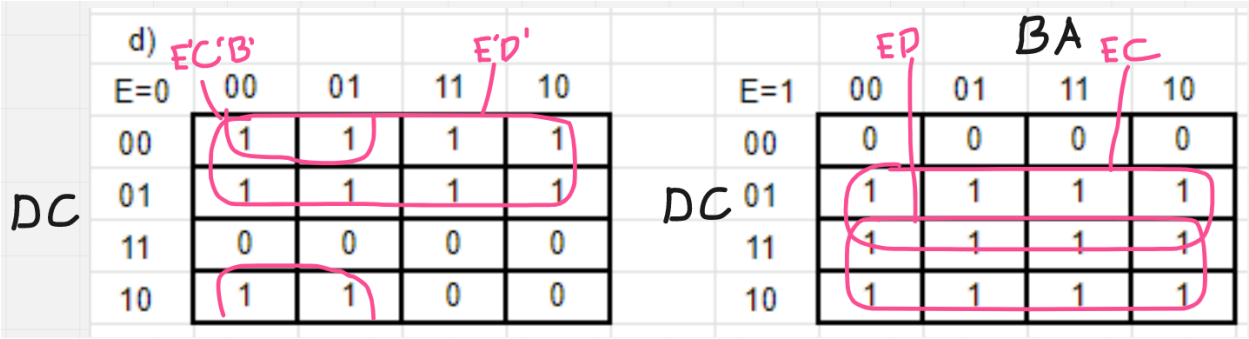


Figure 12. Subcircuit of segment *c* of the Tens 7-segment

(d) SOP of *d* (Tens 7-segment)



Expression E'C'B'+E'D'+ED+EC E'(C'B'+D')+ED+EC **E'(C'B'+D')+E(D+C)**	**Theorem/Axiom** Given Distributivity Distributivity

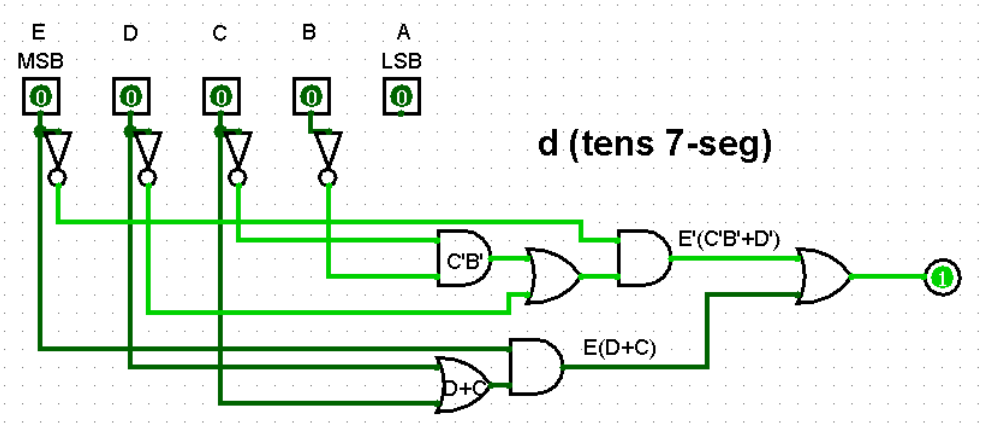


Figure 13. Subcircuit of segment *d* of the Tens 7-segment

(e) SOP of *e* (Tens 7-segment)

e)

DC \ BA	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	0	0	0	0
10	1	1	0	0

E=0 (E'C'B', E'D')

DC \ BA	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	1	1	0	0
10	1	1	1	1

E=1 (EDB', ED'C, EDC')

Expression	Theorem/Axiom
E'C'B'+E'D'+EDB'+ED'C+EDC'	Given
E'(C'B'+D')+EDB'+ED'C+EDC'	Distributivity
E'(C'B'+D')+E(DB'+D'C+DC')	Distributivity

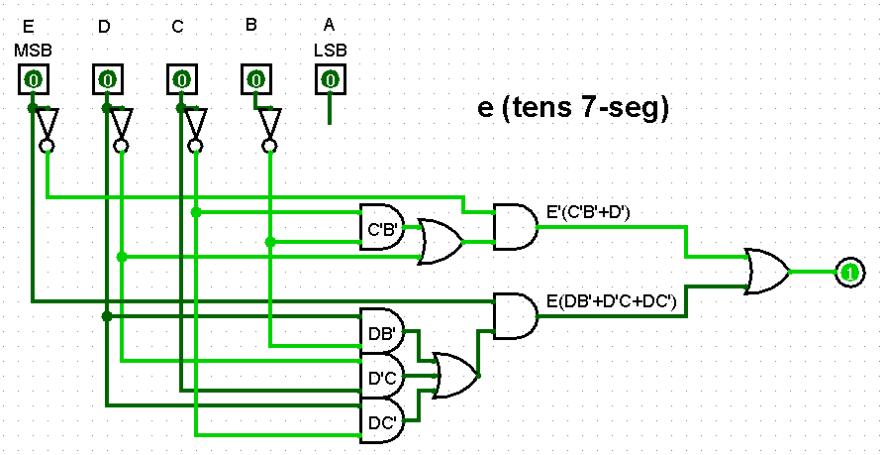


Figure 14. Subcircuit of segment *e* of the Tens 7-segment

(f) SOP of *f* (Tens 7-segment)

f)

DC \ BA	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	0	0	0	0
10	1	1	0	0

E=0 (E'C'B', E'D')

DC \ BA	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	0	0
10	0	0	0	0

E=1

Expression	Theorem/Axiom
E'C'B'+E'D'	Given

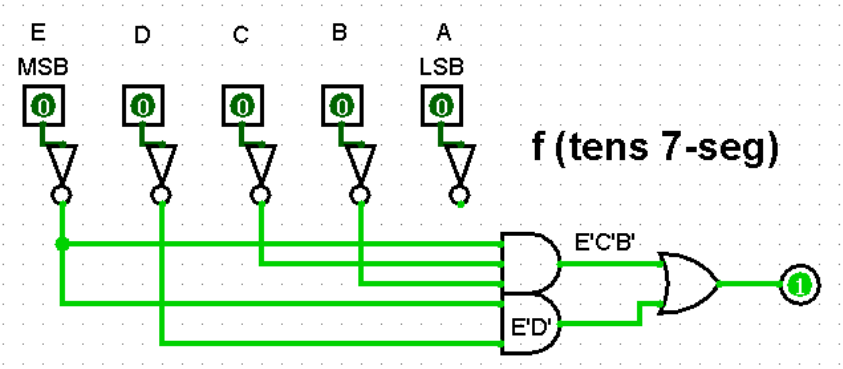


Figure 15. Subcircuit of segment *f* of the Tens 7-segment

(g) SOP of *g* (Tens 7-segment)

g)

DC \ BA	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	0	0
10	0	0	0	0

E=0

E=1

DC \ BA	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

ED

EC

Expression	**Theorem/Axiom**
ED+EC	Given
E(D+C)	Distributivity

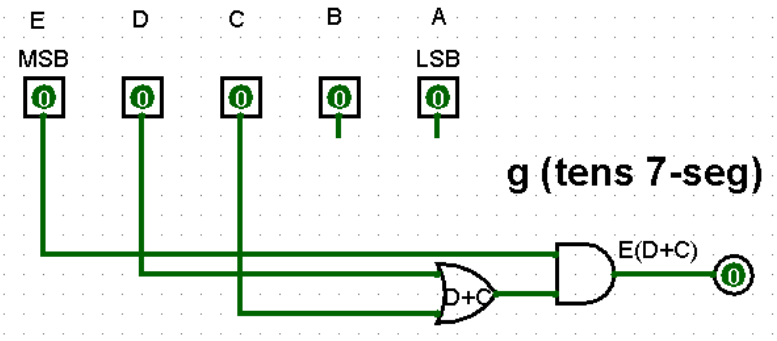


Figure 16. Subcircuit of segment *g* of the Tens 7-segment

Figure 17 shows the subcircuit of the Tens 7-segment comprised of the previously shown subcircuits of each segment. Note that Input *b* of the Tens 7-segment does not have its own subcircuit. This is because segment *b* outputs 1 for all input combinations, and so that we could lessen the number of components needed.

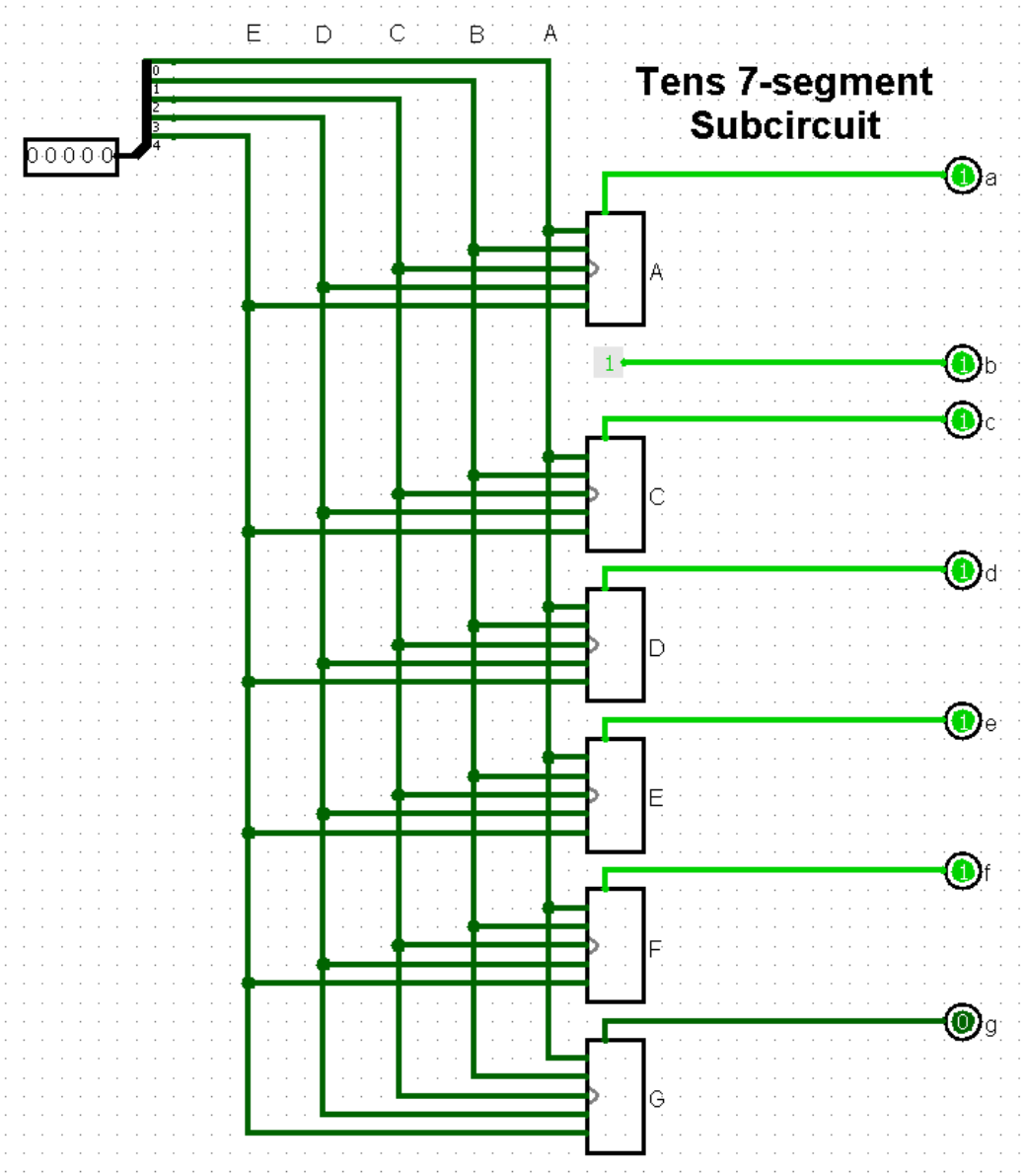


Figure 17. Subcircuit of the Tens 7-segment display

Seen in Figure 18 is the implementation of the subcircuits of the Ones and Tens 7-segment displays connected to a 7-segment display, each, and the Adder component in Figure 1.

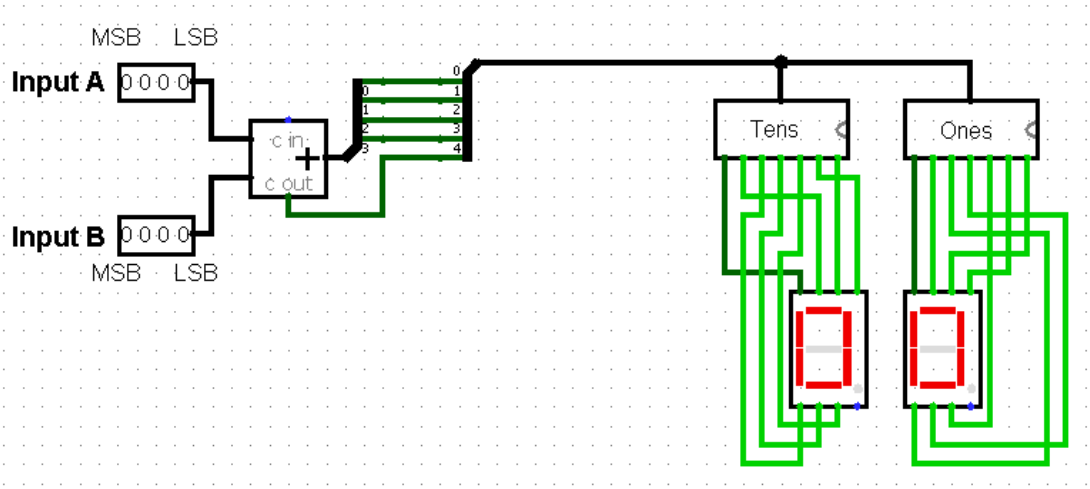


Figure 18. Tens and Ones 7-segment displays connected to the Adder

III. Divisibility

On naming conventions, the leftmost LED that indicates if the sum is divisible by four is labelled *Div by 4.* The middle LED that indicates the sum's divisibility by three is labelled *Div by 3.* Lastly, the rightmost LED that indicates the sum's divisibility by two is labelled *Div by 2.* We shall call the LEDs with the said names for brevity.

a) Divisibility by 2

Note that the binary representation of all even numbers have their least significant bit, the rightmost digit, as zero, e.g., 2: 00010, 14: 01110, 30: 11110.

With this in mind, Div by 2 should be **ON** if the LSB of the sum is 0. This is why a NOT gate connected to the LSB of the output of the Adder is needed for the Div by 2 light to work, as seen in Figure 19. Doing K-maps will not be necessary.

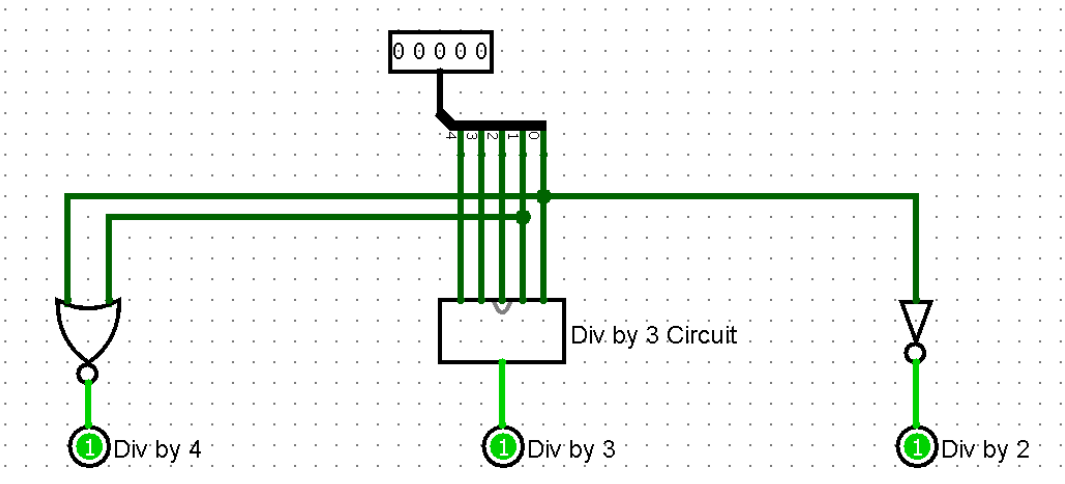


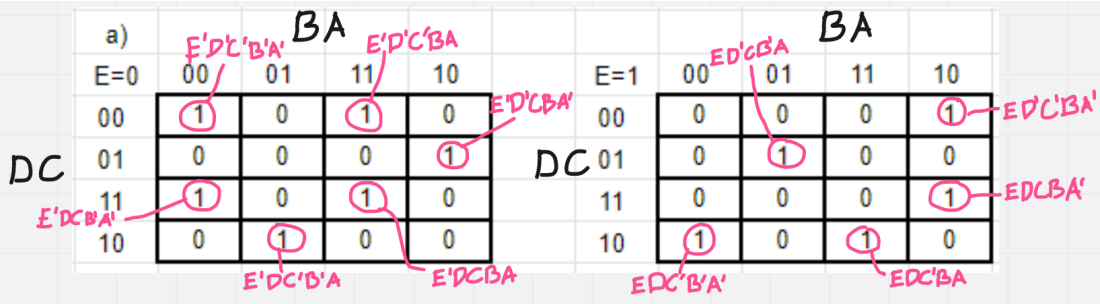
Figure 19. Divisibility Lights Subcircuit

b) Divisibility by 3

Below in Table 3 is the truth table for the Div by 3 light, the K-maps of the subcircuit, and the screenshot of the subcircuit. In a similar manner in the 7-segment displays, this truth table was simplified using K-maps and theorems and axioms to yield a modified minimal SOP expression. This expression is then also implemented in its own subcircuit seen in Figure 20.

Dec.	E	D	C	B	A	Div 3
0	0	0	0	0	0	1
1	0	0	0	0	1	0
2	0	0	0	1	0	0
3	0	0	0	1	1	1
4	0	0	1	0	0	0
5	0	0	1	0	1	0
6	0	0	1	1	0	1
7	0	0	1	1	1	0
8	0	1	0	0	0	0
9	0	1	0	0	1	1
10	0	1	0	1	0	0
11	0	1	0	1	1	0
12	0	1	1	0	0	1
13	0	1	1	0	1	0
14	0	1	1	1	0	0
15	0	1	1	1	1	1
16	1	0	0	0	0	0
17	1	0	0	0	1	0
18	1	0	0	1	0	1
19	1	0	0	1	1	0
20	1	0	1	0	0	0
21	1	0	1	0	1	1
22	1	0	1	1	0	0
23	1	0	1	1	1	0
24	1	1	0	0	0	1
25	1	1	0	0	1	0
26	1	1	0	1	0	0
27	1	1	0	1	1	1
28	1	1	1	0	0	0
29	1	1	1	0	1	0
30	1	1	1	1	0	1
31	1	1	1	1	1	0

Table 3. Truth table of *divisibility by 3* light



Expression	**Theorem/Axiom**
E’DCB’A’+E’D’C’B’A’+E’D’C’BA+E’D’CBA’+E’DCBA+E’DC’B’A+ED’CB’A+ED’C’BA’+EDCBA’+EDC’BA+EDC’B’A’	Given
E’(DCB’A’+D’C’B’A’+D’C’BA+D’CBA’+DCBA+DC’B’A)+ED’CB’A+ED’C’BA’+EDCBA’+EDC’BA+EDC’B’A’	Distributivity
E’(DCB’A’+D’C’B’A’+D’C’BA+D’CBA’+DCBA+DC’B’A)+E(D’CB’A+D’C’BA’+DCBA’+DC’BA+DC’B’A’)	Distributivity

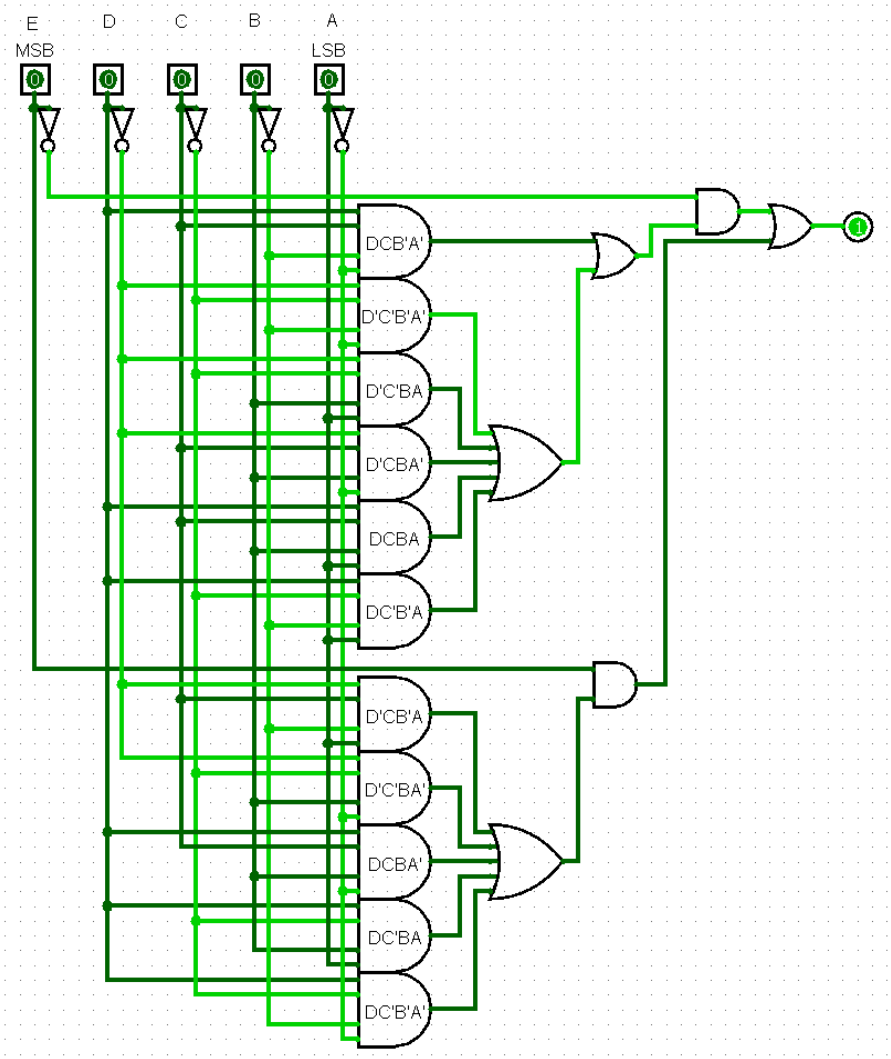


Figure 20. Subcircuit of the Div by 3

c) Divisibility by 4

Also note that the binary representation of all numbers divisible by 4 end with two zeroes, e.g., 4: 00100, 12: 01100, 24: 11000. With this, Div by 4 should be **ON** when the last two binary digits of the sum are both 0, i.e., B'A'.

By De Morgan's laws, we can simplify the expression further into **(A+B)'**.

This can be implemented by connecting one NOR gate to the last two binary digits of the sum, i.e., B and A. The implementation of the NOR gate can be seen in Figure 19. We can also avoid making a truth table and K-maps like in Div by 2.

We connect three LEDs labelled Div by 2, Div by 3, and Div by 4, from left to right, to the subcircuit in Figure 19, labelled Div Lights. Finally, we connect the single input of Div Lights to the output of the adder. Thus, we have the final circuit as seen below.

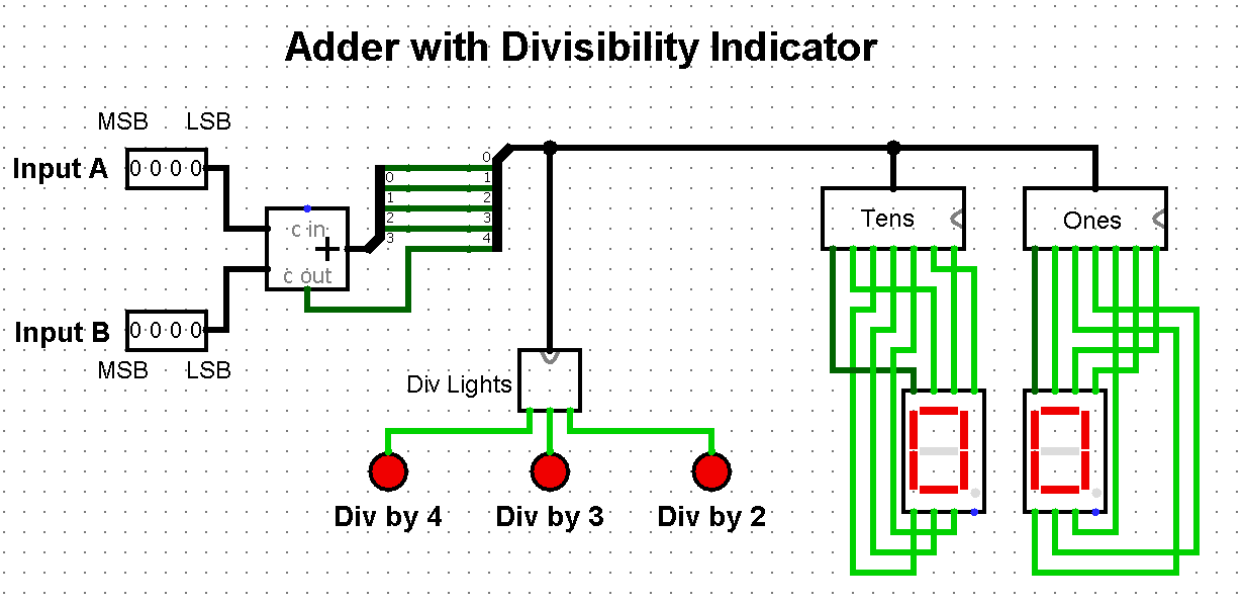


Figure 21. Overview of the circuit