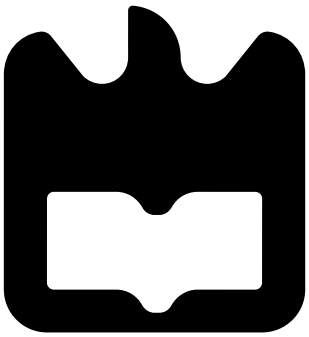

AAD - Assignment 2

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Contents

1 Introduction

This assignment focuses on the implementation and analysis of different accumulator designs in VHDL, including a single-cycle version, a pipelined version, and versions with shift functionality.

2 Implementations

2.1 Single-Cycle Accumulator

As suggested with provided staring point the basic accumulator was implemented in `accumulator_single_cycle.vhd` with the following features:

- Simple write and read ports
- Direct accumulation without pipelining
- Basic addition functionality

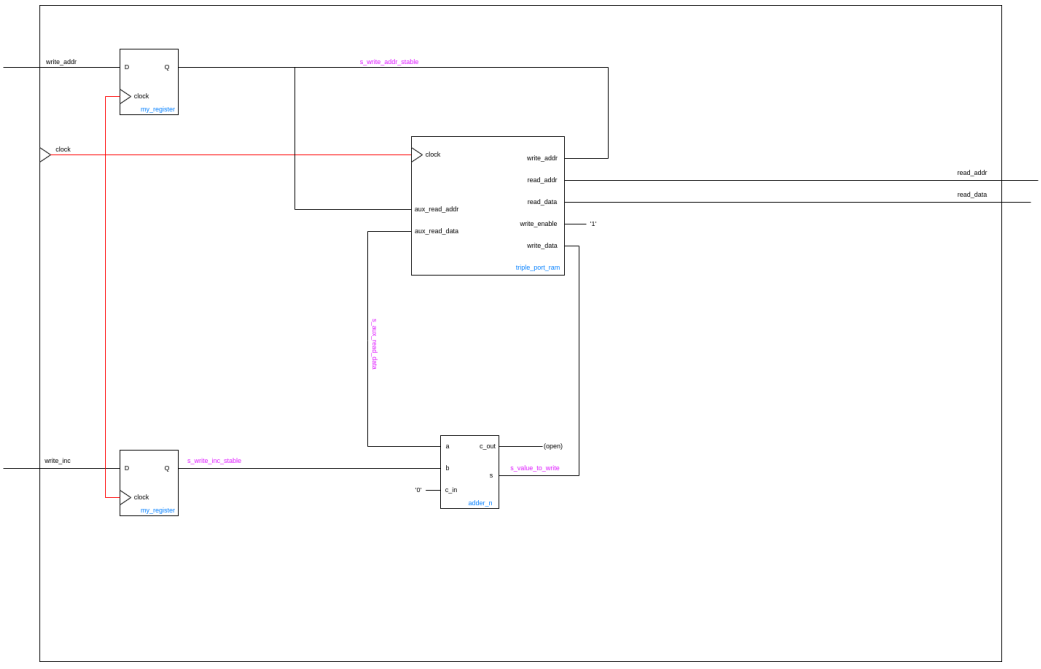

Figure 1: Single-cycle accumulator block diagram

2.2 Pipelined Accumulator

The pipelined version `accumulator_pipeline.vhd` improves upon the basic design by:

- Adding pipeline stages to improve throughput
- Using registers to stabilize signals
- Implementing hazard detection

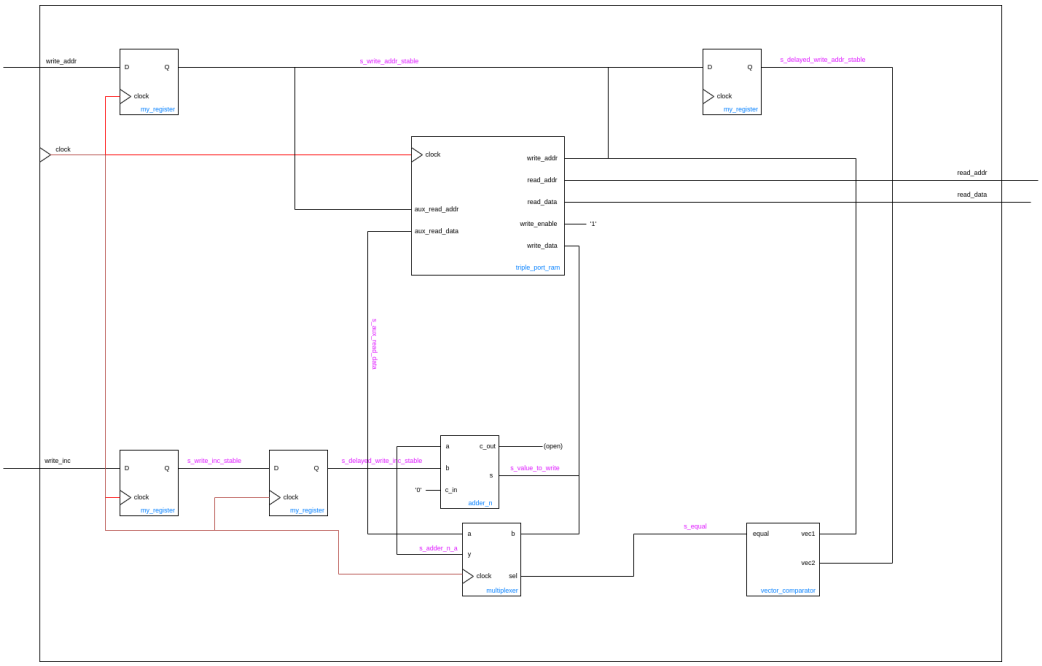

Figure 2: Pipelined accumulator block diagram

2.3 Shift Accumulator

We implemented a version of the accumulator using a barrel Shifter for both the pipelined and single sycle version (`shift_accumulator_pipeline.vhd` and `shift_accumulator.vhd`) both of wich improve upon the basic design by:

- Dynamic shift operations on input data
- Configurable shift amounts

- Integration with the accumulation logic

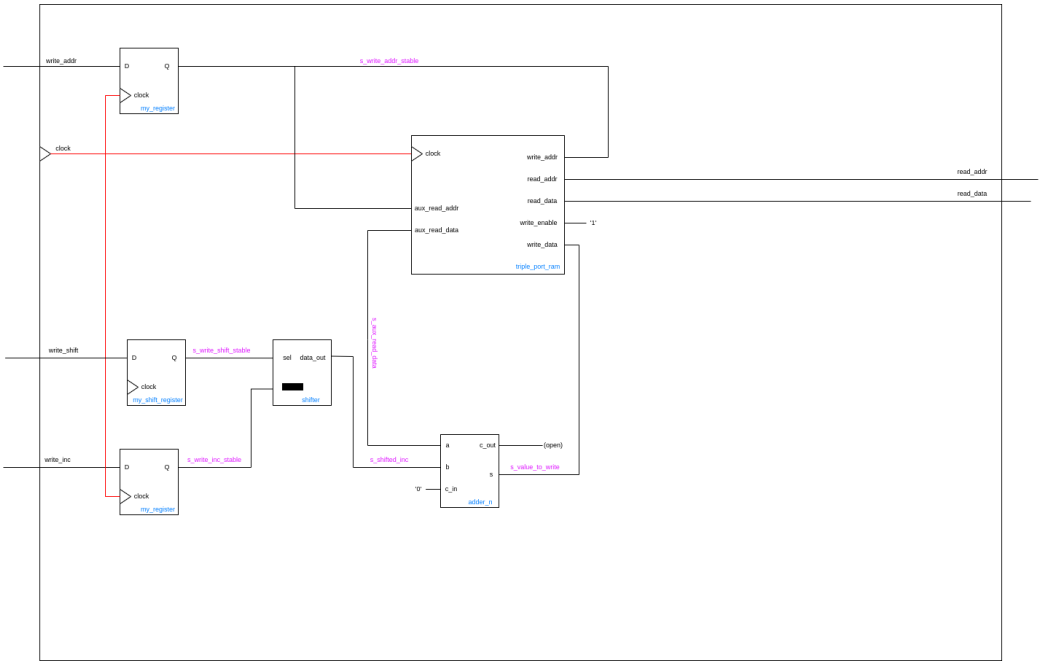

Figure 3: Shift accumulator sigle sycle block diagram

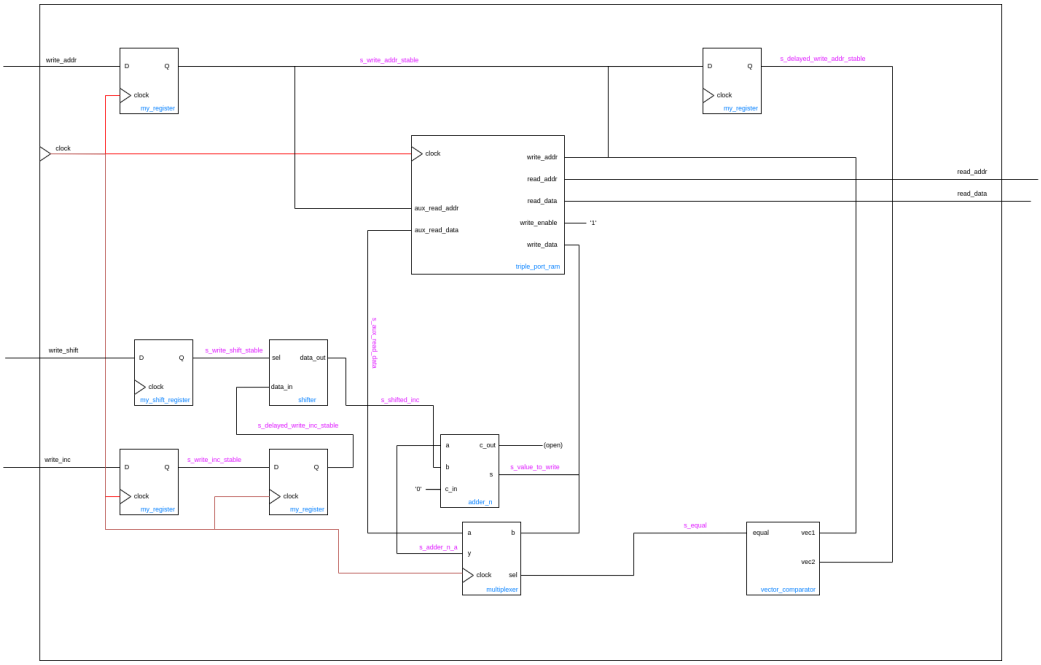

Figure 4: Shift accumulator pipeline block diagram

3 Components

Some of the Components were provided by the professor, and some were implemented by us. Key components used in the designs include:

- Triple Port RAM for memory storage
- Registers for signal stabilization
- Adder N for arithmetic operations
- Shifter for shift operations
- Vector Comparator for address comparison

4 Testing

Testing was performed using:

- GHDL simulator

- VCD waveform generation
- A provisded testbench for the single-cycle accumulator adapted for the pipelined and shift versions

5 Results and Analysis

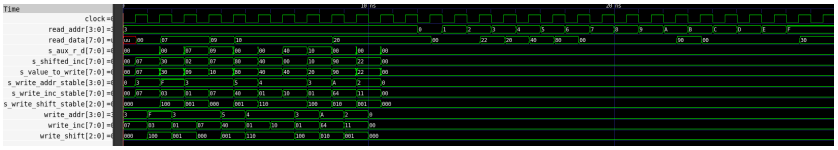

Figure 5: Waveform of the single-cycle accumulator testbench

5 shows the waveform generated by the testbench for the single-cycle accumulator. The testbench was adapted for the pipelined and shift versions, and the results were similar. The shift accumulator was tested with different shift amounts, and the results were as expected.

6 Conclusions