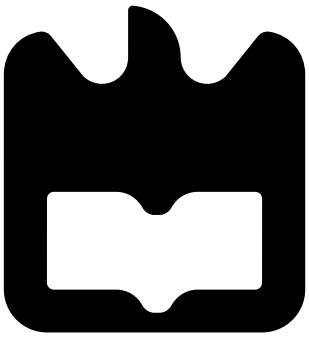

AAD - Assignment 2

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Contents

1 Introduction

This assignment focuses on the implementation and analysis of different accumulator designs in VHDL, including a single-cycle version, a pipelined version, and versions with shift functionality.

2 Implementations

2.1 Single-Cycle Accumulator

The basic accumulator was implemented in `accumulator_single_cycle.vhd` with the following features:

- Simple write and read ports
- Direct accumulation without pipelining
- Basic addition functionality

2.2 Pipelined Accumulator

The pipelined version `accumulator_pipeline.vhd` improves upon the basic design by:

- Adding pipeline stages to improve throughput
- Using registers to stabilize signals
- Implementing hazard detection

2.3 Shift Accumulator

We implemented a version of the accumulator using a barrel Shifter for both the pipelined and single sycle version (`shift_accumulator_pipeline.vhd` and `shift_accumulator.vhd`) both of wich improve upon the basic design by:

- Dynamic shift operations on input data
- Configurable shift amounts
- Integration with the accumulation logic

3 Components

Key components used in the designs include:

- Triple Port RAM for memory storage
- Registers for signal stabilization
- Adder N for arithmetic operations
- Shifter for shift operations
- Vector Comparator for address comparison

4 Testing

Testing was performed using:

- GHDL simulator
- VCD waveform generation
- Comprehensive testbenches for each version

5 Results and Analysis

Compare the performance and characteristics of each implementation:

- Single-cycle vs Pipelined timing
- Impact of shift functionality
- Resource utilization
- Critical path analysis

6 Conclusions