Exibição, em um monitor VGA, de canais filtrados

Equipe

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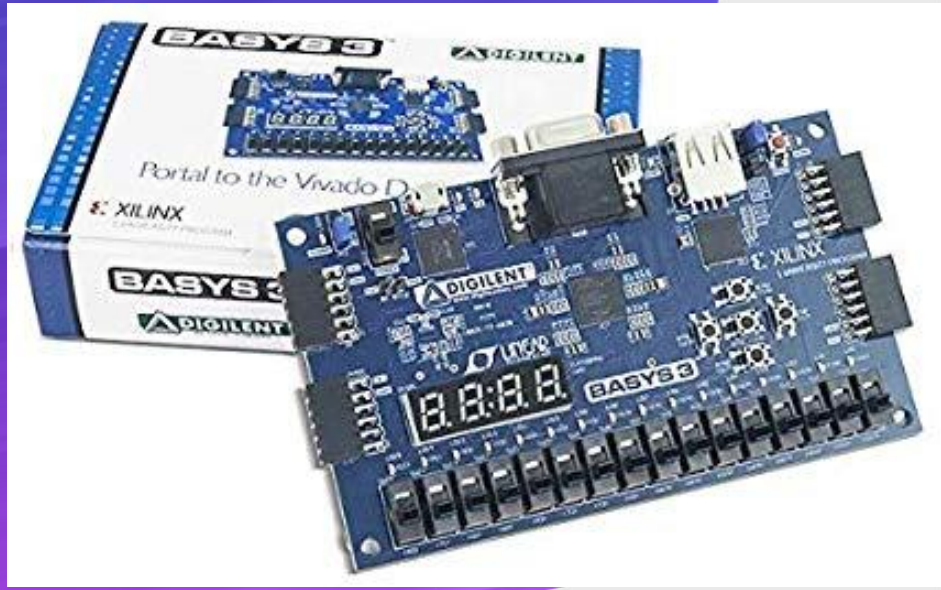
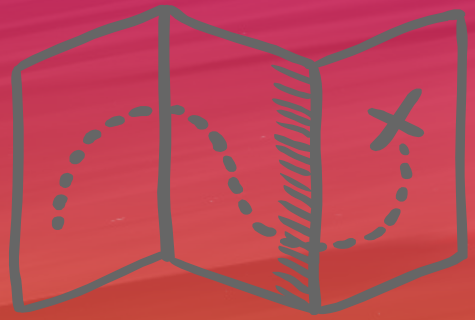
Materiais utilizados

Módulo VGA monitor

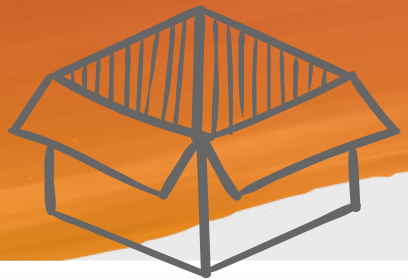
Placa de desenvolvimento FPGA BASYS3

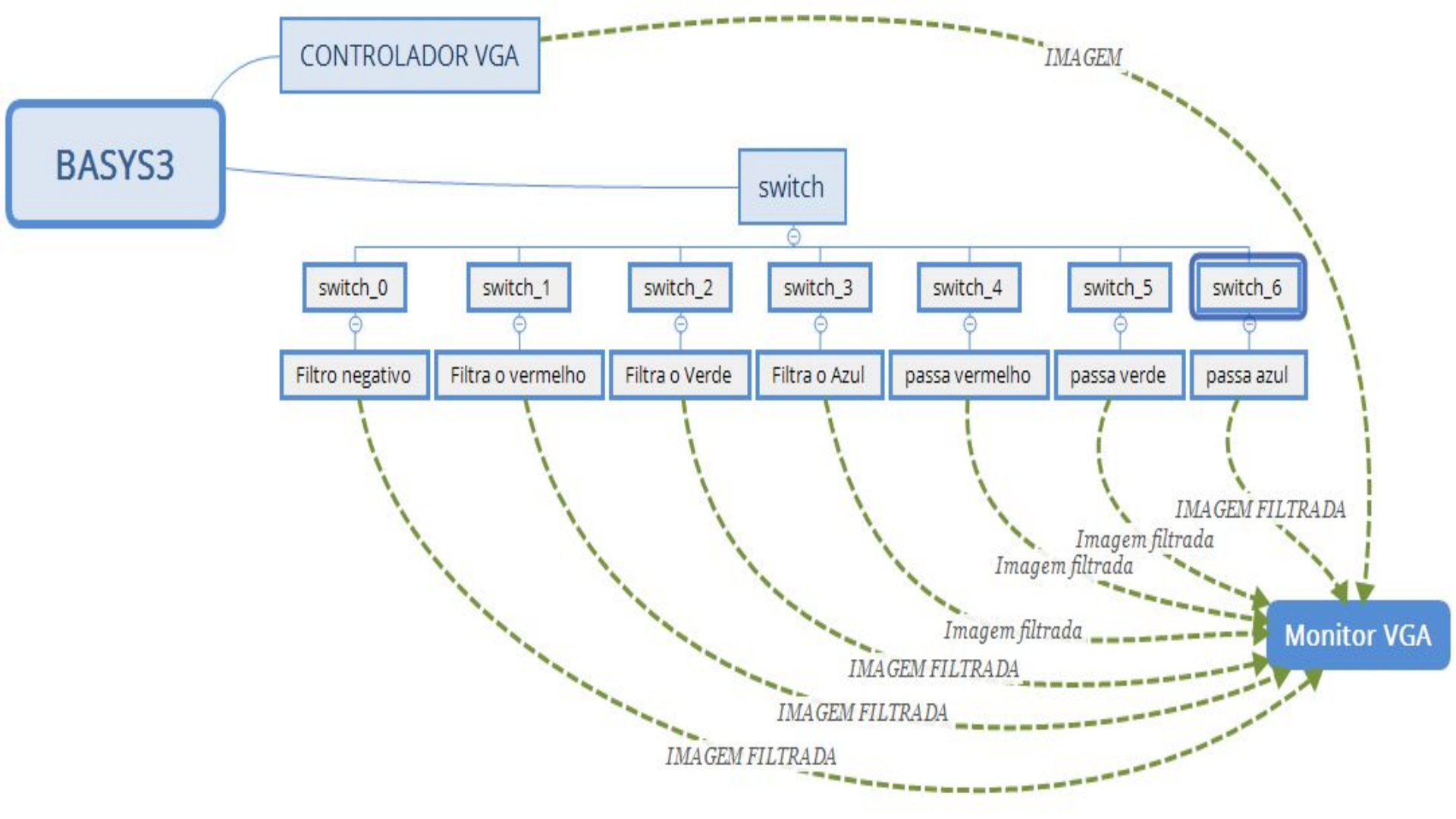


“Noites em claro”



O projeto




BASYS3
CONTROLADOR VGA
switch
switch_0
switch_1
switch_2
switch_3
switch_4
switch_5
switch_6
Filtro negativo
Filtra o vermelho
Filtra o Verde
Filtra o Azul
passa vermelho
passa verde
passa azul
IMAGEM
IMAGEM FILTRADA
Imagem filtrada
Imagem filtrada
Imagem filtrada
IMAGEM FILTRADA
IMAGEM FILTRADA
IMAGEM FILTRADA
Monitor VGA

Demonstração

RESULTADOS

WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs
							83	50	48.00
1.571	0.000	0.092	0.000	0.000	0.099	0	107	54	48.00

Timing — **Setup** | Hold | Pulse Width

Worst Negative Slack (WNS):	1.571 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	933

Implemented Timing Report

Power — **Summary** | On-Chip

Total On-Chip Power:	**0.099 W**
Junction Temperature:	**25,5 °C**
Thermal Margin:	59,5 °C (11,8 W)
Effective ϑJA:	5,0 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Implemented Power Report

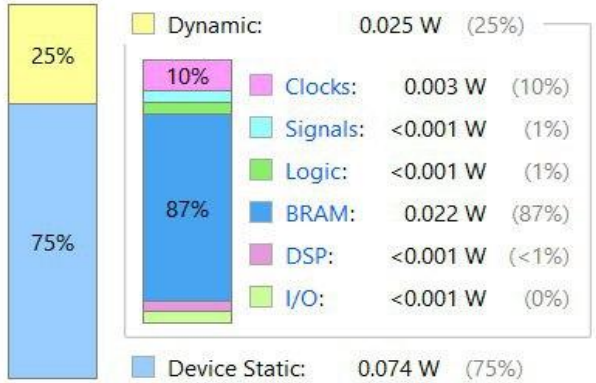
RESULTADOS

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.099 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25,5°C**
Thermal Margin:	59,5°C (11,8 W)
Effective ϑJA:	5,0°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

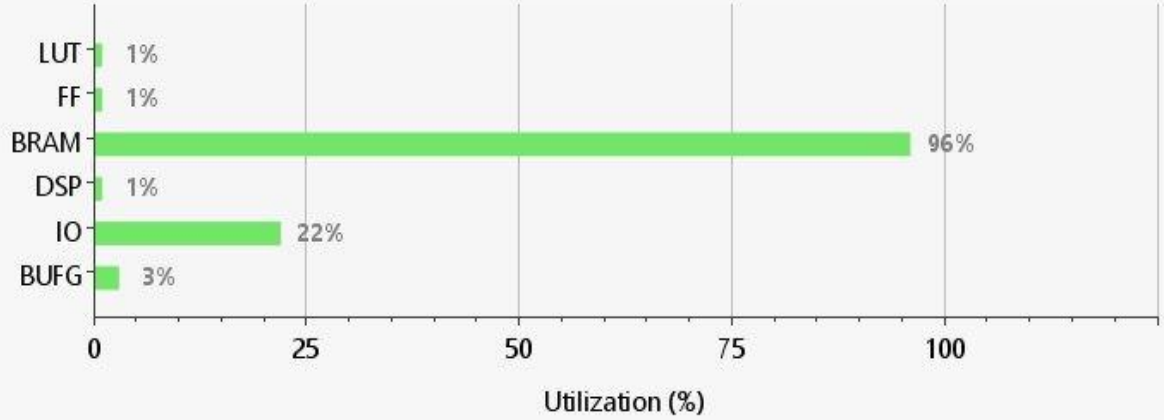
Launch Power Constraint Advisor to find and fix

On-Chip Power



Utilization Post-Synthesis | **Post-Implementation**

Graph | Table



Obrigado