Politecnico di Torino

Microelectronic Systems

DLX Microprocessor: Design & Development

Final Project Report

Master degree in Computer Engineering

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Group 40

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Contents

CHAPTER 1

Introduction

1.1 Architecture

The DLX (DELUXE) is a fully pipelined RISC processor based on the Harvard Architecture, i.e., it relies on two different memories for instructions and data, allowing simultaneous instruction-fetching and data transactions, as shown in Figure 1.1.

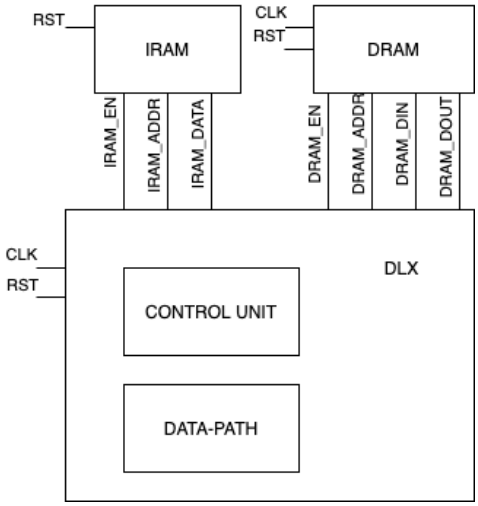

Figure 1.1: DLX block diagram.

The provided IRAM was modified to implement a ROM memory based on a VHDL description provided by Intel FPGA Support Resources. The memory behavior was adjusted to this project testbench by including a procedure that reads the file *"test.asm.mem"*, filling the memory array with its content.

The DRAM was also based on a Single-Port RAM VHDL description provided by Intel FPGA Support Resources, also modified to deal with external files.

The top-level entity consists of the DLX microprocessor itself, which in turn instantiates two components, the Control Unit (CU) and Data-path (DP). The CU in particular had to be implemented in one of three different design models: hardwired, fine-state machine, and micro-programmed. Further details on those components would be discussed in the following sections.

1.2 Implementation

The mandatory specifications for this project consisted of a VHDL description of a DLX Basic version able to run a small sub-set of instructions, followed by its synthesis and physical design.

Moreover, some optional specifications were suggested to achieve a DLX Pro version. The features added by the author are listed below.

- **Extended Instruction Set:** addu, addui, jalr, jr, lb, lbu, lhi, lhu, sb, seq, seqi, sgeu, sgeui, sgt, sgti, sgtu, sgtui, slt, slti, sltu, sltui, sra, srai, subu, subui, mult;
- **Optimized ALU:** Pentium4 adder/subtractor, UltraSPARC T2 3-level Shifter, UltraSPARC T2 Logic Unit using 2-level NAND gates, Multi-purpose Comparator, Zero Detector, and Booth Multiplier. Power optimization by reducing switching activity through state assignment of all blocks;
- **Forwarding Unit:** data hazard control;
- **Clock-Gating:** Register File and Generic Registers gated for power optimization;
- **Scripts:** Scripts were used during design, simulation, and synthesis for automating such processes.

CHAPTER 2

Control Unit

The CU is the component responsible for managing the whole pipeline. Each time the Program Counter (PC) is incremented, a new instruction is fetched from the IRAM by reading the address pointed by the PC value. The newly fetched instruction is then stored into the Instruction Register (IR) before entering the CU for decoding.

The hard-wired design style was chosen when describing the CU behavior due to its simplicity and liability. Two Look-up-Tables were used in the combinational logic that asserts a 23-bit Control Word (CW) signal and the ALU opcode. In each stage of the pipeline (FETCH, DECODE, EXECUTE, MEMORY ACCESS, and WRITE BACK) a portion of the CW is delivered to the data-path, as demonstrated in Figure 2.1.

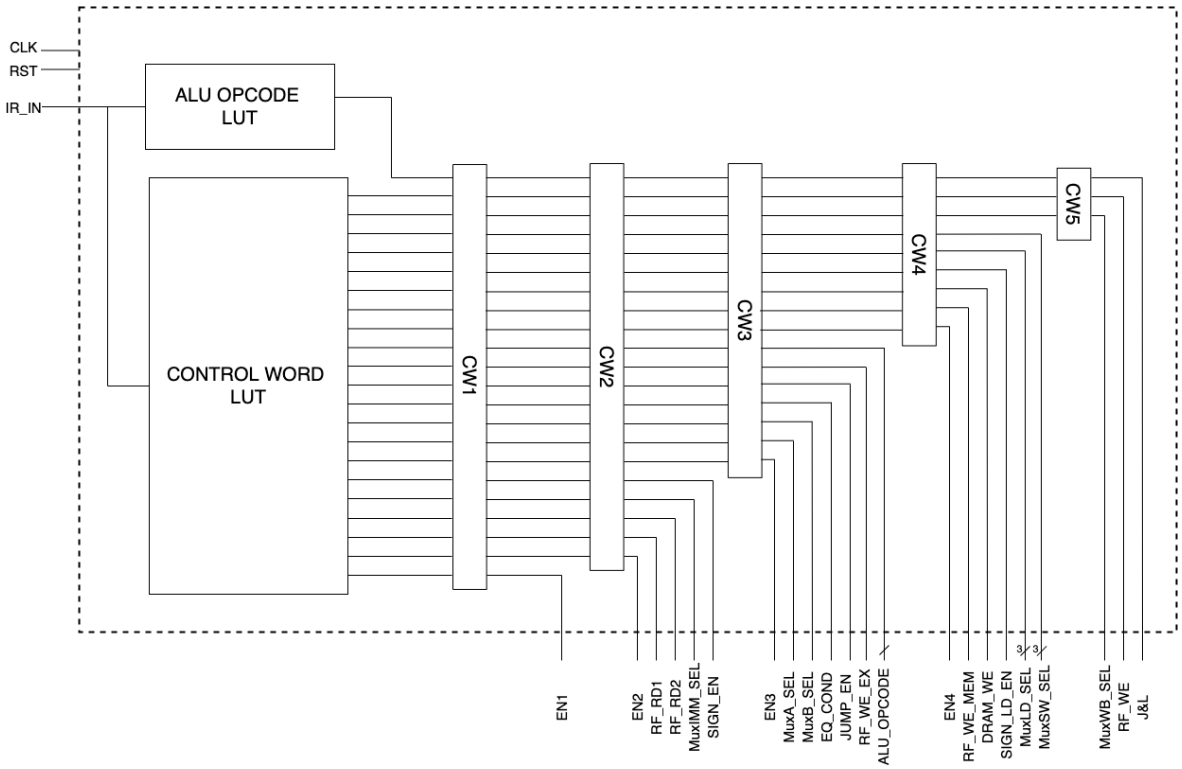

Figure 2.1: Harwired Control Unit.

The instruction set can be divided into three categories, register-to-register (R-type), immediate

operations (I-type), and branching instructions (J-type). The instruction encoding changes according to the instruction type:

- **R-Type:** 6-bit OPCODE, 5-bit operand A (RS1), 5-bit operand B (RS2), 5-bit destination register (RD), and 11-bit FUNC;
- **I-Type:** 6-bit OPCODE, 5-bit operand A (RS1), 5-bit destination register (RD), and 16-bit immediate;
- **J-Type:** 6-bit OPCODE, 26-bit immediate.

Whenever a new instruction is received it is split into an OPCODE field used by both LUTs, and the FUNC field for determining the ALU operation. An implicit encoding for the ALU opcode signal was chosen as it provides better readability during the coding phase, as well as during testbench. The fragment of code below depicts this kind of signal assignment, extracted from the *000-globals.vhd* file.

```
type aluOp is (nopOp, addOp, subOp, andOp, orOp, xorOp, sllOp, srlOp,
    sraOp, multOp, lhiOp, gtOp, geOp, ltOp, leOp, eqOp, neOp, gtUOp,
    geUOp, ltUOp, leUOp);
```

New instructions are fetched at each clock cycle, entering the pipeline in order. Therefore, the DLX microprocessor can execute up to 5 instructions simultaneously, each allocated to one of the pipeline stages. The control word is shifted by one position at each positive edge of the clock cycle to ensure that the portion of control signals related to a certain stage is delivered to the data-path in the correct order. This behavior is highlighted in Figure 2.1. In the following, a brief description of each one of the control signals is provided.

- **EN1:** enable signal for the registers involved in the FETCH stage, and the IRAM also.
- **EN2:** enable signal for the Register File (RF) and the remaining registers involved in the DECODE stage.
- **RF_RD1:** RF read enable source register of operand A.
- **RF_RD2:** RF read enable source register of operand B.
- **MuxIMM_SEL:** select signal for the immediate multiplexer, whose assertion value depends on the type of instruction.
- **SIGN_EN:** asserted when instruction implies an operation over signed immediate, the 26-bit immediate is always signed.
- **EN3:** enable signal for the registers involved in the EXECUTE stage.
- **MuxA_SEL:** select signal for choosing between register A and NPC.
- **MuxB_SEL:** select signal for choosing between register B and immediate register.
- **EQ_COND:** asserted when branching instruction requires equality comparison.
- **JUMP_EN:** asserted whenever there is a branch instruction.
- **RF_WE3:** RF write enable signal during EXECUTE stage fed to the forwarding unit.
- **ALU_OPCODE:** ALU operation code.
- **EN4:** enable signal for the registers involved in the MEMORY ACCESS stage, as well as the DRAM.

- **RF_WE4:** RF write enable signal during MEMORY ACCESS stage fed to the forwarding unit.
- **DRAM_WE:** DRAM write enable signal.
- **SIGN_LD_EN:** asserted when loading a signed half-word or byte.
- **MuxLD_SEL:** select signal for choosing between the different lengths of data in LD instructions.
- **MuxSW_SEL:** select signal for choosing between the different lengths of data in LD instructions.
- **MuxWB_SEL:** select signal that determines the source of the data to be written into the RF.
- **RF_WE:** RF write enable signal during WRITE-BACK stage fed to forwarding unit also.
- **JUMP_LINK:** asserted when branching instruction requires writing into R31 a return address.

CHAPTER 3

Data-path

The data-path is the most critical unit of a microprocessor as it deals with the general data processing. Figure 3.1 depicts the internal architecture of this component. External components such as IRAM and DRAM were placed inside the data-path in that figure for simplicity. Additionally, CU signals were highlighted in red, those extracted from the instruction fields are in blue, and in green are the signals and components used by the forwarding unit.

The data-path is organized in five different stages, given as it follows:

- **INSTRUCTION FETCH (IF):** the PC register points to the address corresponding to the instruction that must be fetched from the IRAM with its subsequent storage in the IR register. The address to the next instruction is then computed and saved into the NPC register.
- **INSTRUCTION DECODE (ID):** source and destination addresses are then extracted according to the type of instruction currently executing and the corresponding signals for accessing the register file are asserted. In particular, in the case of an I-type instruction, the 16-bit immediate is extracted and sign-extended to a 32-bit word, with J-type instructions the 26-bit target address is extracted and sign-extended instead. After reading the operands from RF or extracting the immediate values, those are delivered to their corresponding registers for the next stage.
- **EXECUTION (EX):** the ALU performs the specified operation over the provided operands. These values may come from the previous or following stages according to the results obtained in the forwarding unit. Decisions regarding branch conditions also take place in this stage.
- **MEMORY ACCESS (MEM):** the DRAM is accessed if required by the instruction. In the case of a store the memory is accessed in write mode, the address to be written might be either the ALU result from the previous stage or the value currently in the following WRITE-BACK stage according to the forwarding unit decision. The data incoming is the value read from the register source B data-aligned to a word, half-word, or byte. In case of a load the memory is accessed in reading mode and the data outgoing is stored in the LMD register before going through its data-alignment and subsequent write-back to the destination address.
- **WRITE-BACK (WB):** in this last stage the either the ALU result or the data read from the memory are eventually written into the register file. In case of a jump and link instruction, such as JAL, a return address consisting of the PC value incremented by 8, i.e., the NPC value incremented by 4 is stored into the R31 register instead.

The following section will discuss some details regarding the internal functional units that compose the ALU, as well as a brief explanation of the Forwarding Unit behavior. Comments over the register

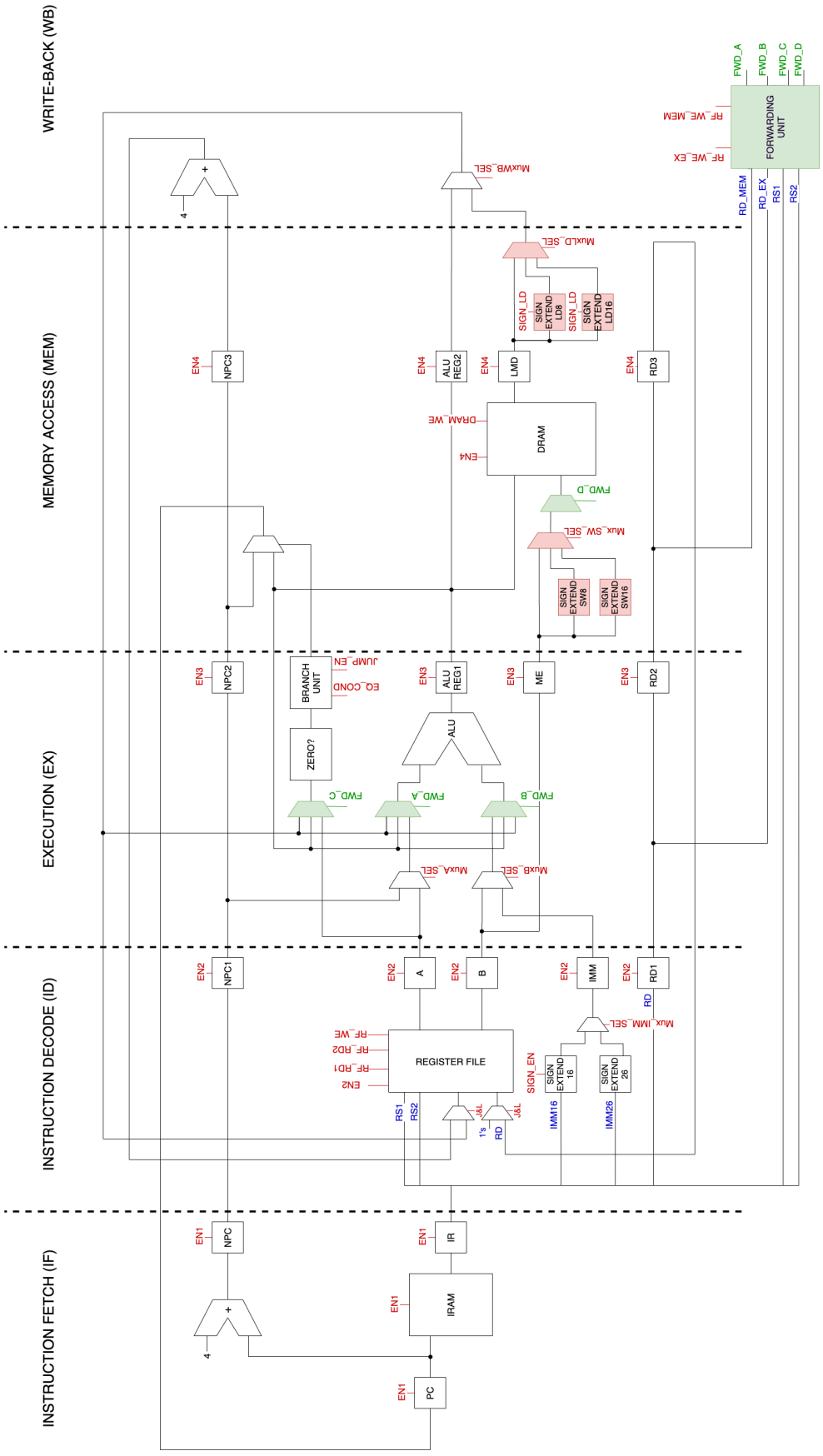

Figure 3.1: Fully pipelined Data-path.

file will be skipped as it was described as a regular 32-bit width and 32-register length dual-port synchronous read/write component. The branch unit will be skipped also as it consists of a simple static branch prediction implementation, i.e., jumping instructions are predicted to be taken always.

3.1 ALU

The ALU depicted in Figure 3.2 is the core of the execution stage able to perform arithmetic and bitwise operations on both sign and unsigned integer numbers. It takes as input the two operands the signal encodes the operation to be performed. Both operands go through a decoder omitted in that figure. This approach aims to reduce the switching activity of those units, hence, decreasing power consumption due to Joule Effect by staging the operands and asserting only the inputs of those functional units involved in a particular operation.

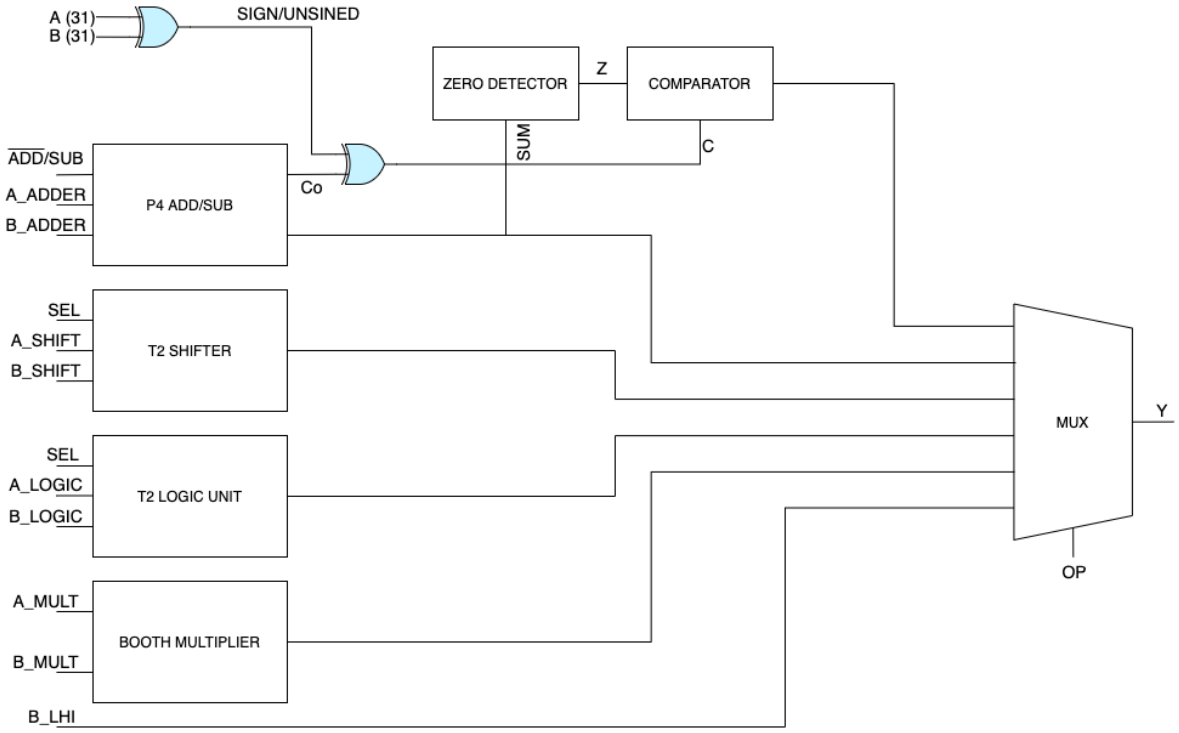

Figure 3.2: ALU block.

The functional units added to the are the following:

- Pentium4 Adder/Subtractor;
- UltraSPARC T2 3-level Shifter;
- UltraSPARC T2 Logic Unit;
- Signed/Unsigned Multi-purpose Comparator;
- Zero Detector;
- Booth Multiplier.

In addition to the components mentioned before, the ALU also implements a combinational logic that determines the operation sign, taking both operands MSB and performing an XOR. This signal is

then compared again with the carry-out asserted by the adder/subtractor. Moreover, the instruction *LHI* was considered as a special case, whose operand B value has its lower 16-bit field concatenated with the higher one and then cleared.

3.1.1 Pentium4 Adder/Subtractor

This unit consists of a 32-bit adder/subtractor revised version from the net-lists delivered in the lab session, which now includes a bitwise xor network between operand B and the carry-in signal, which is asserted in case of subtraction.

3.1.2 UltraSPARC T2 3-level Shifter

The shifter presented during classes was modified to work on 32-bit operands, as it is demonstrated in Figure 3.3. This hardware implements all logic and arithmetic shifts described in the DLX Instruction Set Architecture (ISA).

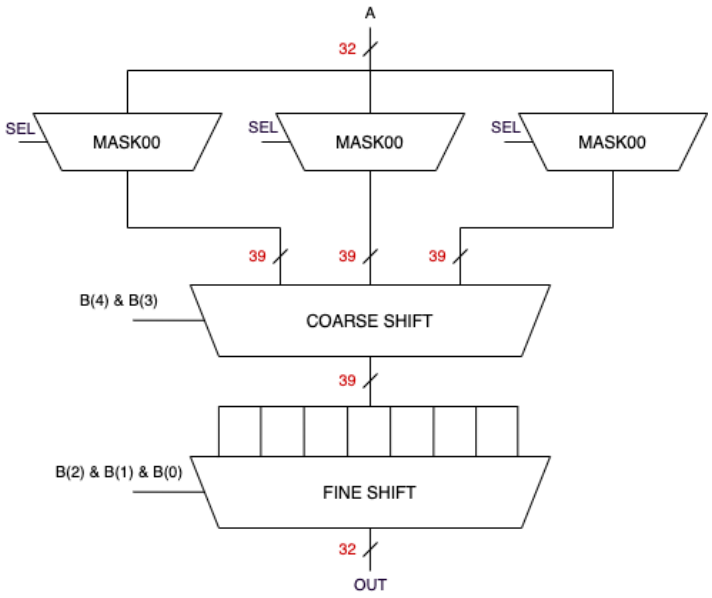

Figure 3.3: T2 3-level Shifter.

It is assumed that operand A represents the operand to be shifted and the lower bits of operand B represent the amount of position to shift, in a range starting from 0 up to 32. The structure is organized as described below:

- **1st-level Mask Generator:** according to the selection signal the first level produces three masks, shifted by 0 (MASK00), 8 (MAKS08) and 16 bits (MASK16), also extending operand A to 39 bits. The selection signal is asserted to:
  - 00: logic shift left, replacing vacant bits with 0's;
  - 01: logic shift right, replacing vacant bits with 0's;
  - 10: arithmetic shift right, replacing vacant bits with MSB.
- **2nd-level Coarse Shift:** one of the masks is selected according to the shift magnitude given by B(4) and B(3);
- **3rd-level Fine Shift:** the final result is produced.

3.1.3 UltraSPARC T2 Logic Unit

The logic unit was based on the UltraSPARC T2 one presented in the lectures, consisting of a 2-level NAND gate network. The first level performs a NAND operation between operands, their respective inverted values and the select signal that determines the final logic operation to be performed, being those: *AND*, **NAND**, **OR**, **NOR**, **XOR**, and *XNOR*. The second level performs a NAND operation between the four outputs of the previous stage, presenting the final result.

3.1.4 Signed/Unsigned Multi-purpose Comparator

The Multi-purpose Comparator presented in the lectures was slightly modified to deal with unsigned operations as well, as depicted in Figure 3.4 and mentioned when discussing the ALU block. The XOR gates and the adder/subtractor block were placed in that figure for simplicity, the comparator itself takes as input the carry signal after the comparison and the output Z given by the Zero Detector unit. It provides hardware support for several operations: $<$, $>$, $\leq$, $\geq$, $=$, and $\neq$.

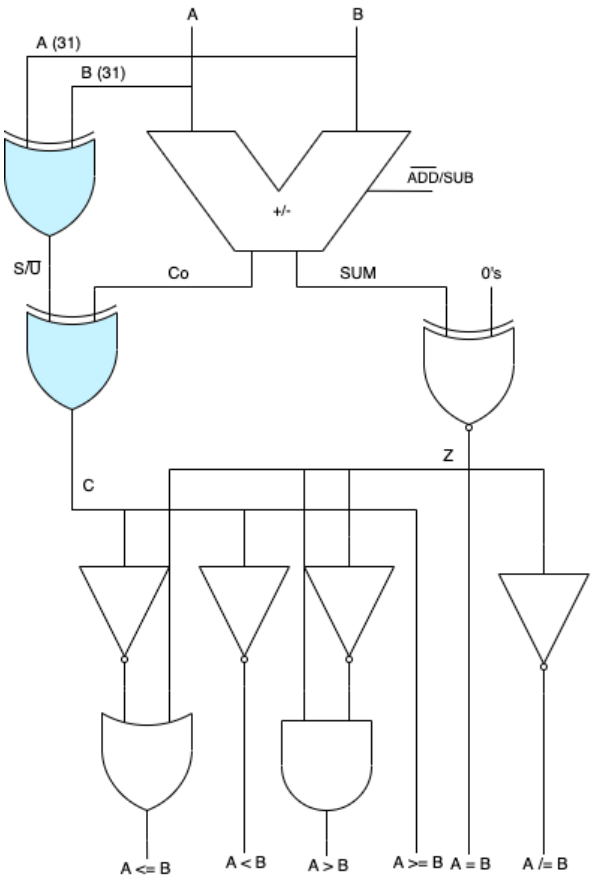

Figure 3.4: Sign/Unsigned Comparator.

3.1.5 Zero Detector

The Zero Detector is a simple XOR gate network that takes as one of the inputs the resulting output from the adder/subtractor and performs a bitwise operation with an array of 0's.

3.1.6 Booth Multiplier

The 32-bit Booth Multiplier takes as input the lower 16-bit field of operands A and B performing a signed integer multiplication. The code from the lab session was reused in this case without structural modifications. The *mult* instruction was assumed as being a special R-type instruction.

3.2 Forwarding Unit

Pipelined architectures have among some of their drawbacks the occurrence of stalls due to data hazards. When there is a true data dependency among instructions being processed by the pipeline simultaneously, such that one instruction must wait for the completion of the following ones as it depends on their result.

In order to avoid stalls and penalties, parallel components can be used to directly forward some results of instruction to another one before completion. Hence, read-after-Write (RAW) dependencies can be solved efficiently using a technique that allows data to skip the normal execution pipeline and to arrive directly where is needed.

In the DLX case, data is produced mainly in the ALU and DRAM, and fed to, again, the ALU and DRAM, but also the branching unit. Therefore, the Forwarding Unit (FU) checks both addresses and RF write enables signals for the instructions currently at the EXECUTE and MEMORY ACCESS stages to determine if there is a true data dependency, hence, taking a decision of which data must be forwarded.

CHAPTER 4

Synthesis

The synthesis phase started after completing the design and simulation, using **Design Vision**. It was split into several phases, where the preliminary one consisted of synthesizing the DLX-basic version for later comparison with the subsequent DLX-pro synthesis results. The results were obtained using a 65nm ST-Microelectronics library, Table 4.1 reports those results achieved with an unconstrained synthesis of both design versions. The significant increase in the data arrival delay from one version to another is mainly due to the insertion of the Booth Multiplier.

Version	Data arrival time ηs	Total cell area μm^2	Total Power μW
DLX-basic	0.12	14518.279764	1.1643e+03
DLX-pro	0.94	17750.977786	1.2455e+03

Table 4.1: Comparison between DLX-basic and DLX-pro version.

The second phase dealt with a static timing analysis performed over the DLX-pro version only. A clock signal was initially set to a **1.0** ηs period in conjunction with a delay constraint set from all inputs to all outputs with its value equal to the clock period. Compilation took place using a high map effort. The period was then increased by a **0.5** step at each iteration, up to **3.0** ηs, with the results reported at the end of each iteration. Details on the commands used during synthesis are reported in Appendix B, the chart in Figure 4.1 depicts the results obtained with each clock period in a 2D design space exploration.

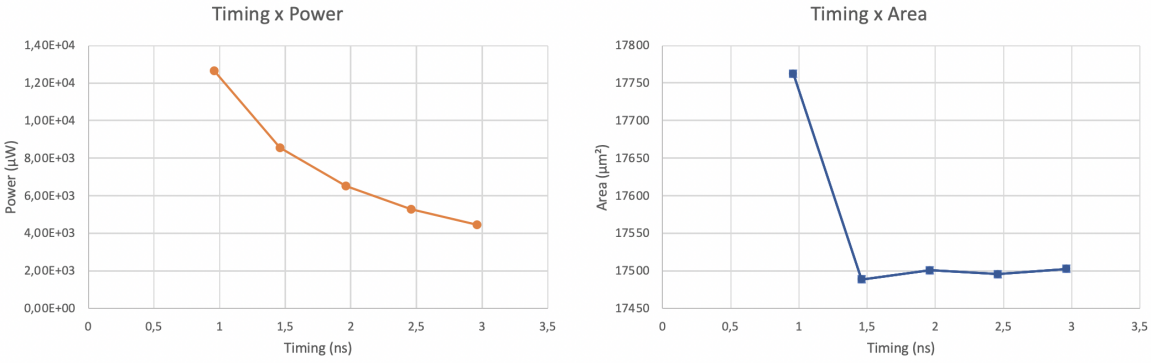

Figure 4.1: Static timing analysis.

The system running with a **1.0** ηs constraint presented a slack violation. From those results, it's

clear that the system running with a **1.5** ηs constraint had a better performance overall in terms of timing and area, despite being the implementation with the worst power performance.

The synthesis then proceeds to a power optimization phase. As mention in the previous sections, the ALU was optimized to reduce circuit switching activity. In addition, all 3-input multiplexers instantiated throughout the data-path were design used the one-hot encoding technique to reduce power consumption also. The Table 4.2 compares both design styles regarding the switching power with the **1.5** ηs timing constraint.

Version	Switching Power μW
Non-optimized ALU	636.7305
Optimized ALU	590.7418

Table 4.2: Comparison between switching power achieved before and after optimizing the ALU circuit.

Finally, the last synthesis phase consisted of applying the clock-gating technique on all generic registers used in the data-path, as well as the register file. The actual implementation consists of simply inserting an AND gate between the clock signal and the enable signal. The tool performs an exhaustive search over the VHDL description file for declarations that correspond to an enable signal, hence, such design files must be carefully written. Additionally, further optimization was achieved at the end of the compilation as this technique uses the command **compile_ultra**. The results obtained are reported bellow.

Number of Clock gating elements: 39
Number of Gated registers: 1518 (93.99%)
Number of Ungated registers : 97 (6.01%)
Total number of registers: 1615

The final version delivered to the physical layout implementation was the DLX-pro with optimized ALU and gated registers with a maximum delay of **1.46** ηs able to operate correctly with a **1.5** ηs clock period, i.e., a **666** MHz clock frequency, accounting setup and hold times. Other parameters are reported below.

Total cell area: 13459.865882 μm^2
Total power: 6.5272e+03 μW

CHAPTER 5

Physical Layout

The final step of this project requires using the netlists obtained during synthesis to implement the DLX physical layout over the **Cadence Innovus**. The same steps given during the lab session related to this subject were followed and Figure 5.1 illustrates the final schematic obtained after routing. The PWR and GND distribution is achieved through two rings around the die and 7 vertical lines using Metal 9 and Metal 10.

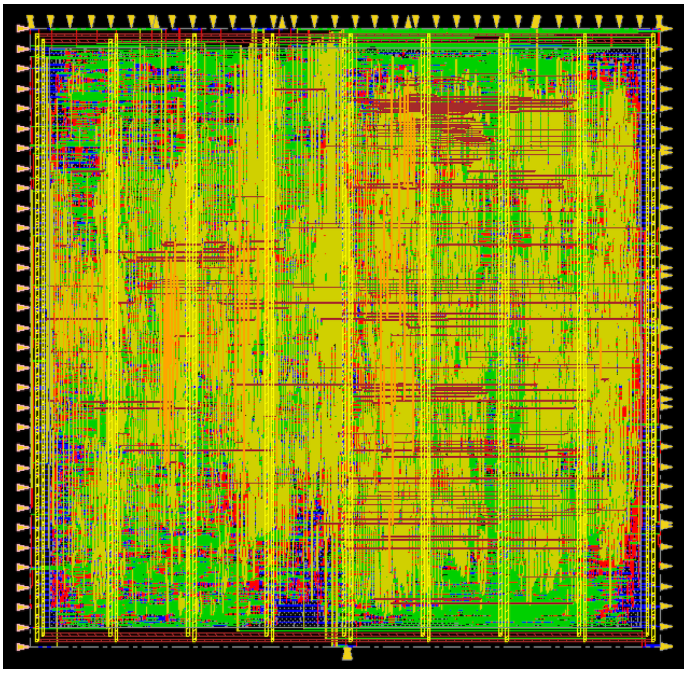

Figure 5.1: Final schematic.

The final gate count, with a gate area of **0.7980** μm^2 is reported in Table 5.1

Level	Gates	Cells	Area μm^2
0 Module DLX_WIDTH32	16931	6292	13511.5
1 Module DP/RegFILE	9084	2902	7249.0

Table 5.1: Gate count results.

APPENDIX A

Appendix A

```
# Compile
vcom 000-globals.vhd
vcom 01-fa.vhd
vcom 01-generic_mux21.vhd
vcom 01-generic_mux31.vhd
vcom 01-generic_rca.vhd
vcom 01-generic_register.vhd
vcom 01-ivx.vhd
vcom 01-nand2.vhd
vcom a.b-DataPath.core/a.b.a-ALU.core/a.b.a.a-adder.core/a.b.a.a.a-
    pg_network.vhd
vcom a.b-DataPath.core/a.b.a-ALU.core/a.b.a.a-adder.core/a.b.a.a.b-
    g_block.vhd
vcom a.b-DataPath.core/a.b.a-ALU.core/a.b.a.a-adder.core/a.b.a.a.c-
    pg_block.vhd
vcom a.b-DataPath.core/a.b.a-ALU.core/a.b.a.a-adder.core/a.b.a.a.d-
    carry_select_block.vhd
vcom a.b-DataPath.core/a.b.a-ALU.core/a.b.a.a-adder.core/a.b.a.a.e-
    sum_generator.vhd
vcom a.b-DataPath.core/a.b.a-ALU.core/a.b.a.a-adder.core/a.b.a.a.f-
    sparse_tree.vhd
vcom a.b-DataPath.core/a.b.a-ALU.core/a.b.a.b-shifter.core/a.b.a.b.a-
    mask_generator.vhd
vcom a.b-DataPath.core/a.b.a-ALU.core/a.b.a.b-shifter.core/a.b.a.b.b-
    coarse_shift.vhd
vcom a.b-DataPath.core/a.b.a-ALU.core/a.b.a.b-shifter.core/a.b.a.b.c-
    fine_shift.vhd
vcom a.b-DataPath.core/a.b.a-ALU.core/a.b.a.c-logic.core/a.b.a.c.a-nand3.
    vhd
vcom a.b-DataPath.core/a.b.a-ALU.core/a.b.a.c-logic.core/a.b.a.c.b-nand4.
    vhd
vcom a.b-DataPath.core/a.b.a-ALU.core/a.b.a.f-multiplier.core/a.b.a.f.a-
    booth_encoder.vhd
vcom a.b-DataPath.core/a.b.a-ALU.core/a.b.a.f-multiplier.core/a.b.a.f.b-
```

```
    rca_mul.vhd
vcom a.b-DataPath.core/a.b.a-ALU.core/a.b.a.a-adder.vhd
vcom a.b-DataPath.core/a.b.a-ALU.core/a.b.a.b-shifter.vhd
vcom a.b-DataPath.core/a.b.a-ALU.core/a.b.a.c-logic.vhd
vcom a.b-DataPath.core/a.b.a-ALU.core/a.b.a.d-comparator.vhd
vcom a.b-DataPath.core/a.b.a-ALU.core/a.b.a.e-zero_detector.vhd
vcom a.b-DataPath.core/a.b.a-ALU.core/a.b.a.f-multiplier.vhd
vcom a.b-DataPath.core/a.b.a-ALU.vhd
vcom a.b-DataPath.core/a.b.b-register_file.vhd
vcom a.b-DataPath.core/a.b.c-sign_extend.vhd
vcom a.b-DataPath.core/a.b.d-branch_unit.vhd
vcom a.b-DataPath.core/a.b.e-forwarding_unit.vhd
vcom a.a-CU_HW.vhd
vcom a.b-DataPath.vhd
vcom a-DLX.vhd
vcom b-IRAM.vhd
vcom c-DRAM.vhd
vcom test_bench/TB_DLX.vhd

# Start simulation
vsim -t 10ps work.dlx_tb(testbench)

# ProgramCounter #
add wave -group ProgramCounter sim:/dlx_tb/uut/pc/*

# IRAM #
add wave -group InstructionMemory sim:/dlx_tb/iram/*

# InstructionRegister #
add wave -group InstructionRegister sim:/dlx_tb/uut/ir/*

# ControlUnit #
add wave -group ControlUnit sim:/dlx_tb/uut/cu/*

# DataPath #
# Stage 1
add wave -group DataPath -group RegNPC1 sim:/dlx_tb/uut/dp/RegNPC1/*
# Stage 2
add wave -group DataPath -group MuxWR sim:/dlx_tb/uut/dp/MuxWR/*
add wave -group DataPath -group RegFILE sim:/dlx_tb/uut/dp/RegFILE/*
add wave -group DataPath -group RegA sim:/dlx_tb/uut/dp/RegA/*
add wave -group DataPath -group RegB sim:/dlx_tb/uut/dp/RegB/*
add wave -group DataPath -group SignImm16 sim:/dlx_tb/uut/dp/SignImm16/*
add wave -group DataPath -group SignImm26 sim:/dlx_tb/uut/dp/SignImm26/*
add wave -group DataPath -group MuxIMM sim:/dlx_tb/uut/dp/MuxIMM/*
add wave -group DataPath -group RegIMM sim:/dlx_tb/uut/dp/RegIMM/*
add wave -group DataPath -group RegRD2 sim:/dlx_tb/uut/dp/RegRD2/*
add wave -group DataPath -group RegNPC2 sim:/dlx_tb/uut/dp/RegNPC2/*
# Stage 3
```

```
add wave -group DataPath -group MuxA sim:/dlx_tb/uut/dp/MuxA/*
add wave -group DataPath -group MuxB sim:/dlx_tb/uut/dp/MuxB/*
add wave -group DataPath -group FwdA sim:/dlx_tb/uut/dp/FwdA/*
add wave -group DataPath -group FwdB sim:/dlx_tb/uut/dp/FwdB/*
add wave -group DataPath -group FwdC sim:/dlx_tb/uut/dp/FwdC/*
add wave -group DataPath -group ALU0 sim:/dlx_tb/uut/dp/ALU0/*
add wave -group DataPath -group RegALU3 sim:/dlx_tb/uut/dp/RegALU3/*
add wave -group DataPath -group ZERO sim:/dlx_tb/uut/dp/ZERO/*
add wave -group DataPath -group COND sim:/dlx_tb/uut/dp/COND/*
add wave -group DataPath -group RegME sim:/dlx_tb/uut/dp/RegME/*
add wave -group DataPath -group RegRD3 sim:/dlx_tb/uut/dp/RegRD3/*
add wave -group DataPath -group RegNPC3 sim:/dlx_tb/uut/dp/RegNPC3/*
# Stage 4
add wave -group DataPath -group MuxMEM sim:/dlx_tb/uut/dp/MuxMEM/*
add wave -group DataPath -group FwdD sim:/dlx_tb/uut/dp/FwdD/*
add wave -group DataPath -group RegLMD sim:/dlx_tb/uut/dp/RegLMD/*
add wave -group DataPath -group RegRD4 sim:/dlx_tb/uut/dp/RegRD4/*
add wave -group DataPath -group RegNPC4 sim:/dlx_tb/uut/dp/RegNPC4/*
add wave -group DataPath -group RegALU4 sim:/dlx_tb/uut/dp/RegALU4/*
# Stage 5
add wave -group DataPath -group MuxWB sim:/dlx_tb/uut/dp/MuxWB/*
# Forwarding Unit
add wave -group DataPath -group FU sim:/dlx_tb/uut/dp/FU/*

# DRAM #
add wave -group DataMemory sim:/dlx_tb/dram/*

# Set unsigned as DEFAULT radix
radix -hex
# Run simulation
run 250 ns
# Print postscript waveform
#write wave p4adder.ps -start 0 -end 230000 -perpage 230000
```

APPENDIX B

Appendix B

```
#########################################################################
exec mkdir -p work
exec mkdir -p report
exec mkdir -p netlist

analyze -library WORK -format vhdl {000-globals.vhd}
analyze -library WORK -format vhdl {01-fa.vhd}
analyze -library WORK -format vhdl {01-generic_mux21.vhd}
analyze -library WORK -format vhdl {01-generic_mux31.vhd}
analyze -library WORK -format vhdl {01-generic_rca.vhd}
analyze -library WORK -format vhdl {01-generic_register.vhd}
analyze -library WORK -format vhdl {01-ivx.vhd}
analyze -library WORK -format vhdl {01-nand2.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.a-ALU.core/a.b.
    a.a-adder.core/a.b.a.a.a-pg_network.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.a-ALU.core/a.b.
    a.a-adder.core/a.b.a.a.b-g_block.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.a-ALU.core/a.b.
    a.a-adder.core/a.b.a.a.c-pg_block.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.a-ALU.core/a.b.
    a.a-adder.core/a.b.a.a.d-carry_select_block.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.a-ALU.core/a.b.
    a.a-adder.core/a.b.a.a.e-sum_generator.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.a-ALU.core/a.b.
    a.a-adder.core/a.b.a.a.f-sparse_tree.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.a-ALU.core/a.b.
    a.b-shifter.core/a.b.a.b.a-mask_generator.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.a-ALU.core/a.b.
    a.b-shifter.core/a.b.a.b.b-coarse_shift.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.a-ALU.core/a.b.
    a.b-shifter.core/a.b.a.b.c-fine_shift.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.a-ALU.core/a.b.
    a.c-logic.core/a.b.a.c.a-nand3.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.a-ALU.core/a.b.
```

```
    a.c-logic.core/a.b.a.c.b-nand4.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.a-ALU.core/a.b.
    a.f-multiplier.core/a.b.a.f.a-booth_encoder.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.a-ALU.core/a.b.
    a.f-multiplier.core/a.b.a.f.b-rca_mul.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.a-ALU.core/a.b.
    a.a-adder.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.a-ALU.core/a.b.
    a.b-shifter.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.a-ALU.core/a.b.
    a.c-logic.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.a-ALU.core/a.b.
    a.d-comparator.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.a-ALU.core/a.b.
    a.e-zero_detector.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.a-ALU.core/a.b.
    a.f-multiplier.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.a-ALU.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.b-register_file
    .vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.c-sign_extend.
    vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.d-branch_unit.
    vhd}
analyze -library WORK -format vhdl {a.b-DataPath.core/a.b.e-
    forwarding_unit.vhd}
analyze -library WORK -format vhdl {a.a-CU_HW.vhd}
analyze -library WORK -format vhdl {a.b-DataPath.vhd}
analyze -library WORK -format vhdl {a-DLX.vhd}

# Elaborate
current_design DLX_WIDTH32
elaborate DLX -architecture STRUCTURAL -library WORK -parameters "WIDTH =
    32"
set_wire_load_model -name 5K_hvratio_1_4

#Unconstrained synthesis
compile -exact_map
report_area > report/DLX_AREA.txt
report_timing > report/DLX_TIMING.txt
report_power > report/DLX_POWER.txt

#Static timing analysis
#1.0 cycle constraint
create_clock -name "CLK" -period 1.0 CLK
set_max_delay 1.0 -from [all_inputs] -to [all_outputs]
compile -exact_map -map_effort high
report_area > report/DLX_AREA_10.txt
report_timing > report/DLX_TIMING_10.txt
```

```
report_power > report/DLX_POWER_10.txt
#1.5 cycle constraint
create_clock -name "CLK" -period 1.5 CLK
set_max_delay 1.5 -from [all_inputs] -to [all_outputs]
compile -exact_map -map_effort high
report_area > report/DLX_AREA_15.txt
report_timing > report/DLX_TIMING_15.txt
report_power > report/DLX_POWER_15.txt
#2.0 cycle constraint
create_clock -name "CLK" -period 2.0 CLK
set_max_delay 2.0 -from [all_inputs] -to [all_outputs]
compile -exact_map -map_effort high
report_area > report/DLX_AREA_20.txt
report_timing > report/DLX_TIMING_20.txt
report_power > report/DLX_POWER_20.txt
#2.5 cycle constraint
create_clock -name "CLK" -period 2.5 CLK
set_max_delay 2.5 -from [all_inputs] -to [all_outputs]
compile -exact_map -map_effort high
report_area > report/DLX_AREA_25.txt
report_timing > report/DLX_TIMING_25.txt
report_power > report/DLX_POWER_25.txt
#3.0 cycle constraint
create_clock -name "CLK" -period 3.0 CLK
set_max_delay 3.0 -from [all_inputs] -to [all_outputs]
compile -exact_map -map_effort high
report_area > report/DLX_AREA_30.txt
report_timing > report/DLX_TIMING_30.txt
report_power > report/DLX_POWER_30.txt


#Clock Gating
create_clock -name "CLK" -period 1.5 CLK
set_max_delay 1.5 -from [all_inputs] -to [all_outputs]

report_clock_gating > report/CLK_GATING_BEFORE.txt

write -hierarchy -format verilog -output netlist/dlx.v
write_sdc netlist/dlx.sdc

current_design REGISTER_FILE_WIDTH32_LENGTH5
set_clock_gating_style -minimum_bitwidth 1 -max_fanout 1024 -
    positive_edge_logic {latch and} -control_point before
compile_ultra -gate_clock
current_design DLX_WIDTH32

for {set i 0} {$i <= 3} {incr i} {
    current_design REGISTER_GENERIC_WIDTH5_$i
        set_clock_gating_style -minimum_bitwidth 1 -max_fanout 1024 -
```

```
            positive_edge_logic {latch and} -control_point before
        compile_ultra -gate_clock
        current_design DLX_WIDTH32
}

for {set i 0} {$i <= 12} {incr i} {
    current_design REGISTER_GENERIC_WIDTH32_$i
        set_clock_gating_style -minimum_bitwidth 1 -max_fanout 1024 -
            positive_edge_logic {latch and} -control_point before
        compile_ultra -gate_clock
        current_design DLX_WIDTH32
}

current_design DLX_WIDTH32
report_clock_gating > report/CLK_GATING_AFTER.txt
report_area > report/DLX_AREA_GATED.txt
report_timing > report/DLX_TIMING_GATED.txt
report_power > report/DLX_POWER_GATED.txt

write -hierarchy -format verilog -output netlist/dlx_gated.v
write_sdc netlist/dlx_gated.sdc
```