ELEC353 Lecture Notes Set 8

The homework assignments are posted on the course web site. http://users.encs.concordia.ca/~trueman/web_page_353.htm

Homework #4: Do homework #4 by February 8, 2019. Homework #5: Do homework #5 by February 14, 2019.

Mid-term test: Thursday February 14, 2019.

- Includes Homework #5!
- See the course web site for sample mid-term tests with solutions.
- Study tip:
 - Download the question paper for a mid-term from a previous year.
 - Spend one hour 15 minutes solving the test with your calculator and the formula sheet, but no textbook or notes.
 - Grade your answer against the solution to the test!

Tentative final exam date: Tuesday April 23, 2019, 9:00 to 12:00.

Mid-term Test: Thursday February 14, 2019

What is covered on the mid-term? Everything done in class up to February 12.

Lecture Notes Set 1 to Set 7

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Homework assignments #1 to 5
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#1 = lumped and distributed circuit analysis, RC model of a TL

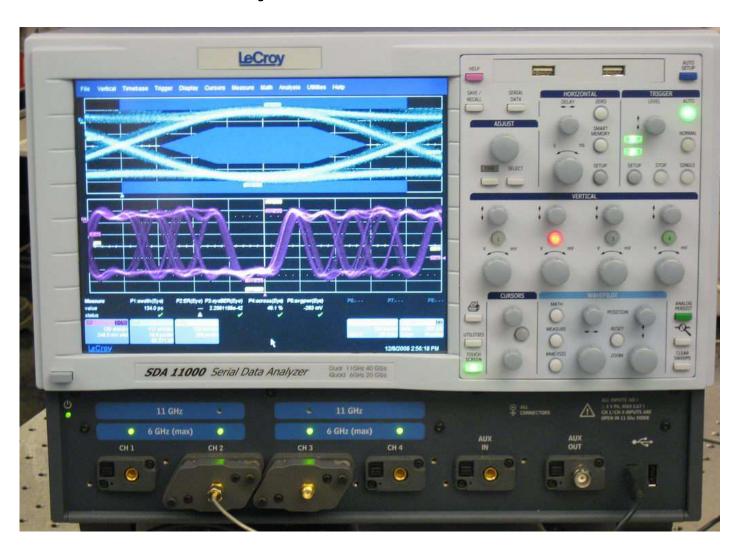
#2 = introductory TL questions, bounce diagram

#3 = TL in series, TL with shunt load

#4 = branching TL, RL load, TDR

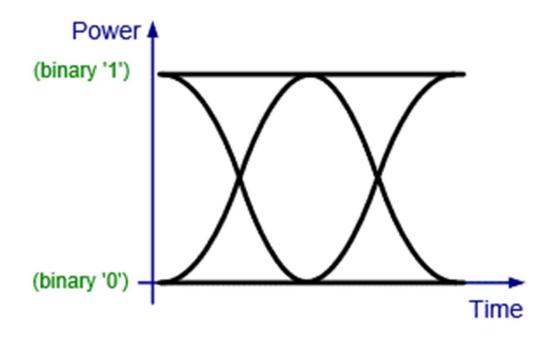
#5 = RL load, transmission lines in series, pulse generator, TDR

Eye Patterns



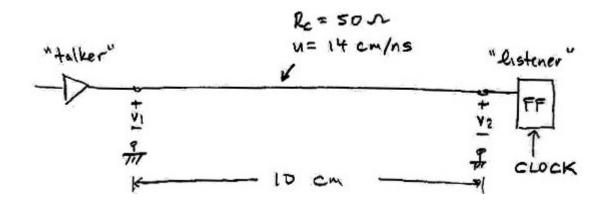
Wikipedia:

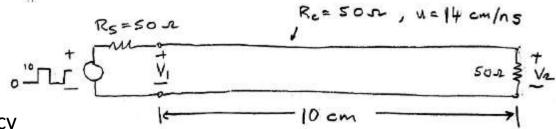
In <u>telecommunication</u>, an **eye pattern**, also known as an **eye diagram**, is an <u>oscilloscope</u> display in which a <u>digital signal</u> from a receiver is repetitively sampled and applied to the vertical input, while the data rate is used to trigger the horizontal sweep. It is so called because, for several types of coding, the pattern looks like a series of eyes between a pair of rails. It is a tool for the evaluation of the combined effects of channel noise and <u>intersymbol interference</u> on the performance of a baseband pulse-transmission system. It is the synchronised superposition of all possible realisations of the signal of interest viewed within a particular signaling interval.



An Ideal Transmission Path

- o No mismatch
- o No reflections
- The only difference between the "input" and the "output" is the propagation delay of $T_d = \frac{L}{u}$.





Frequency

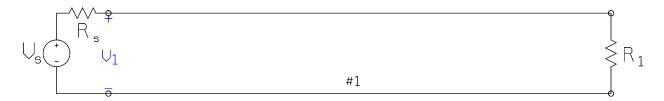
2GHz

Rise time

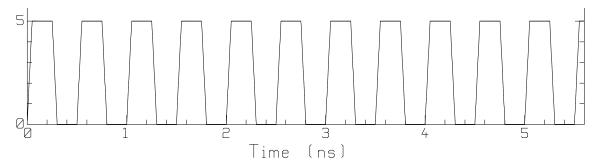
0.05 ns

The transit time on the 10 cm line is $T = \frac{L}{u} = \frac{10}{14} = 0.714$ ns

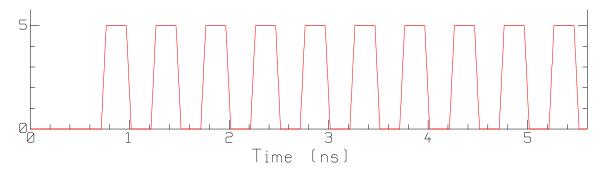
An ideal transmission path:



Input:



Output: a delayed copy of the input.

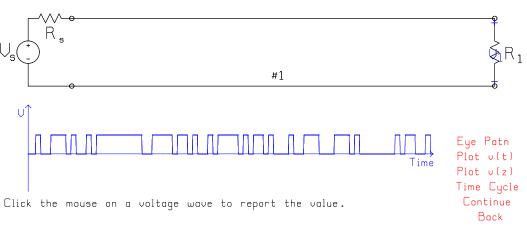


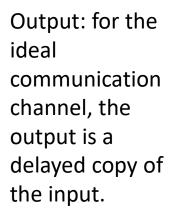
Eye Pattern for the Ideal Communication Channel

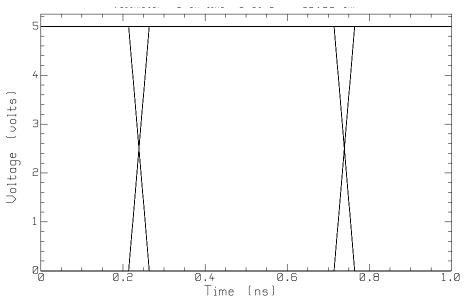
Input: V_s is a random series of Os and 1s.

Frequency 2GHz Rise time 0.05 ns

This is the eye pattern for the bit stream shown above.

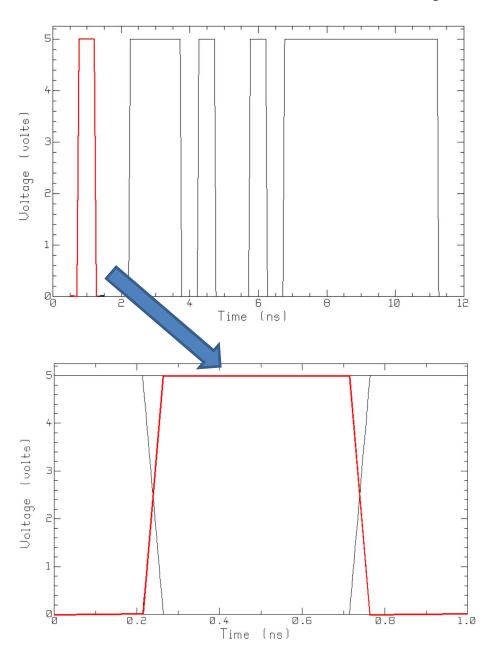






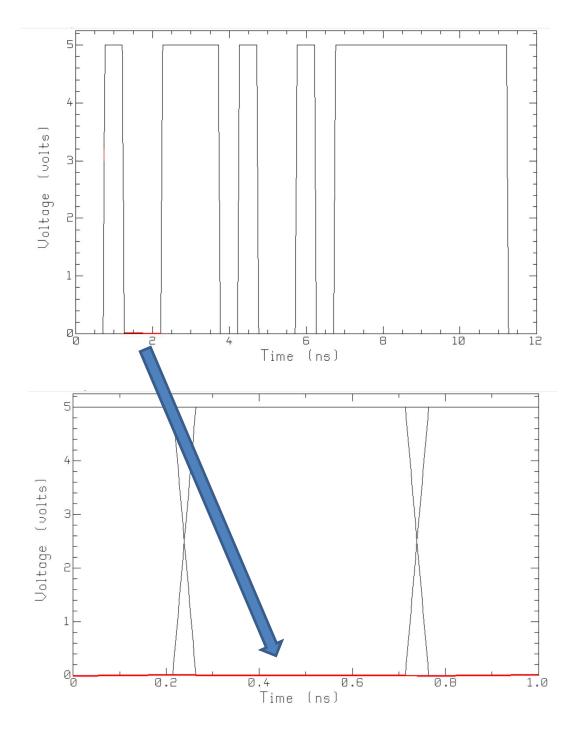
How do we construct the eye pattern?

Construct an Eye Pattern

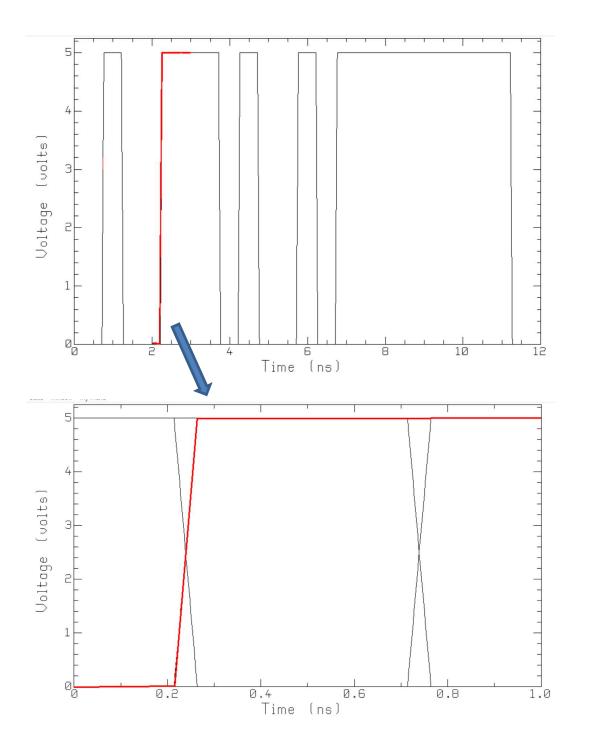


The voltage across the load has a series of 1s and 0s, with transitions lasting 0.05 ns.

Draw the first "time slot" on an expanded scale, showing the transition up and the transition down.



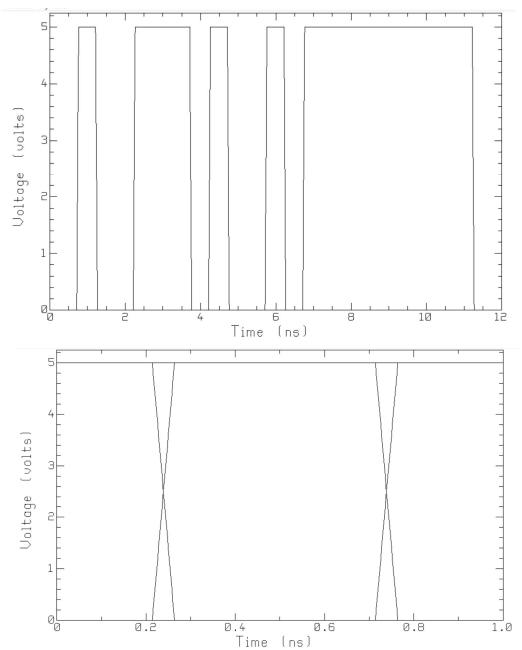
The second time slot has a zero bit.



The third time slot has a transition from 0 to 1.

We can continue for the whole sample of 0s and 1s, leading to the complete Eye Pattern diagram for the time sample.

Plot all the transitions:

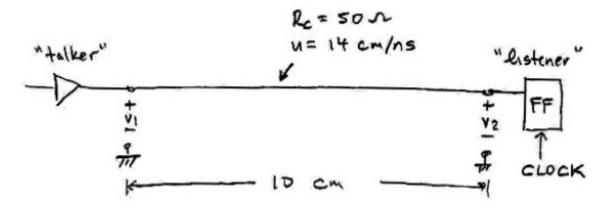


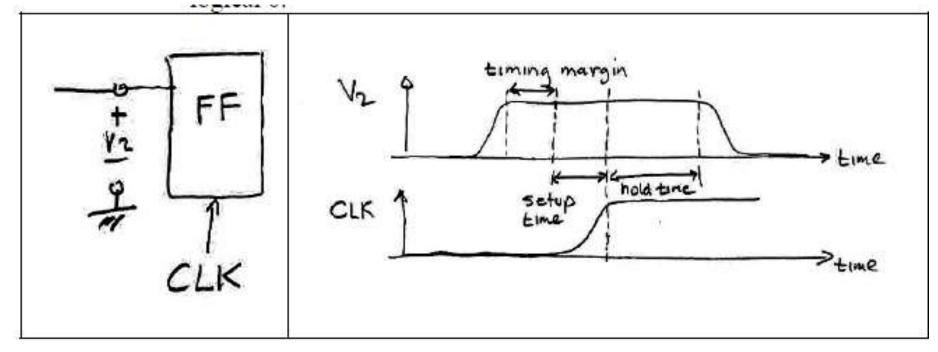
Plot all the 0s and 1s to get the complete eye pattern.

In real practice eye patterns include thousands and thousands of transitions from 0 to 1 and from 1 to 0.

What can we learn from an eye pattern?

What is "fast enough" in a digital circuit?

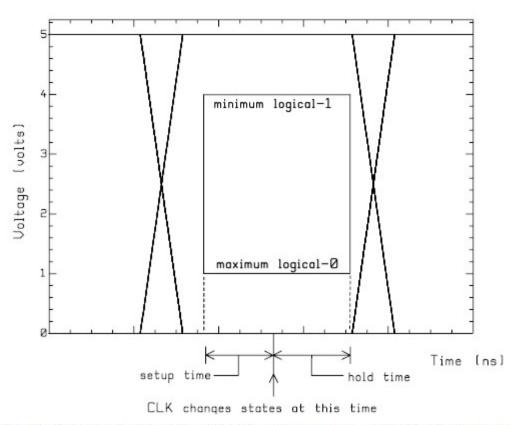




Interpreting Eye Patterns

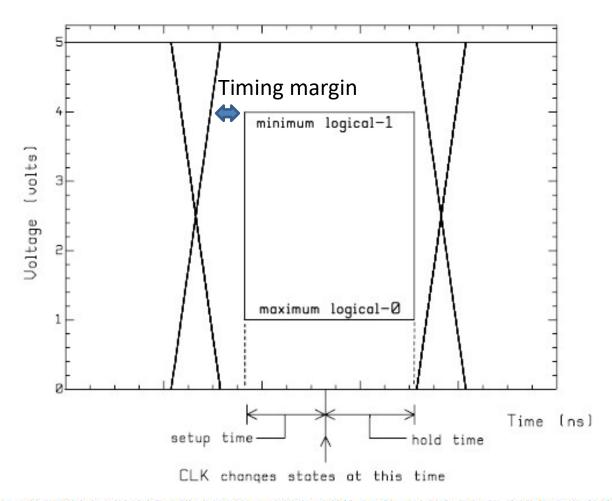
Suppose for our logic family, the specs are:

- o 0 to 5 volt logic
- o The minimum voltage for "logical 1" is 4 volts
- o The maximum voltage for "logical 0" is 1 volt



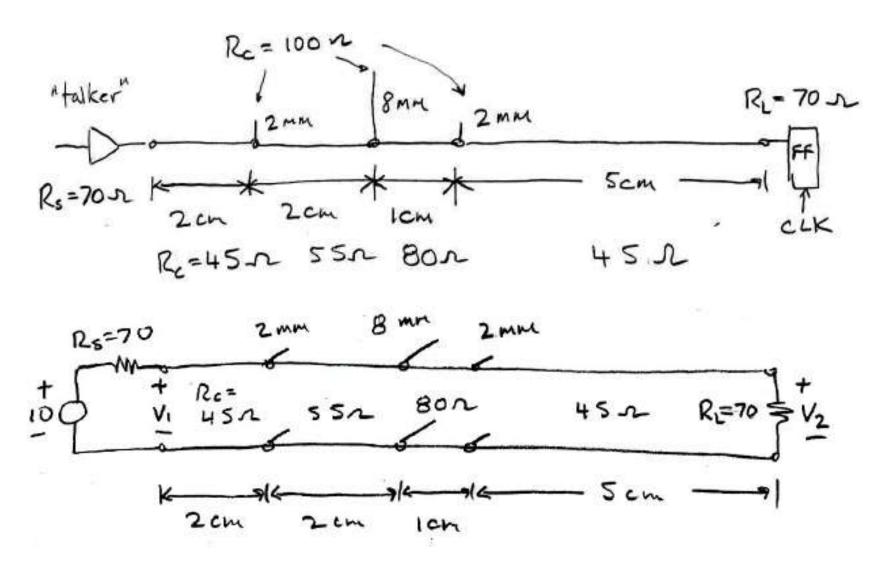
- The "timing margin" is the amount of time between the instant when the data is "valid" and the instant when the setup time starts.
- Note that the "timing margin" is about 1/3 of the setup time in this example.

Timing Margin

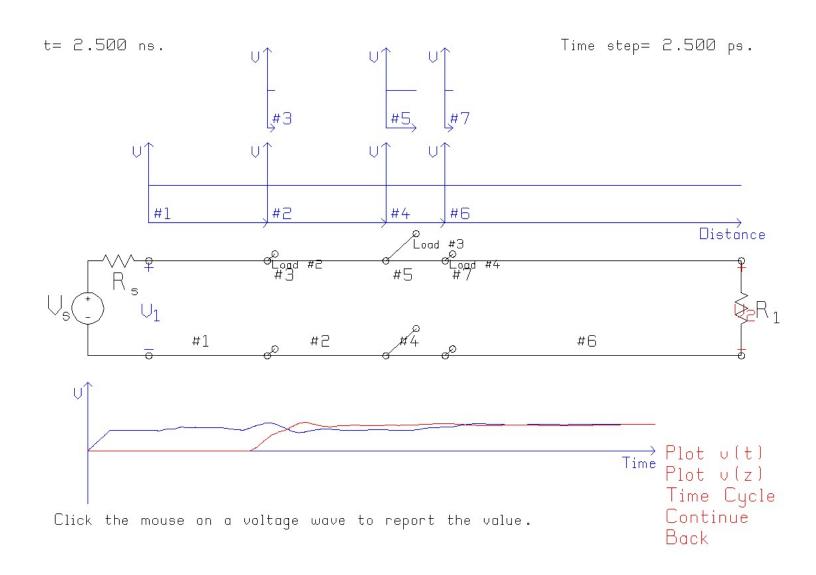


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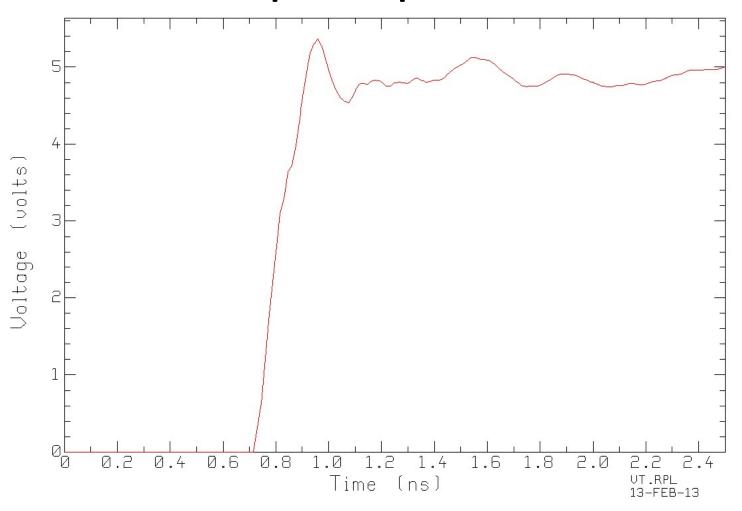
Realistic Communication Path



Step Response

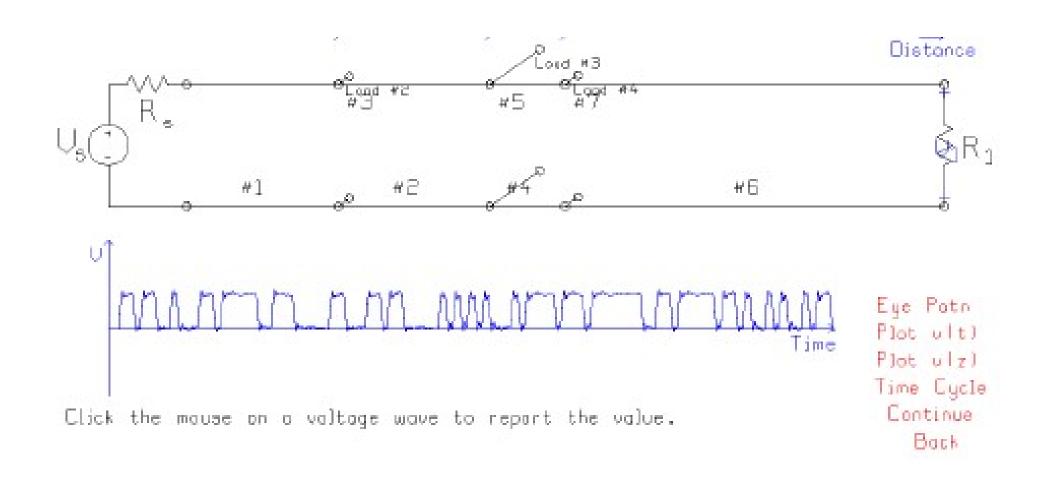


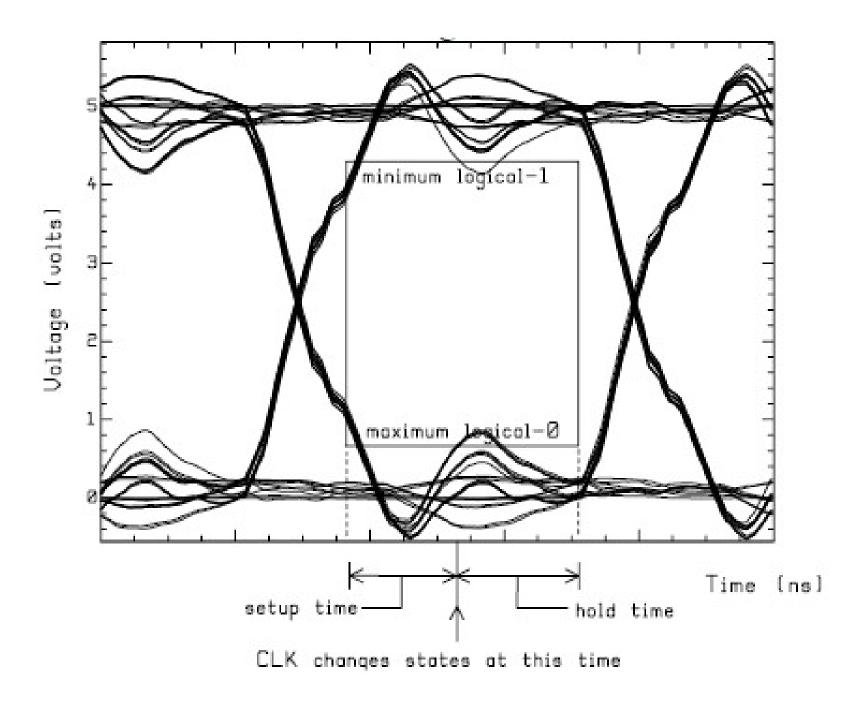
Step Response



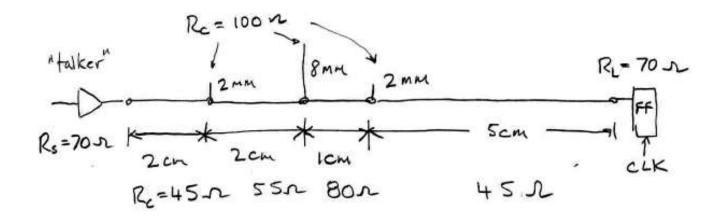
The time slot for each bit is 1 ns. The step takes more than 2 time slots to settle. Does the step response settle fast enough? How do we judge what is "fast enough"?

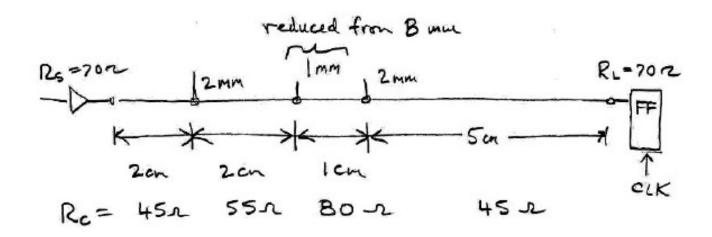
Examine many transitions from 0 to 1 and from 1 to 0 to verify that each transition meets the timing requirements:

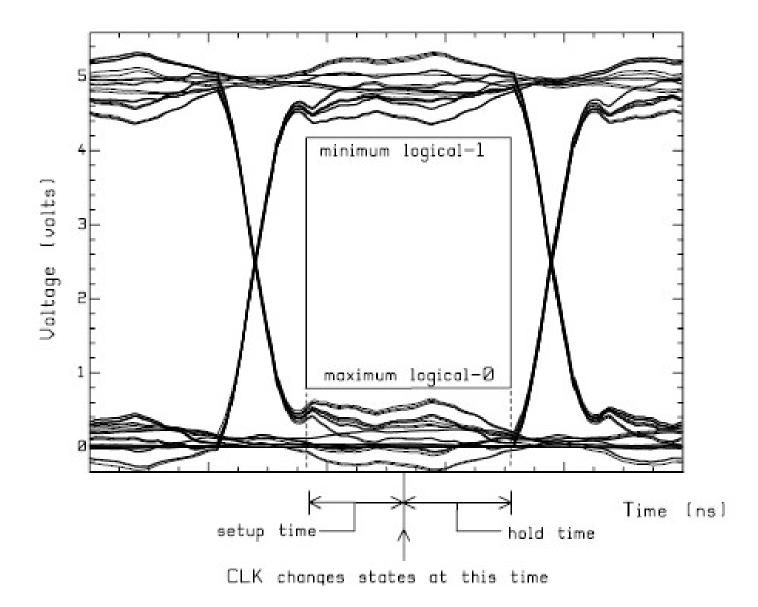


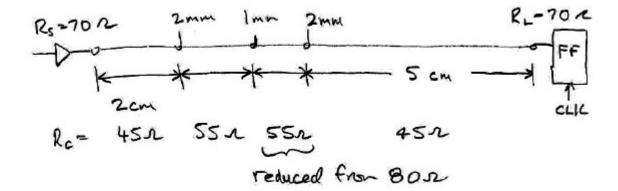


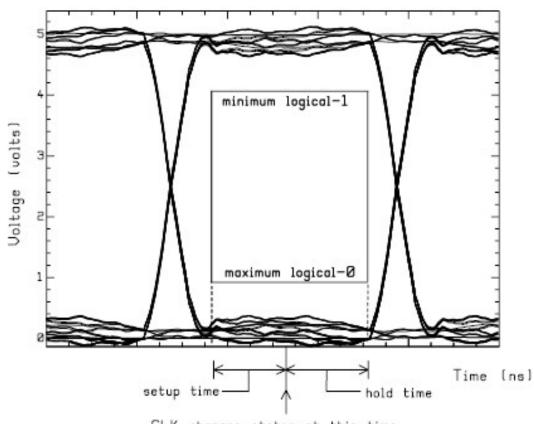
How can we "clean up" the eye pattern?





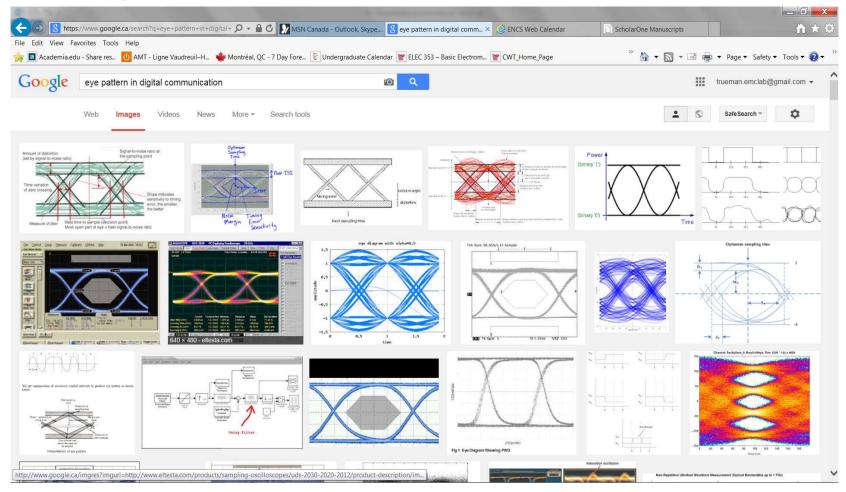






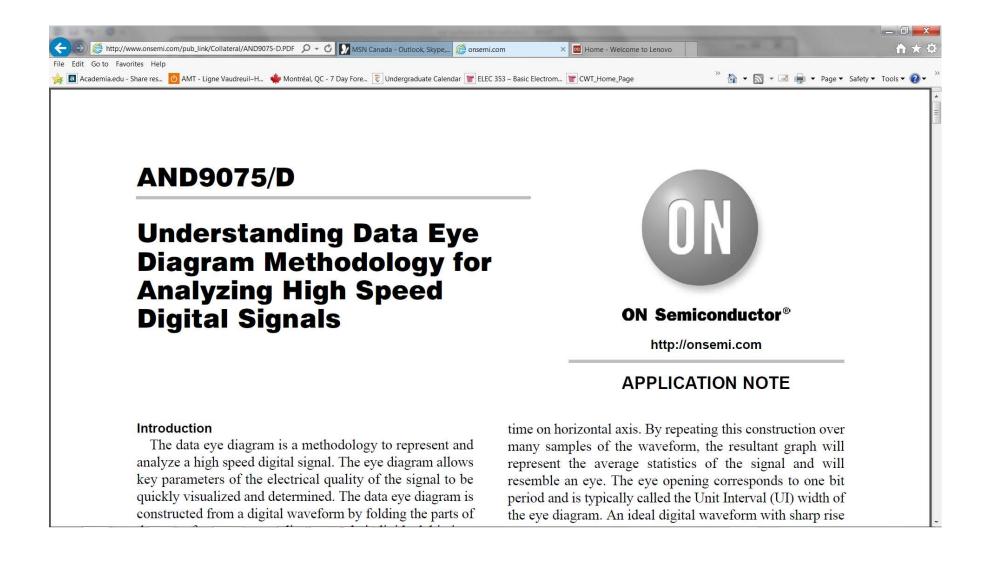
CLK changes states at this time

Eye Patterns on the Internet



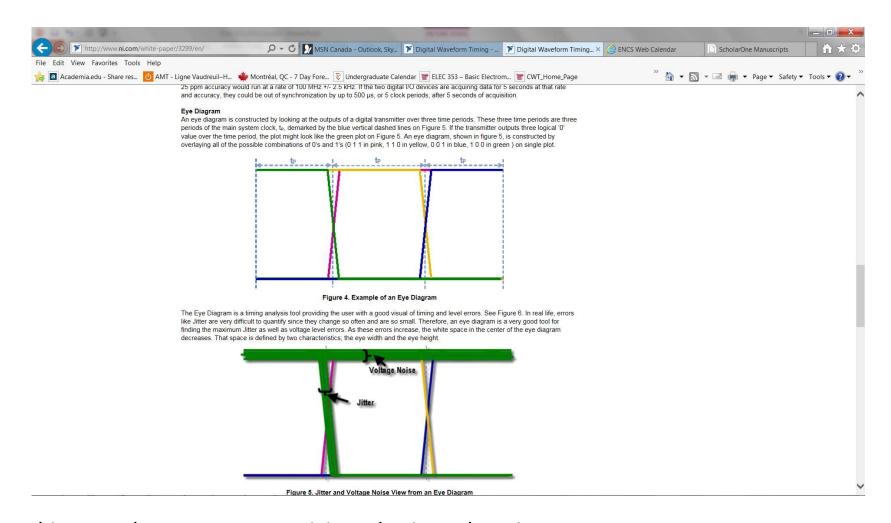
This page has many pictures of eye patterns

https://www.google.ca/search?q=eye+pattern+in+digital+communication&biw=15 36&bih=757&tbm=isch&tbo=u&source=univ&sa=X&ei=3GrbVIzZKpT_yQTT3YHwC Q&ved=0CCMQsAQ



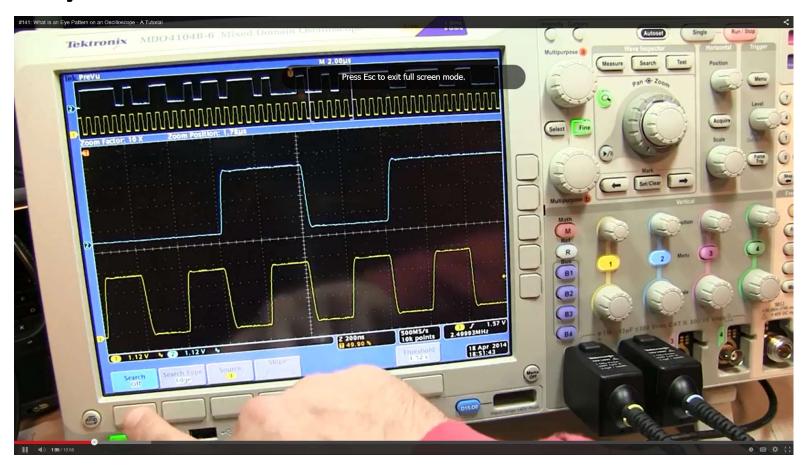
This paper has a really good detailed explanation about eye patterns and what they are:

http://www.onsemi.com/pub_link/Collateral/AND9075-D.PDF

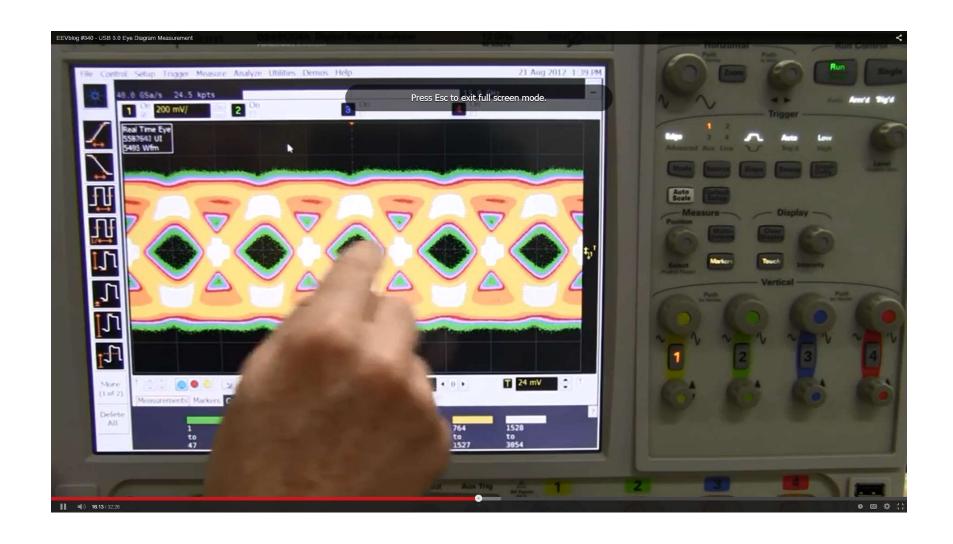


This note about eye patters giving a basic explanation: http://www.ni.com/white-paper/3299/en/

Eye Pattern Videos on You Tube



Video explaining eye patterns on an oscilloscope screen: https://www.youtube.com/watch?v=cL7QsELuv_M
11 minutes



Long video explaining how to use a great oscilloscope with eye patterns: https://www.youtube.com/watch?v=o8DPlqWVmzk 33 minutes!