ELEC353 Lecture Notes Set 2

The course web site is:
www.ece.concordia.ca/~trueman/web_page_353.htm

- The course outline
- The lecture notes
- The homework assignment each week
- A set of practice problems with solutions
- Software: BOUNCE, TRLINE, WAVES

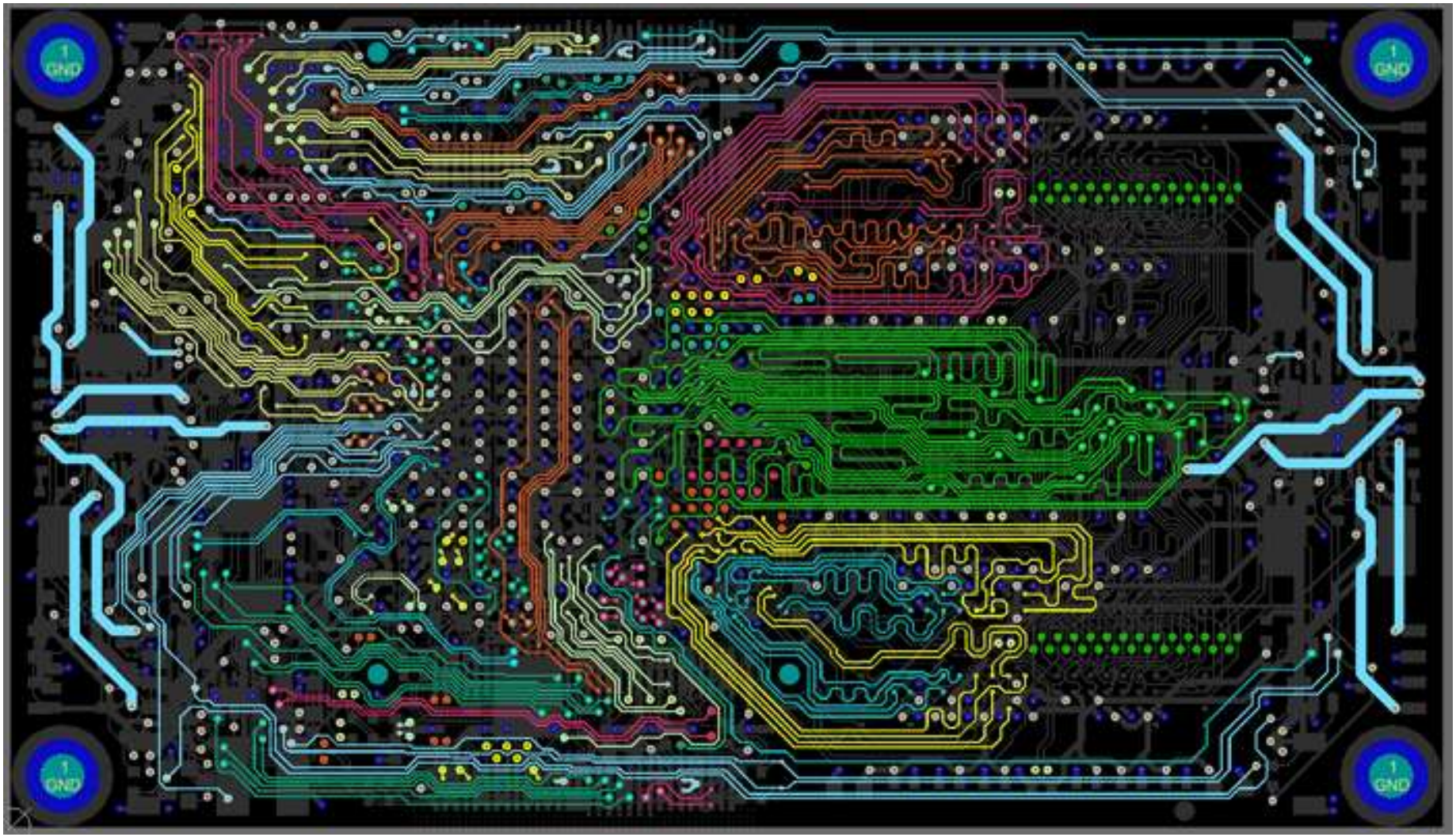
The homework assignments are posted on the course web site.

Homework #1: Do this assignment by January 18th, 2019.
Homework #2: Do this assignment by January 25nd.

Reading Assignment

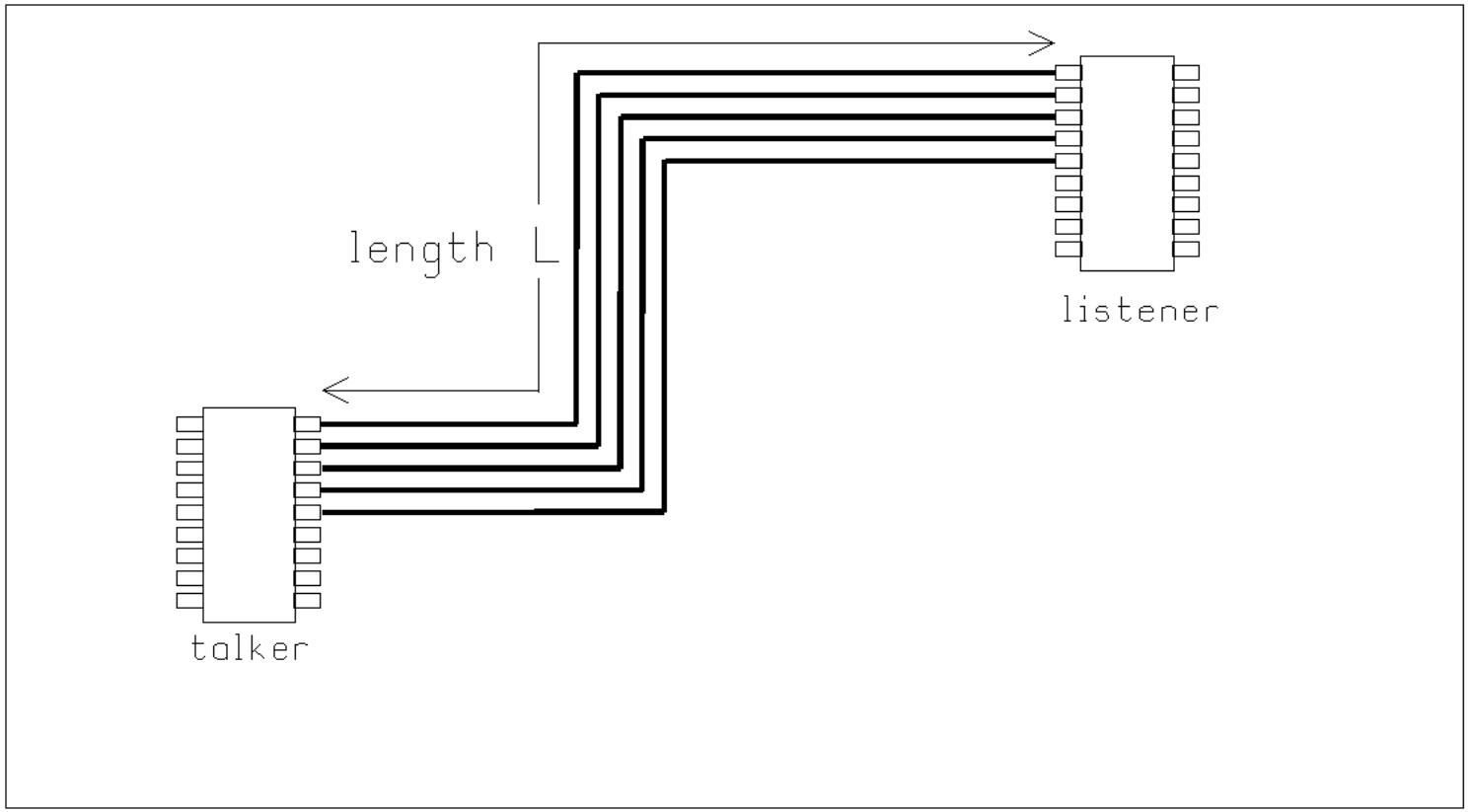
- Read Inan, Inan and Said Chapter 1 about lumped and distributed circuit analysis.
- Read inan, Inan and Said Chapter 2 about transmission lines. We will cover Chapter 2 over the next four weeks.

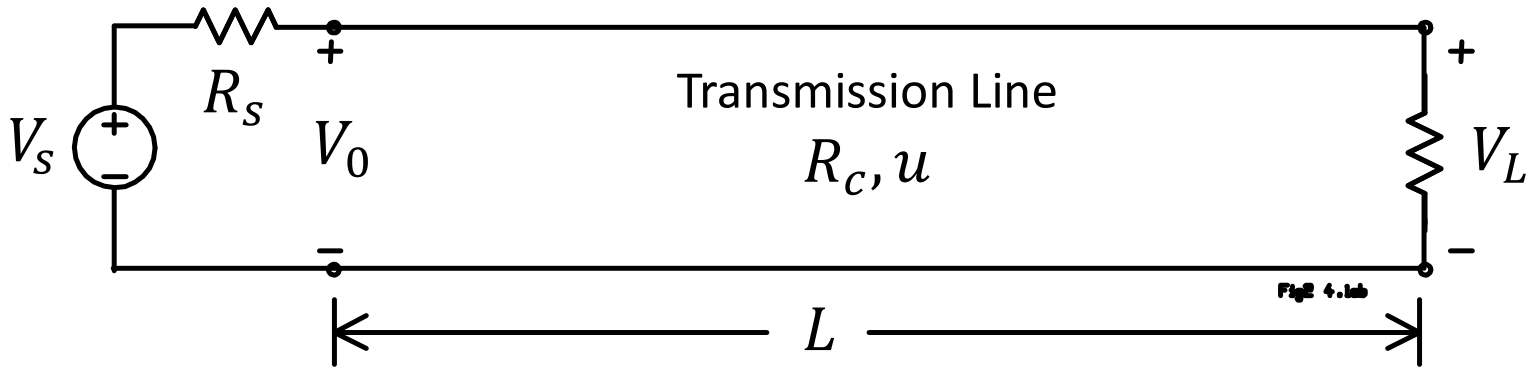
Modelling Circuit Interconnections on a PC Board

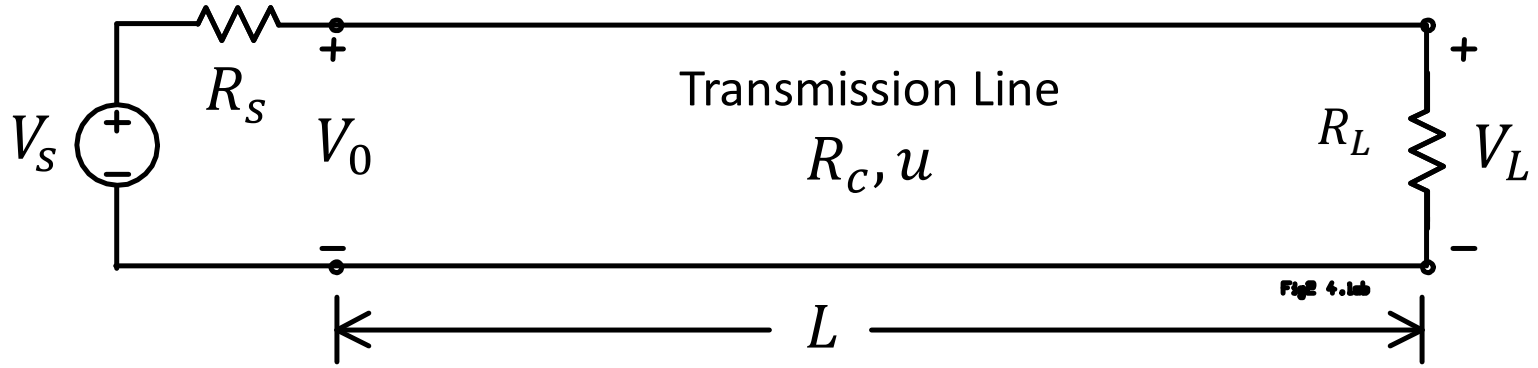


https://www.google.ca/search?q=printed+circuit+board+design&source=lnms&tbm=isch&sa=X&ved=0ahUKEwiagMvU_NvfAhXQuFkKHQZ0AGUQ_AUIDigB&biw=1280&bih=611#imgrc=3fsbexDR5K8z_M:

Equivalent Circuit for an Interconnection







Example: Suppose $V_s = 10$ volts and is a step function generator. Suppose $R_s = 30\ \Omega$ and $R_L = 1000\ \Omega$. If the circuit interconnection is an *ideal short circuit*, then what is the output voltage?

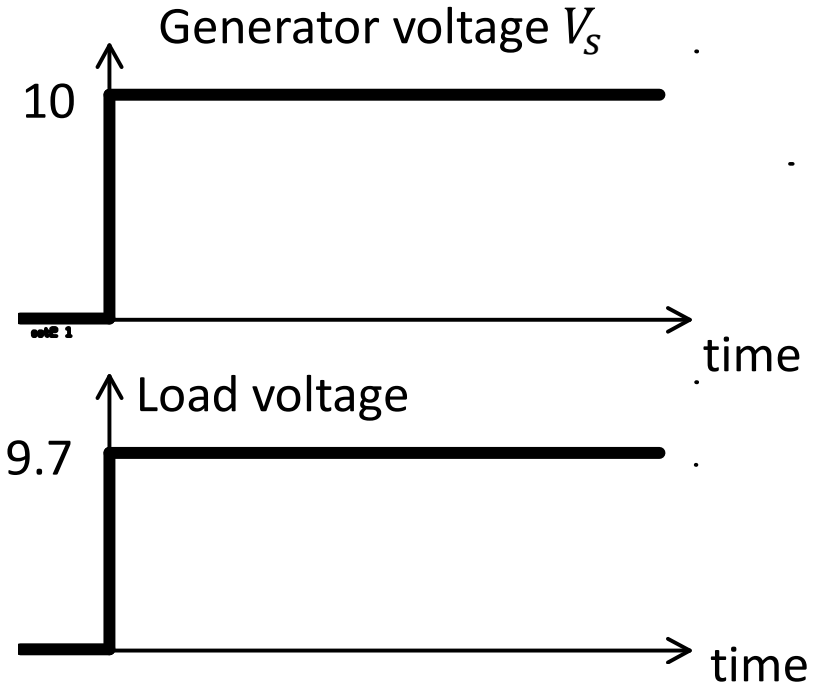
What is an ideal short circuit?

- A short circuit path behaves as a resistor with zero resistance.
- A short circuit path has zero time delay to go from the input a distance L to the output.

The output voltage is

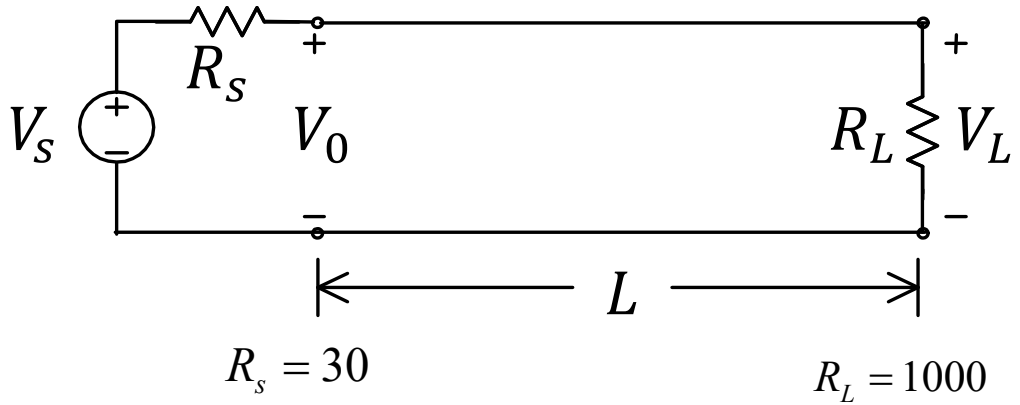
$V_L = \frac{10x1000}{1000+30} = 9.7$ volts

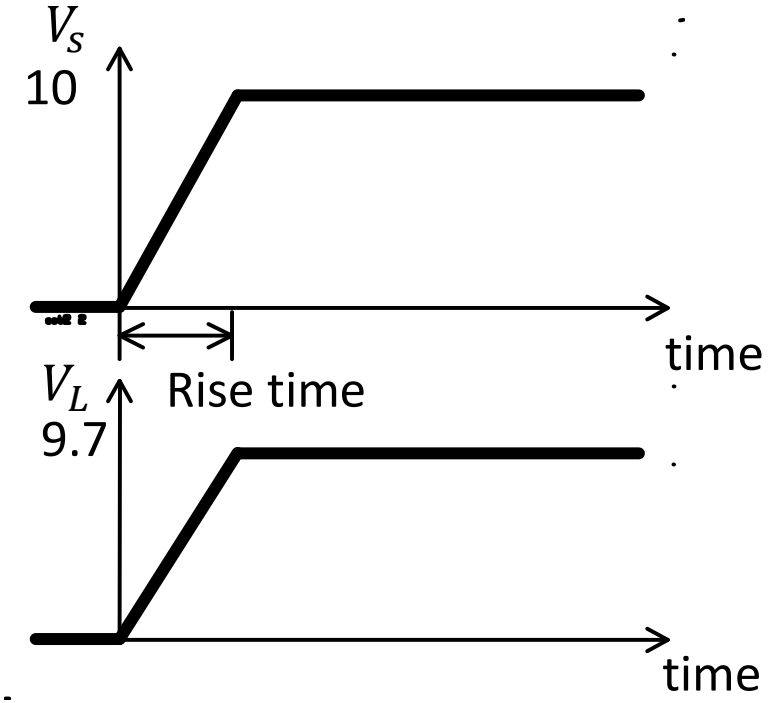
There no time delay at the output: when the source rises from 0 to 10 volts, the output simultaneously rises to 9.7 volts.



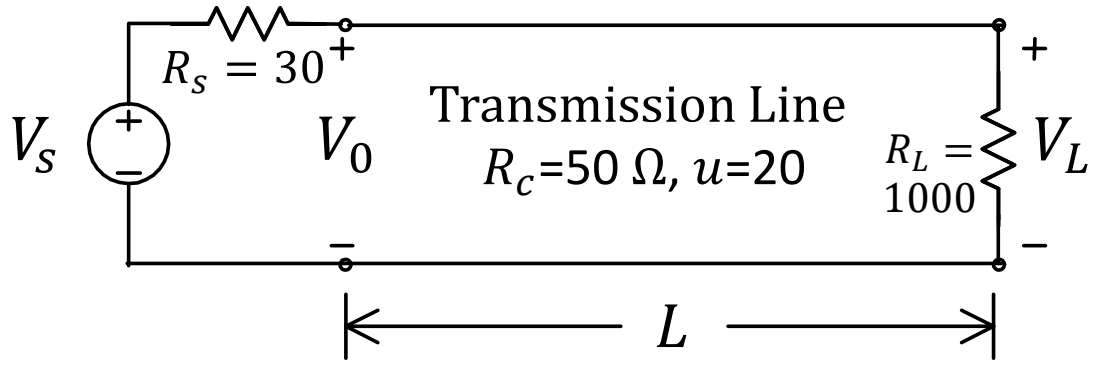
Accounting for Rise Time

- Suppose the clock speed is 2 GHz so the period is 0.5 ns.
- Suppose the rise time is 1/10 of the period, or 0.05 ns.
- If the interconnection path on the circuit board depends as a ideal short circuit, then the output is an exact copy of the input, with amplitude 9.7 volts.





Accounting for Time Delay



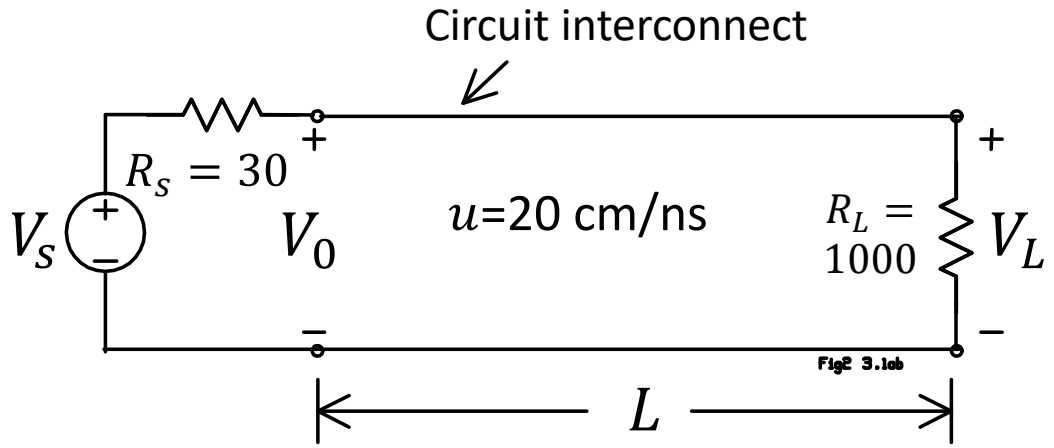
- Suppose the speed of travel on the interconnection path is $u = 20$ cm/ns:
  - This is a typical figure for real circuit boards
  - The speed-of-light in space is $c = 30$ cm/ns.
- We will see later that we need to know the "characteristic resistance" of the interconnection path, so assume it is $R_c = 50$ ohms.

The time taken to travel *L* meters at a speed of *u* m/s is $T = \frac{L}{u}$.

Three cases:

- Short interconnection path (1 mm)
- Intermediate length (1 cm)
- Long interconnection path (10 cm)

Short interconnection path:



$L = 1$ mm

Time delay: $T_d = \frac{L}{u} = \frac{0.1}{20} = 0.005$ ns

Rise time: $T_r = 0.05$ ns

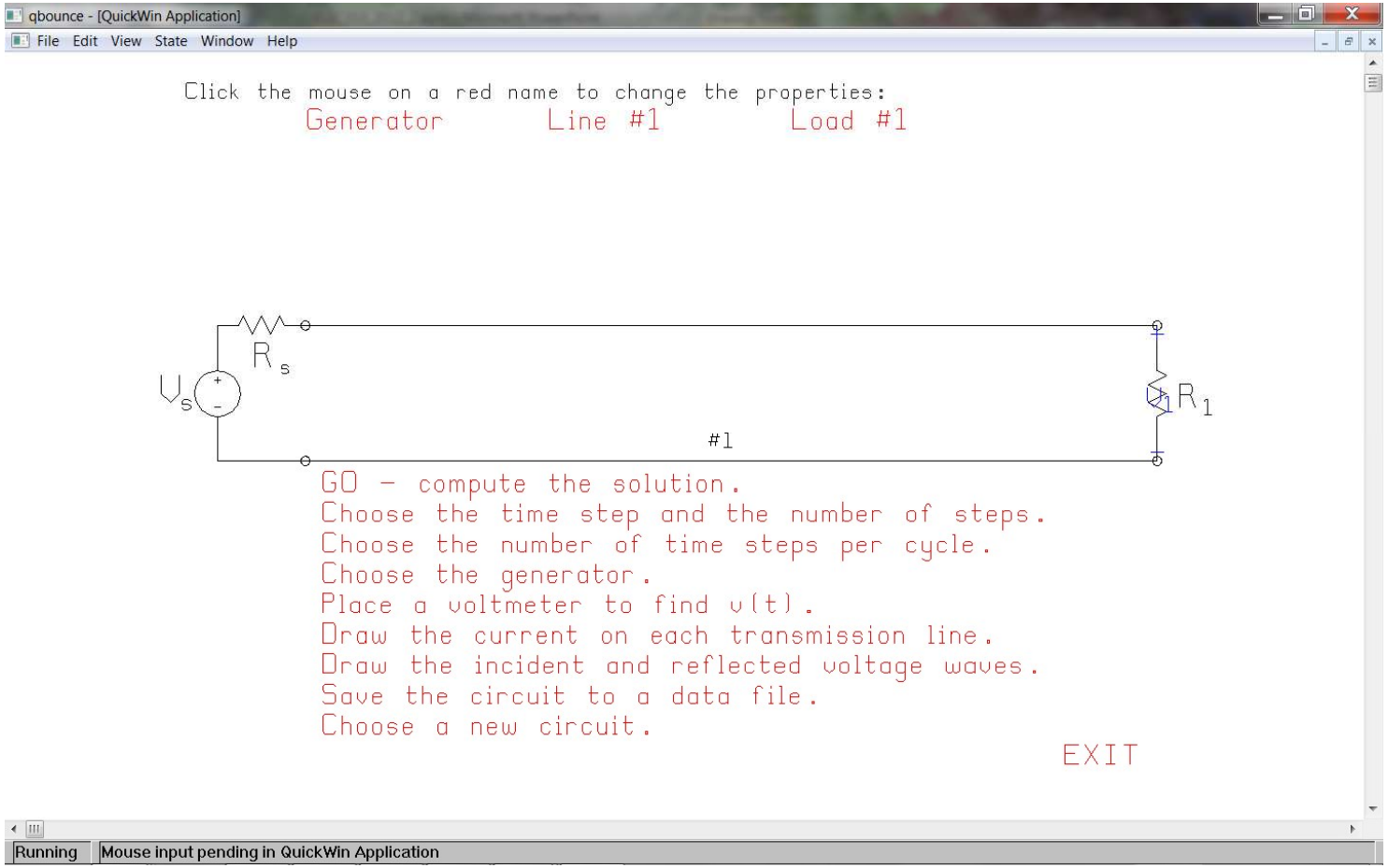
Rise time >> time delay

The "**rise length**" is defined as the distance travelled in one rise time.
The "**rise length**" is $L_r = uT_r$.
The rise length is also called the "length of the leading edge".
It is useful to compare the rise length with the length of the transmission line.

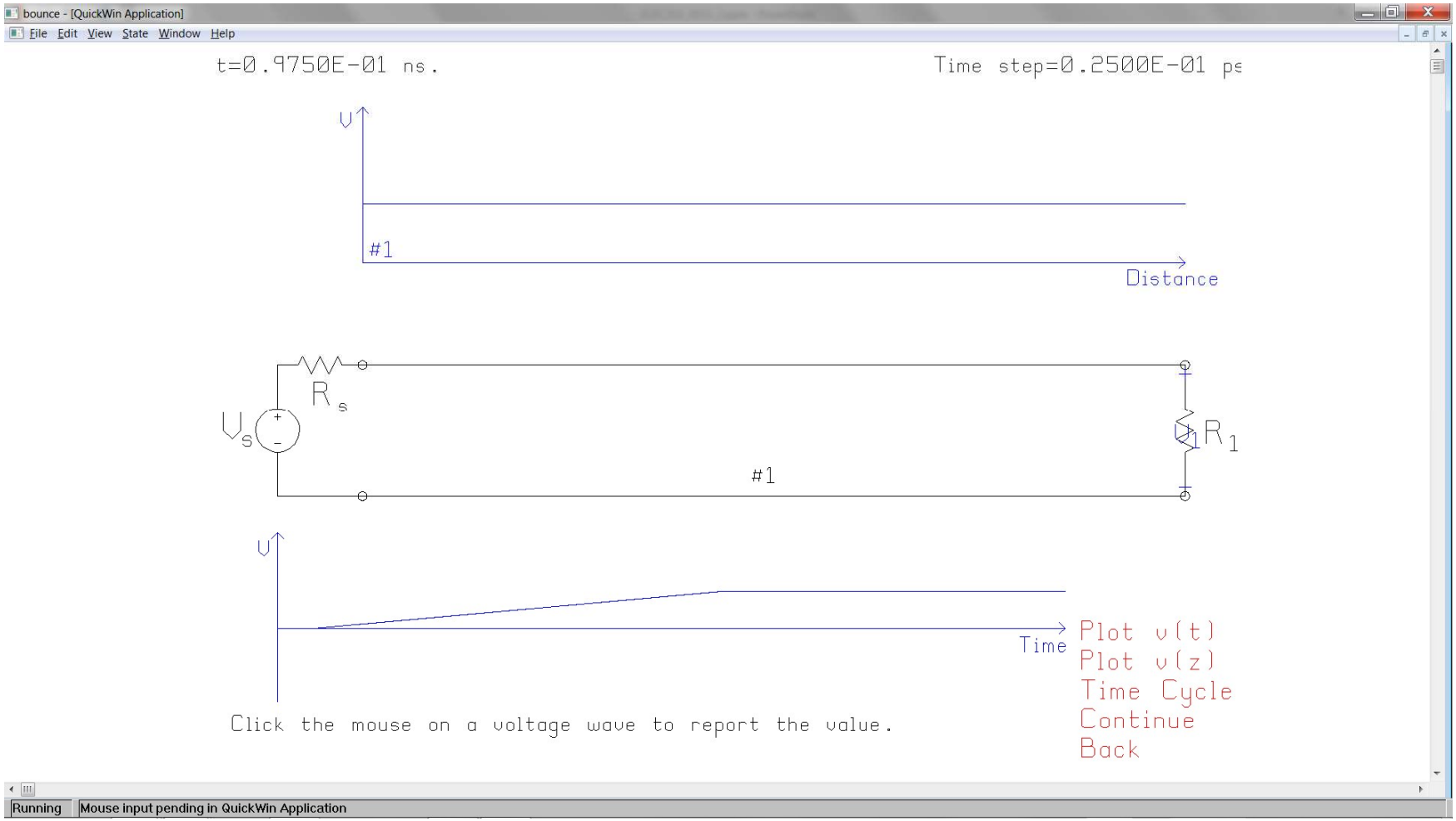
The rise length is $L_r = uT_r$ = 20x0.05= 1 cm so $L_r \gg L$.

Rise length >> path length

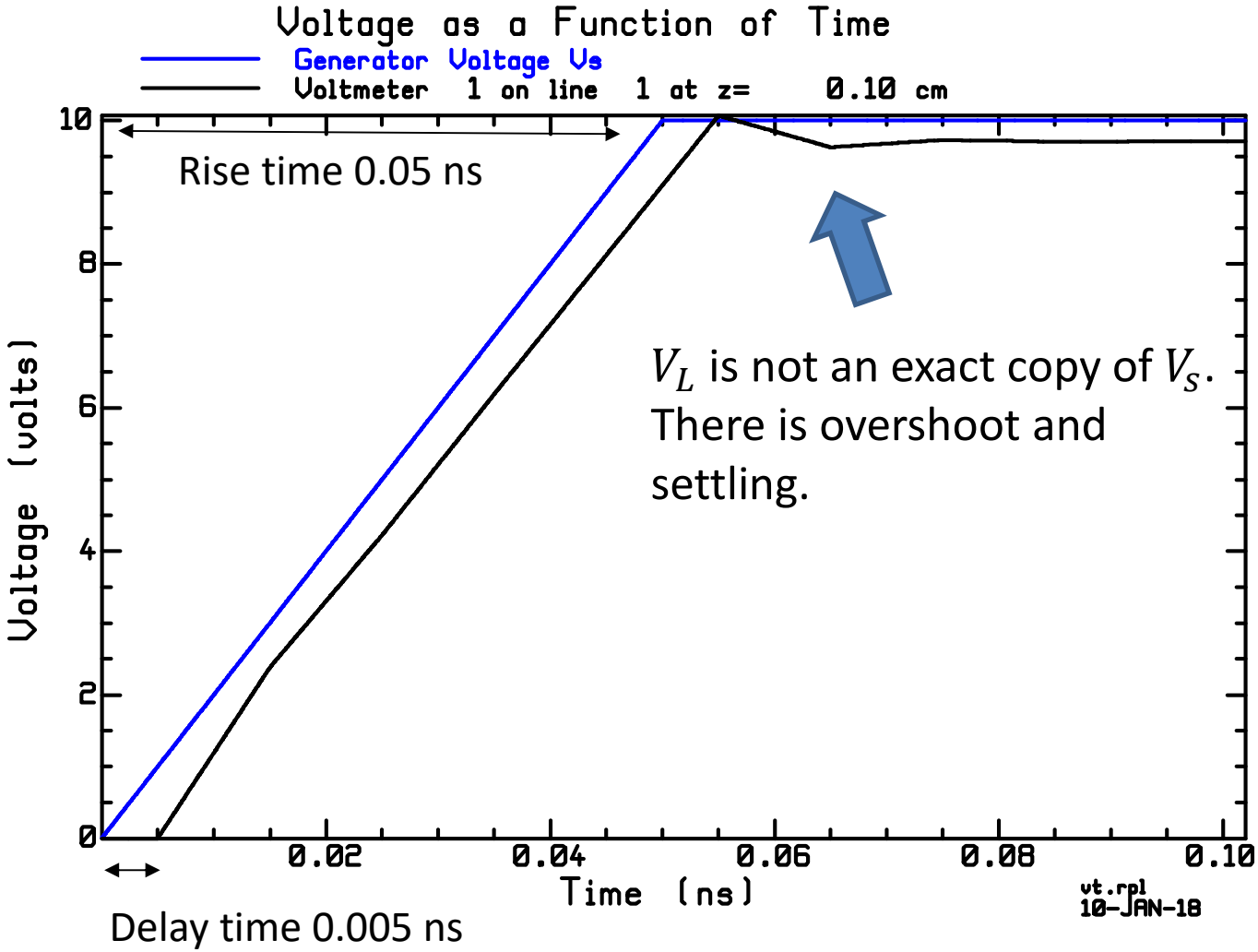
BOUNCE Simulation:



Generator: V_S=10 volts, R_S=30 ohms, rise time 0.05 ns
Line: L=0.1 cm, R_C=50 ohms, u=20 cm/ns
Load: R_L=1000 ohms

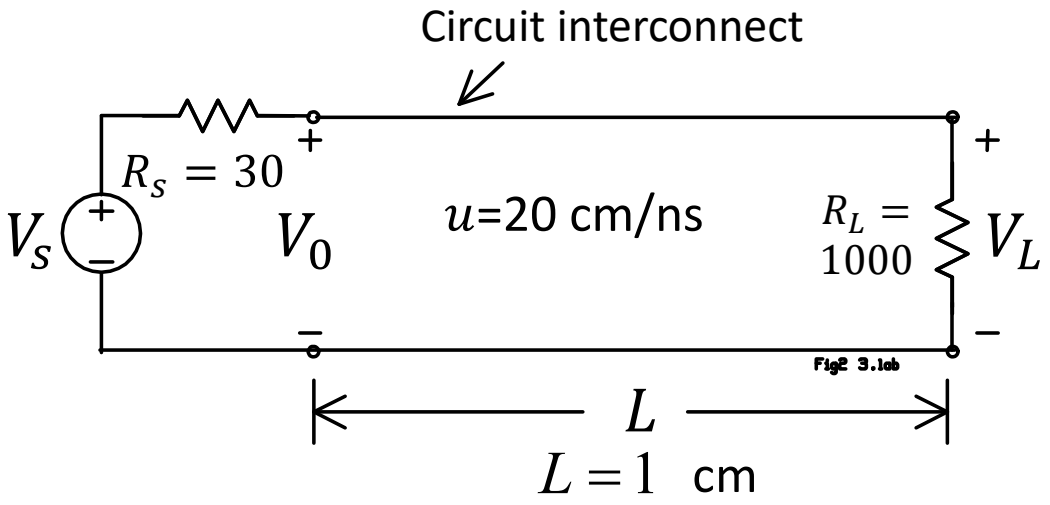


The voltage on the transmission line is almost constant over the whole length of the transmission line as time advances.



- The rise time (0.05 ns) is much, much longer than the delay time (0.005 ns).
- The "rise length" (1 cm) is much, much longer than the length of the circuit path (0.1 cm).
- Use "lumped" circuit analysis.

Interconnection path that is not short but not long either:



Time delay: $T_d = \frac{L}{u} = \frac{1}{20} = 0.05$ ns

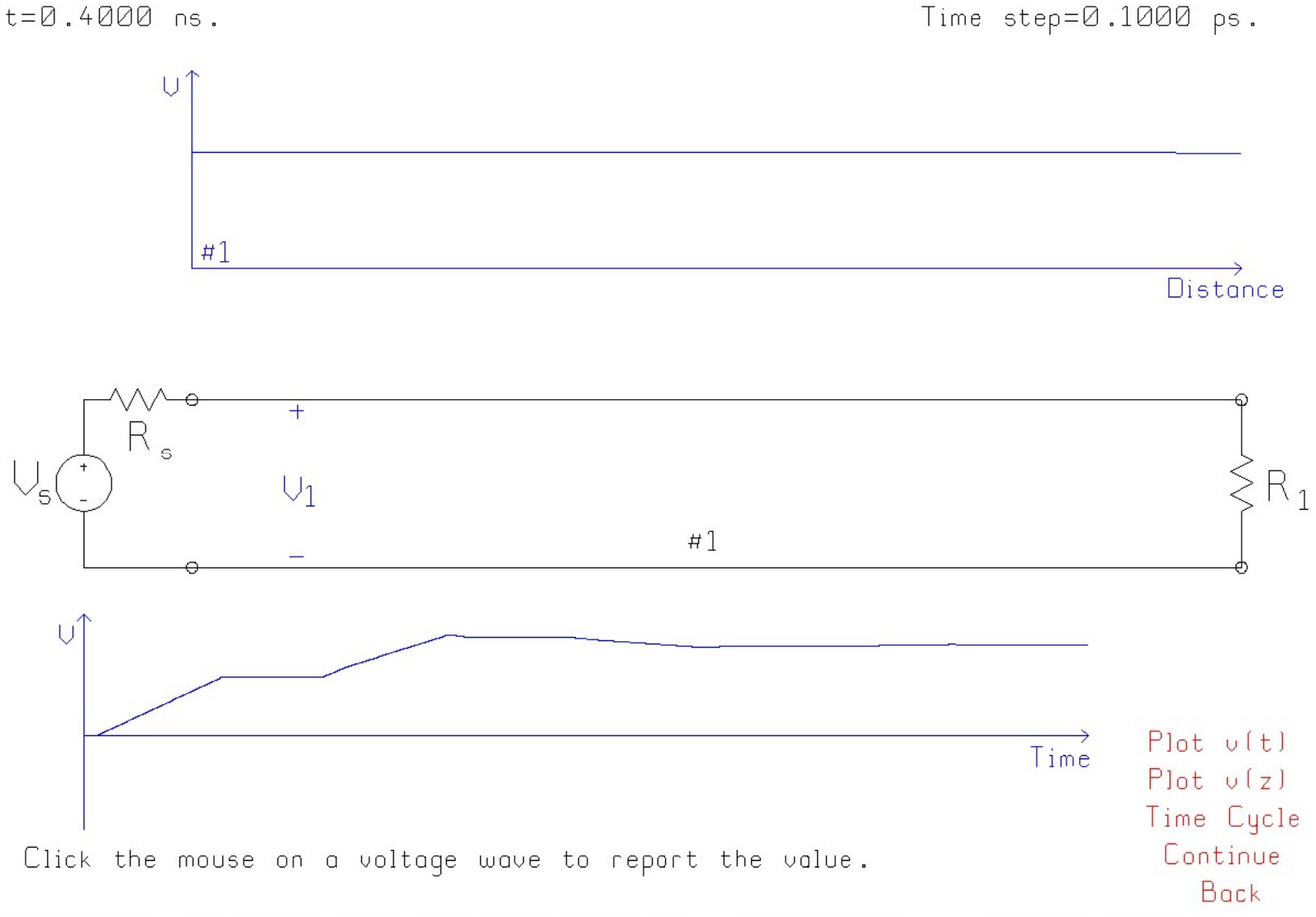
Rise time: $T_r = 0.05$ ns

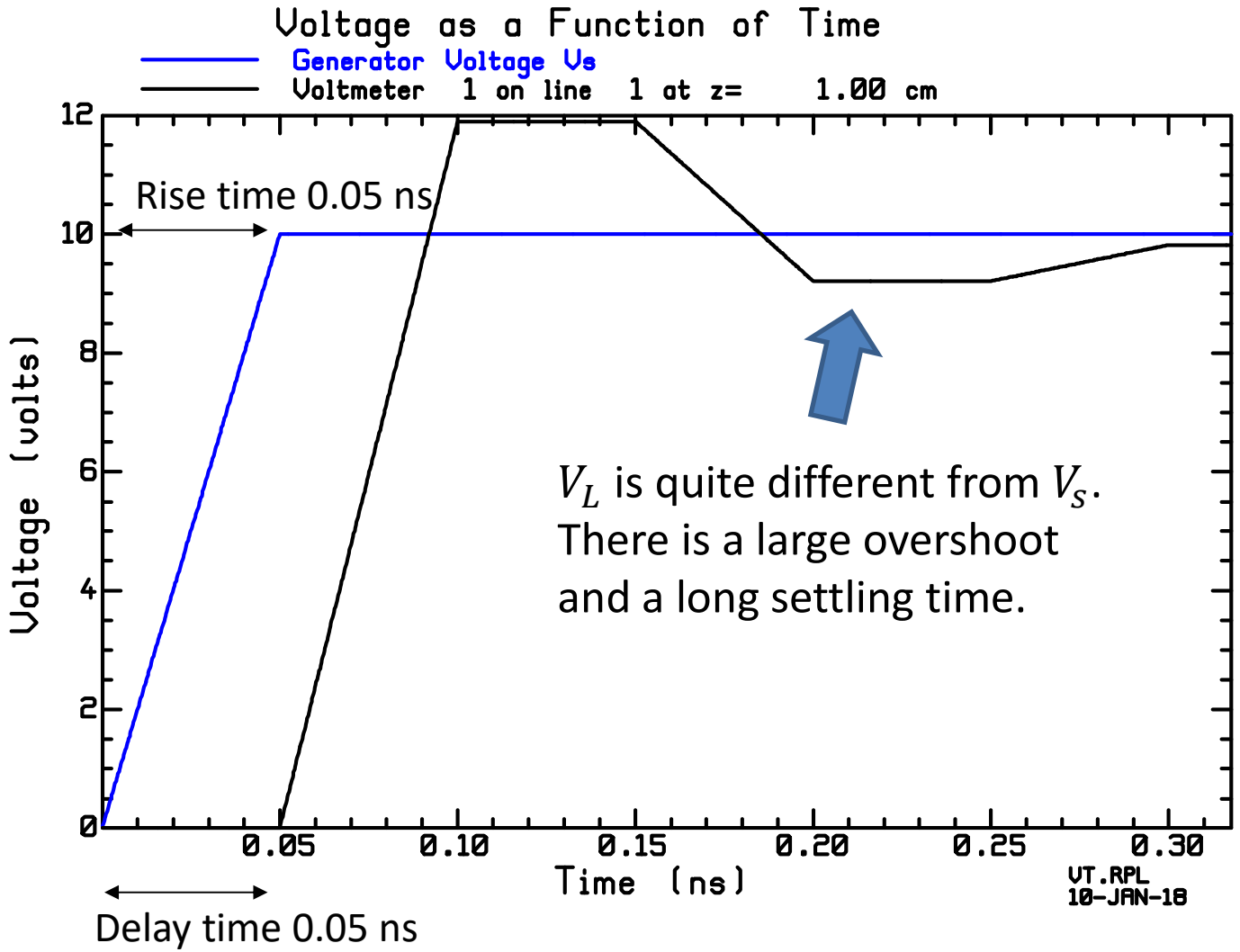
Rise time = time delay

The rise length is $L_r = uT_r$ = 20x0.05= 1 cm so $L_r = L$

Rise length = path length

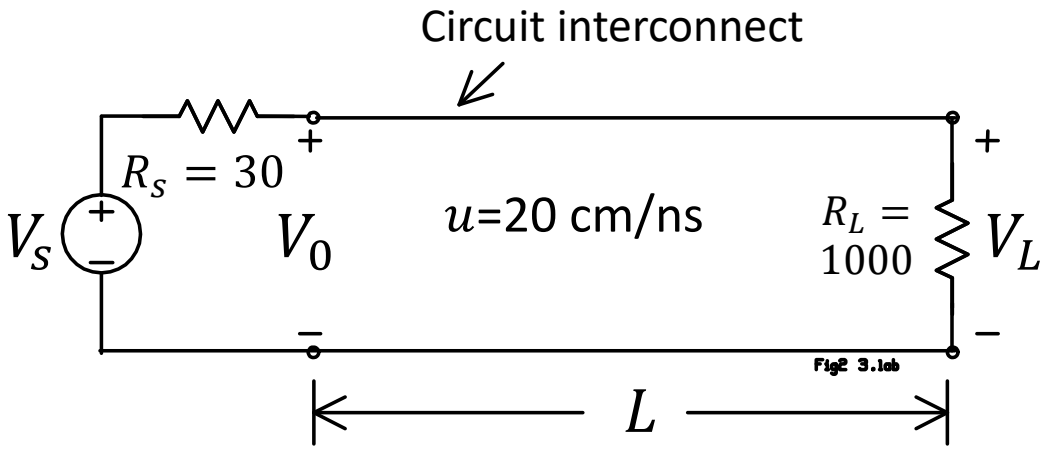
BOUNCE Simulation:





- The rise time (0.05 ns) is equal to the delay time (0.05 ns).
- The "rise length" (1 cm) is equal to the length of the circuit path (1 cm).
- Cannot use "lumped" circuit analysis!

Long interconnection path:



$$L = 10 \text{ cm}$$

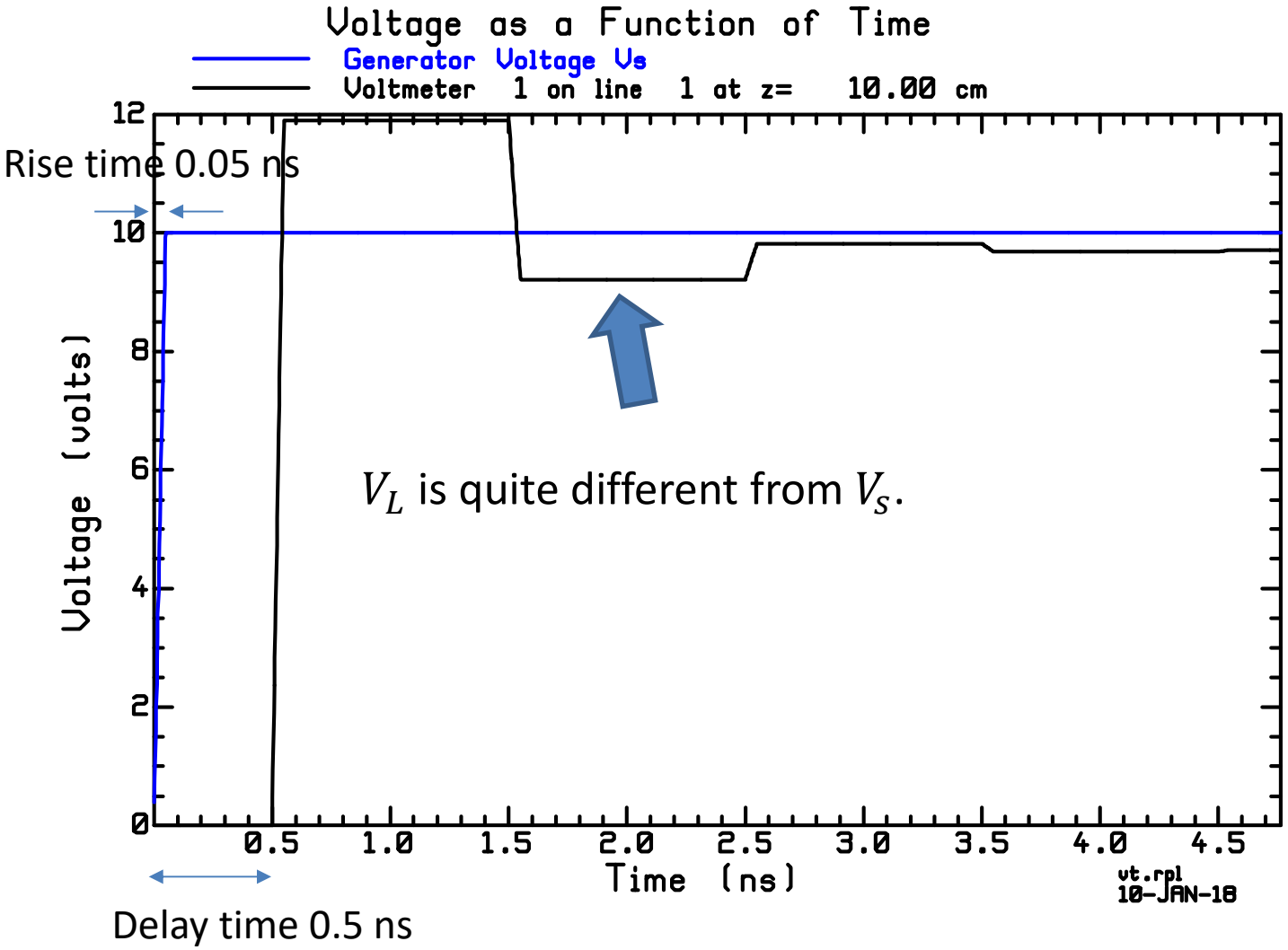
Time delay: $T_d = \frac{L}{u} = \frac{10}{20} = 0.5$ ns

Rise time: $T_r = 0.05$ ns

Rise time << time delay

The rise length is $L_r = uT_r$ = 20x0.05= 1 cm so $L_r >> L$

Rise length << path length



•The rise time (0.05 ns) is much much shorter than the delay time (0.5 ns).

•The "rise length" (1 cm) is much much shorter than the length of the circuit path (10 cm).

Rule of Thumb

Inan, Inan and Said page 14

- If the rise time is more than 6 times the delay time, then use lumped circuit analysis.
- If the rise time is less than 2.5 times the delay time, then use distributed circuit analysis.

$$\text{If } \frac{T_r}{T_d} > 6 \text{, use lumped circuit analysis.} \quad \text{(Short time delay case.)}$$

$$\text{If } \frac{T_r}{T_d} < 2.5 \text{, use distributed circuit analysis.} \quad \text{(Long time delay case.)}$$

In terms of rise length:

$L_r > 6L$ Rise length much longer than line length:
Use lumped circuit analysis.

$L_r < 2.5L$ Rise length shorter than 2.5 x line length:
Use distributed circuit analysis.