ELEC353 Lecture Notes Set 1

There is a tutorial on Friday January 11! You will do the first "workshop problem" in the tutorial. Bring a calculator.

The course web site is:
www.ece.concordia.ca/~trueman/web_page_353.htm

- The course outline
- The lecture notes
- The homework assignment each week
- A set of practice problems with solutions
- Software: BOUNCE, TRLINE, WAVES

The homework assignments are posted on the course web site.

Homework #1: Do this assignment by January 18th, 2019.
Homework #2: Do this assignment by January 25nd.

Reading Assignment

- Read Inan, Inan and Said Chapter 1 about lumped and distributed circuit analysis.
- Read inan, Inan and Said Chapter 2 about transmission lines. We will cover Chapter 2 over the next four weeks.

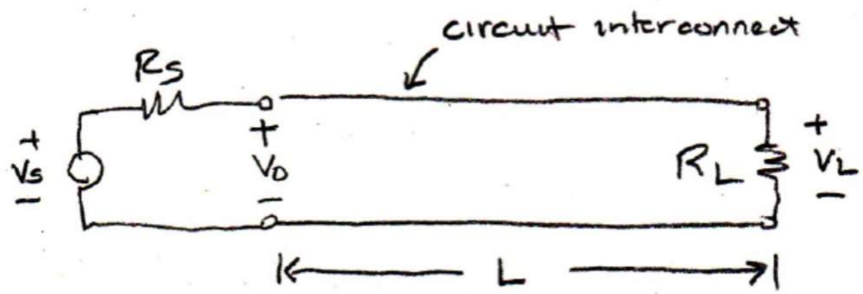
Homework #1

Fetch the homework from the course web site:
www.ece.Concordia.ca/~trueman/web_page_353.htm
Do Homework #1 by January 18.

ELEC 353 – Assignment #1

Note: In ELEC353, assignments are not handed in. Do the assignments week-by-week and then evaluate your work in comparison to the solution.

1. What is an "ideal" short circuit?

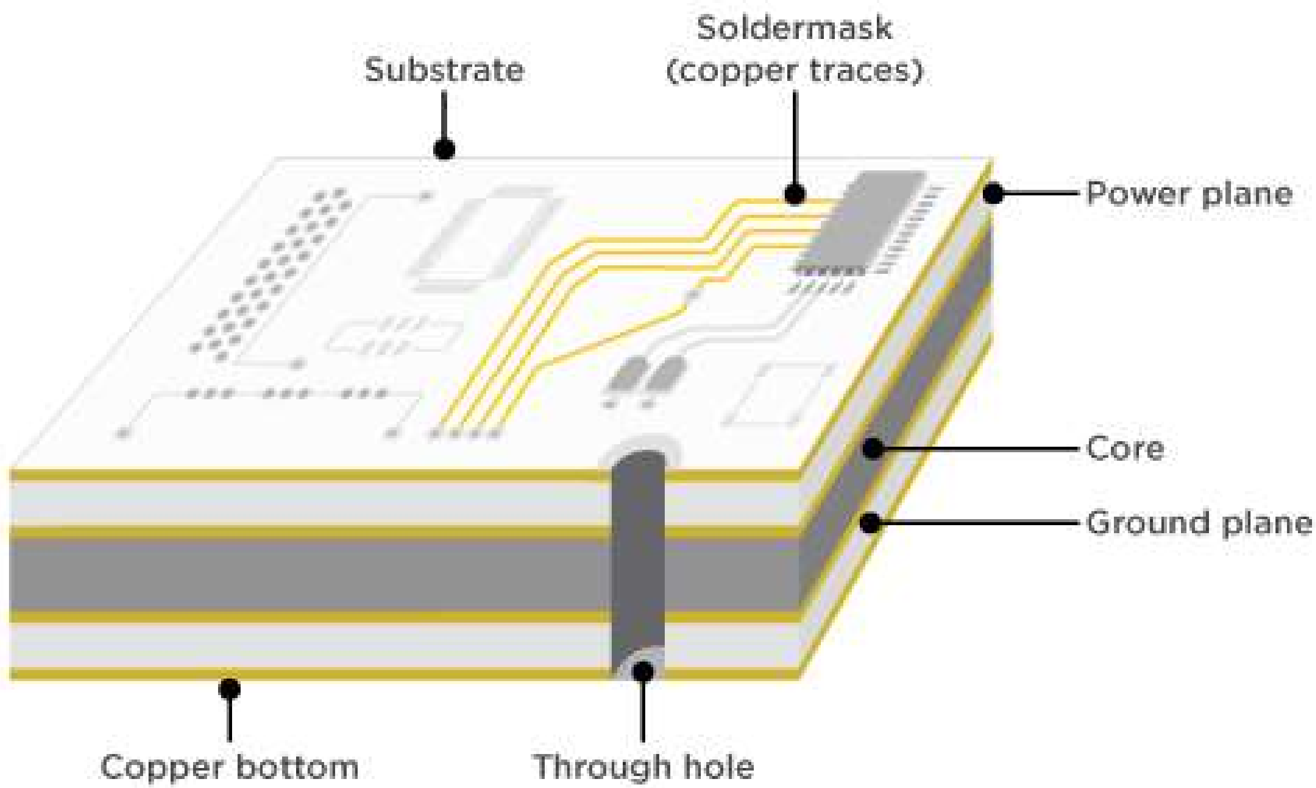


2. In the circuit shown above, V_s and R_s are the Thevenin equivalent circuit for the output of a logic chip. The output of the chip is connected to a load R_L with a circuit interconnect of length L. The load represents the input of another logic chip. The source is step-function generator that steps up from 0 volts to $V_s = 10$ volts at $t = 0$, and has internal resistance $R_s = 30$ ohms. The load resistor is $R_L = 1000$ ohms. Find the voltage across the generator terminals $v_0(t)$ and across the load terminals $v_L(t)$. Treat the circuit interconnect as an *ideal short circuit*. Plot the voltage at the source terminals and at the load terminals as a function of time. This problem is trivially simple and represents the "ideal"

PART 1
Waves on Circuit Interconnections in the Time Domain

- Time delay
- When is time delay significant?
- Wave equation and travelling waves
- Timing problems and intersymbol interference.

Printed Circuit Board (PCB)



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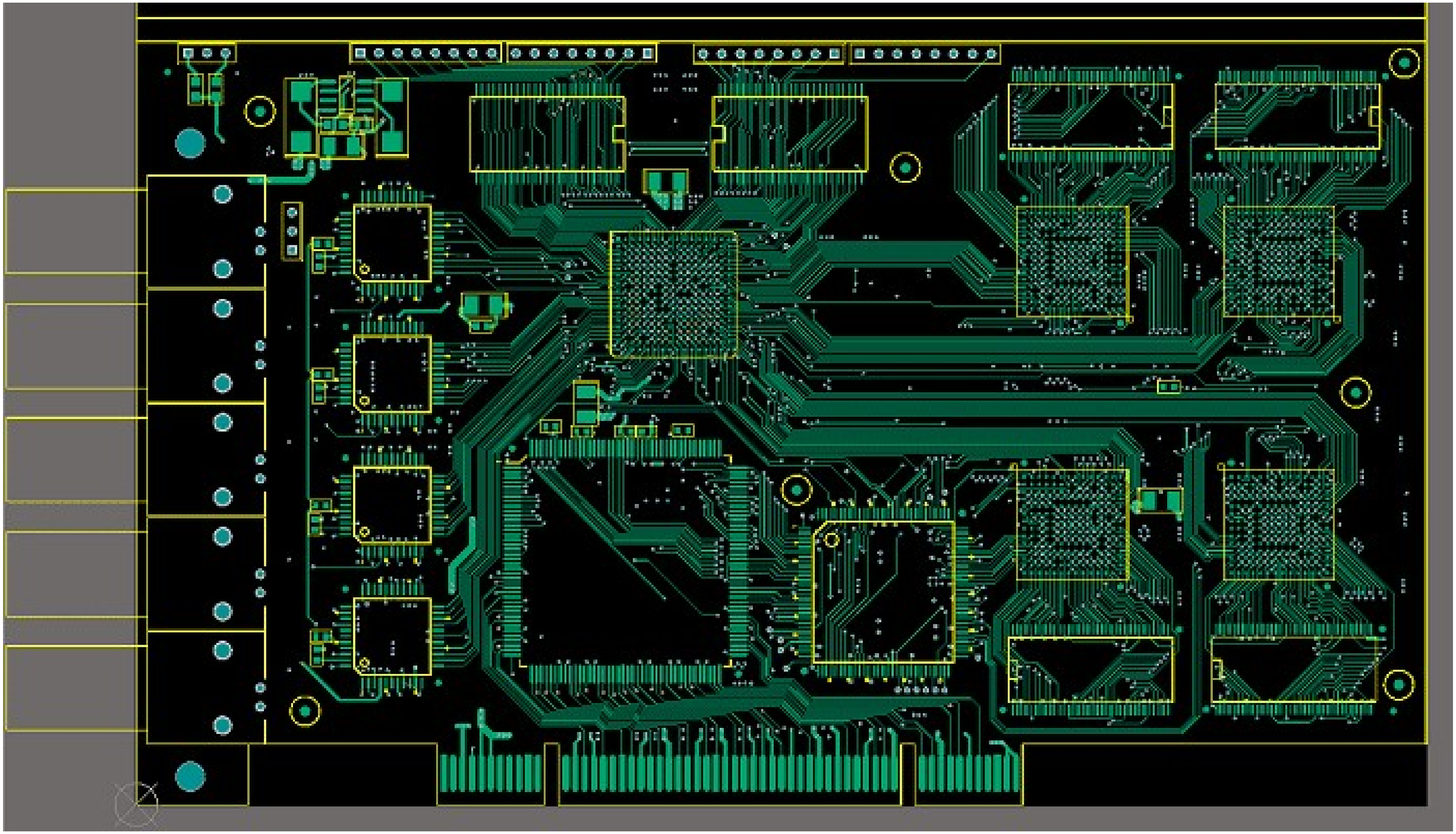
Printed Circuit Boards can have 100s or even 1000s of circuit paths:



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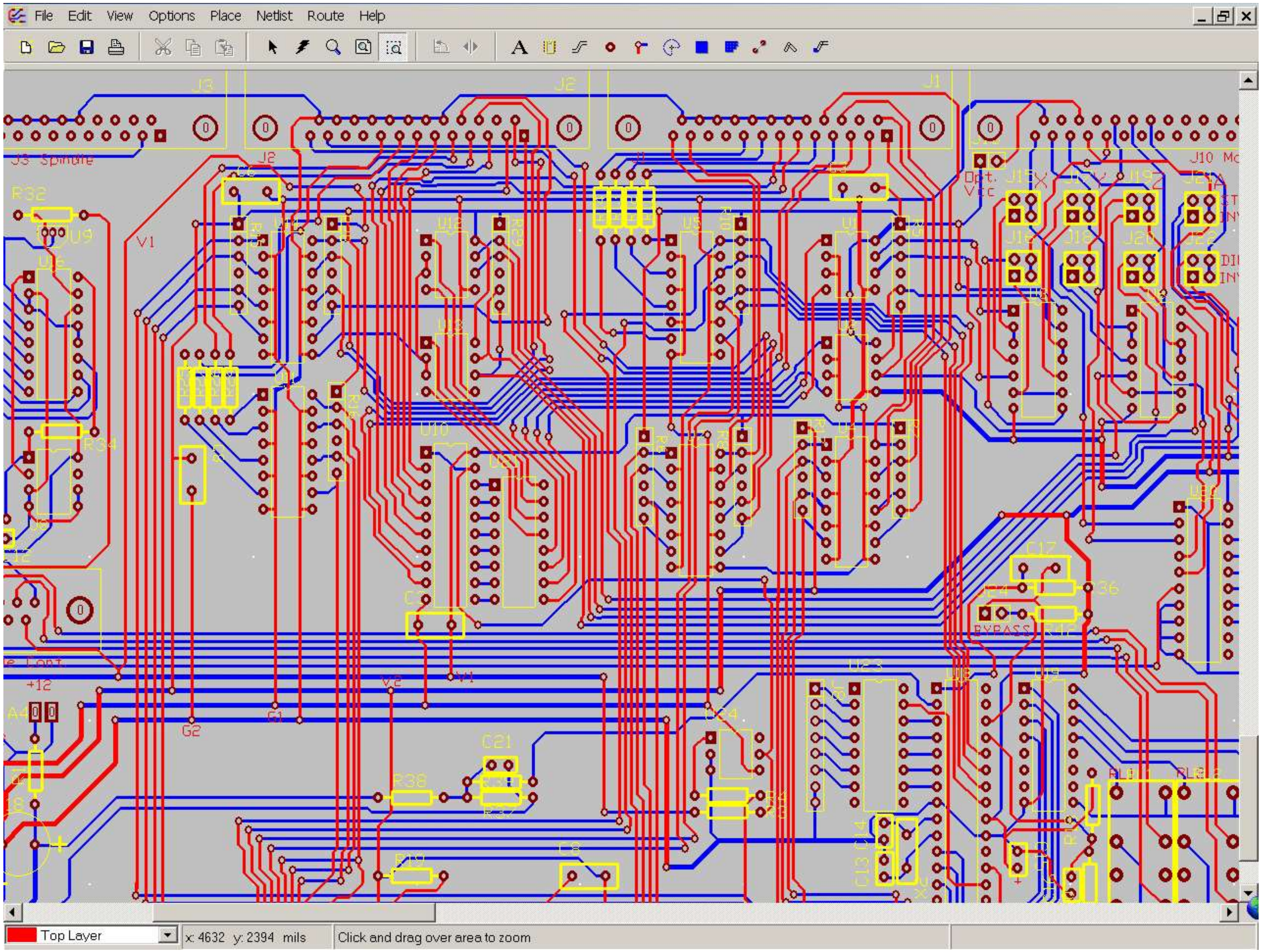
Two Layer Printed Circuit Board:



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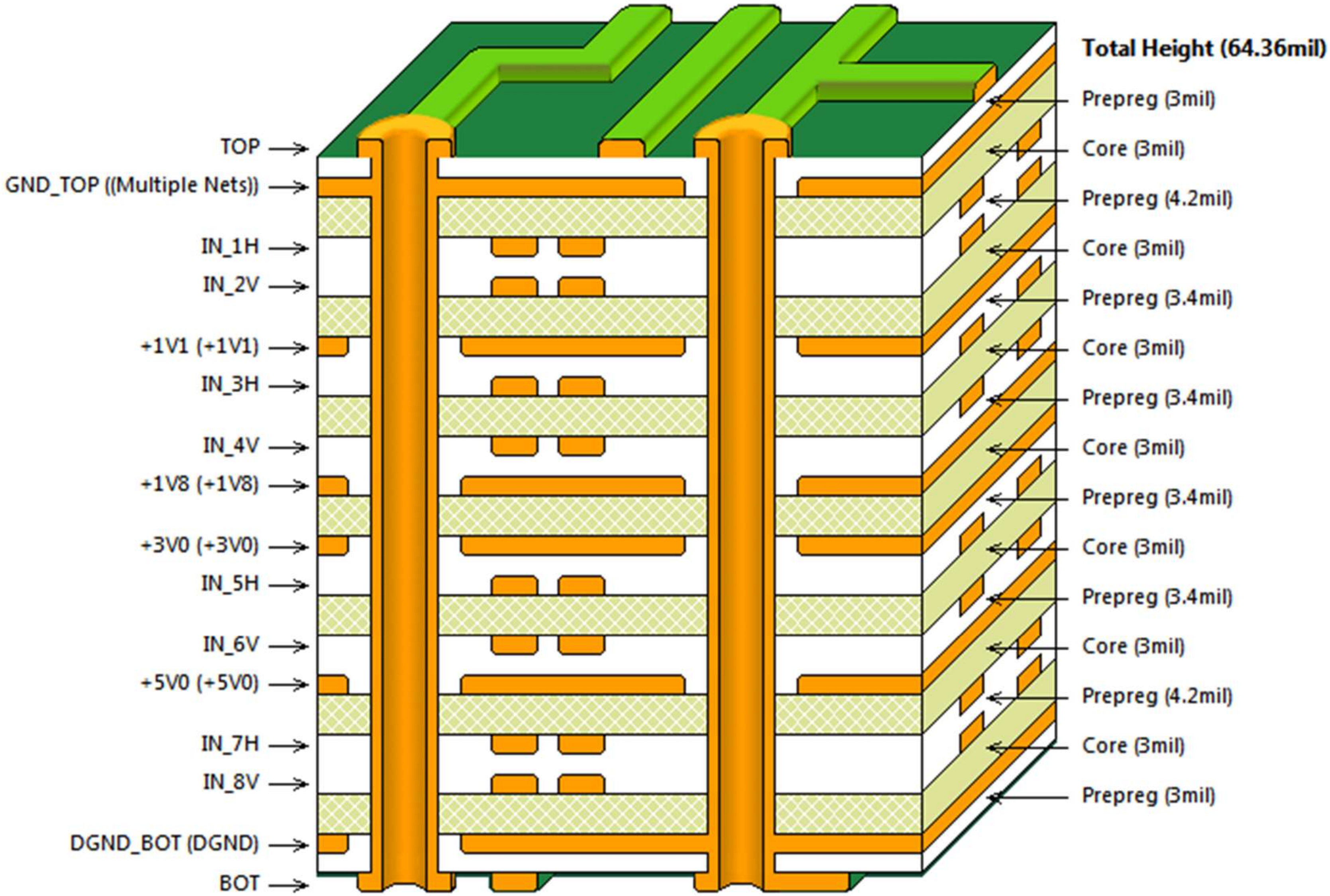
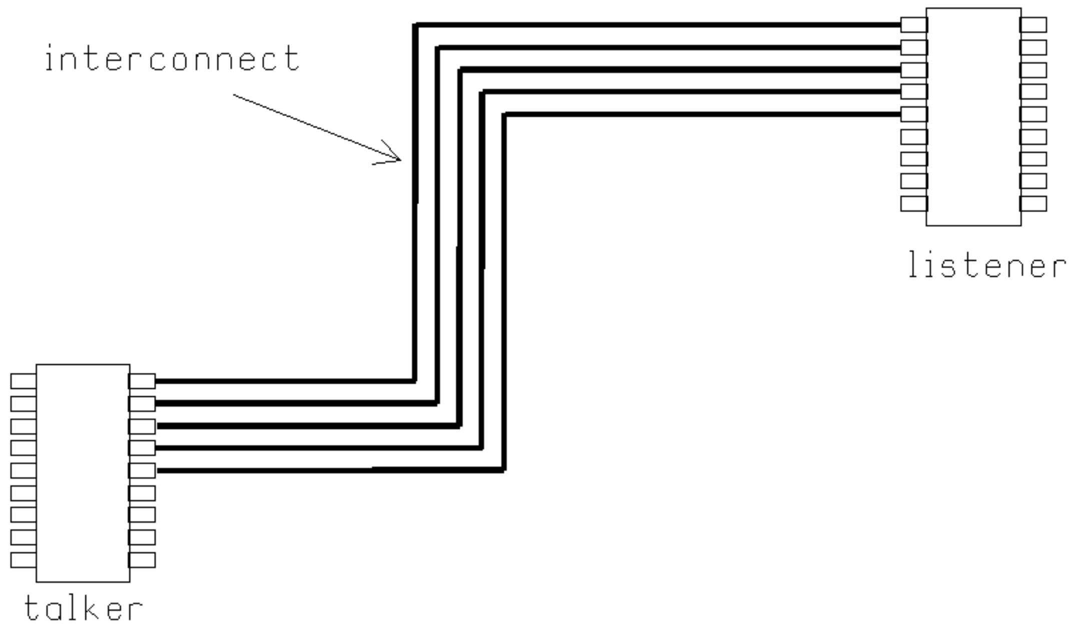
Multi-Layer Printed Circuit Board includes Signal Layers, Power Distribution Layers and Ground Layers



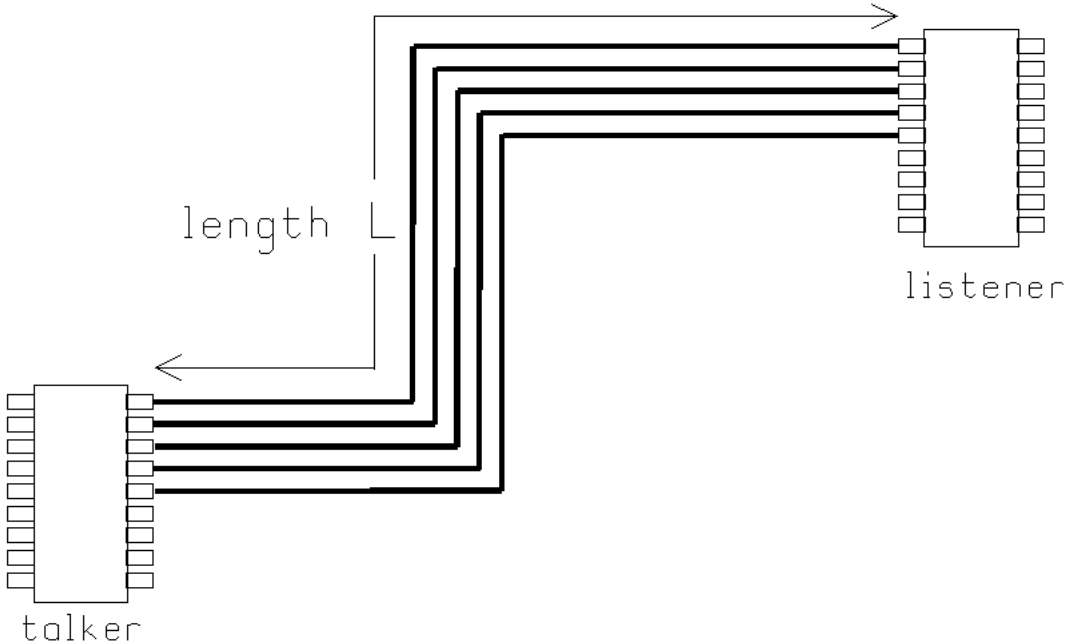
https://electronics.stackexchange.com/questions/82869/on-referencing-power-planes-and-return-current-paths

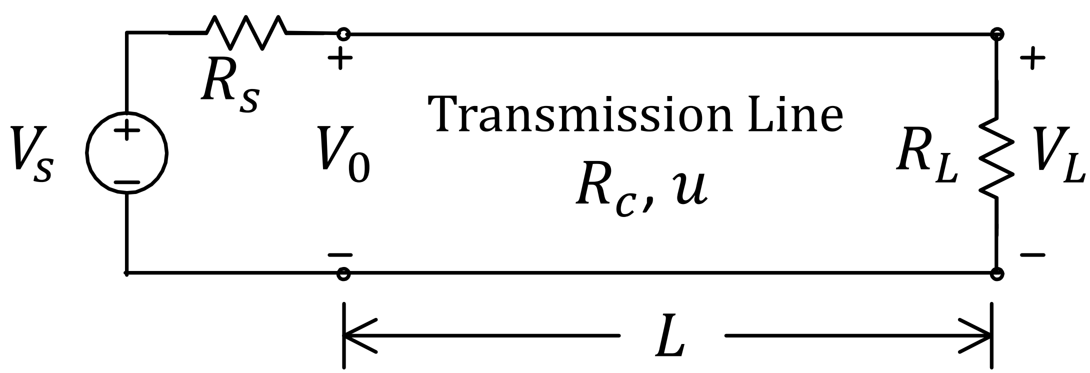
Point of View in ELEC 353



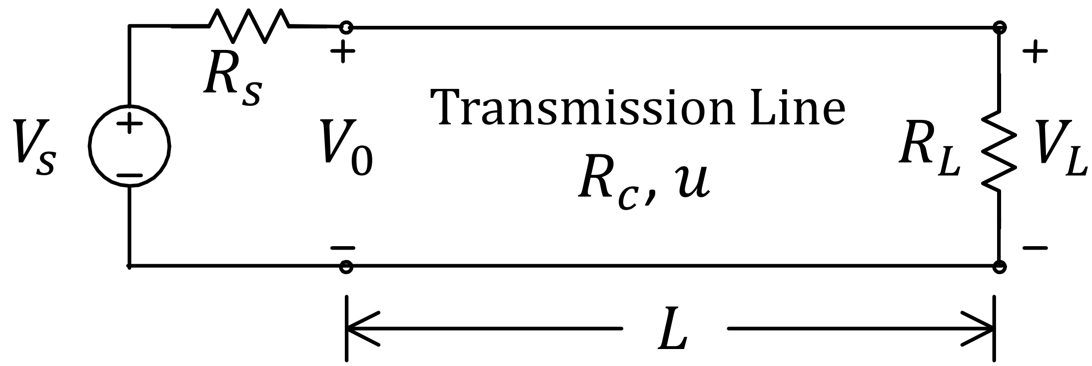
- Every "interconnection" path on a circuit board is a communications channel.
- Each "interconnect" is characterized by:
  - Time domain: the impulse response $h(t)$
  - Frequency domain: the transfer function $H(j\omega)$

Equivalent Circuit for One Interconnection





Typical Response of a Circuit Interconnection



Parameters:

V_s = step function from 0 to 10 volts starting at t=0

R_s = internal resistance of the "talker" chip. Use 1 ohm.

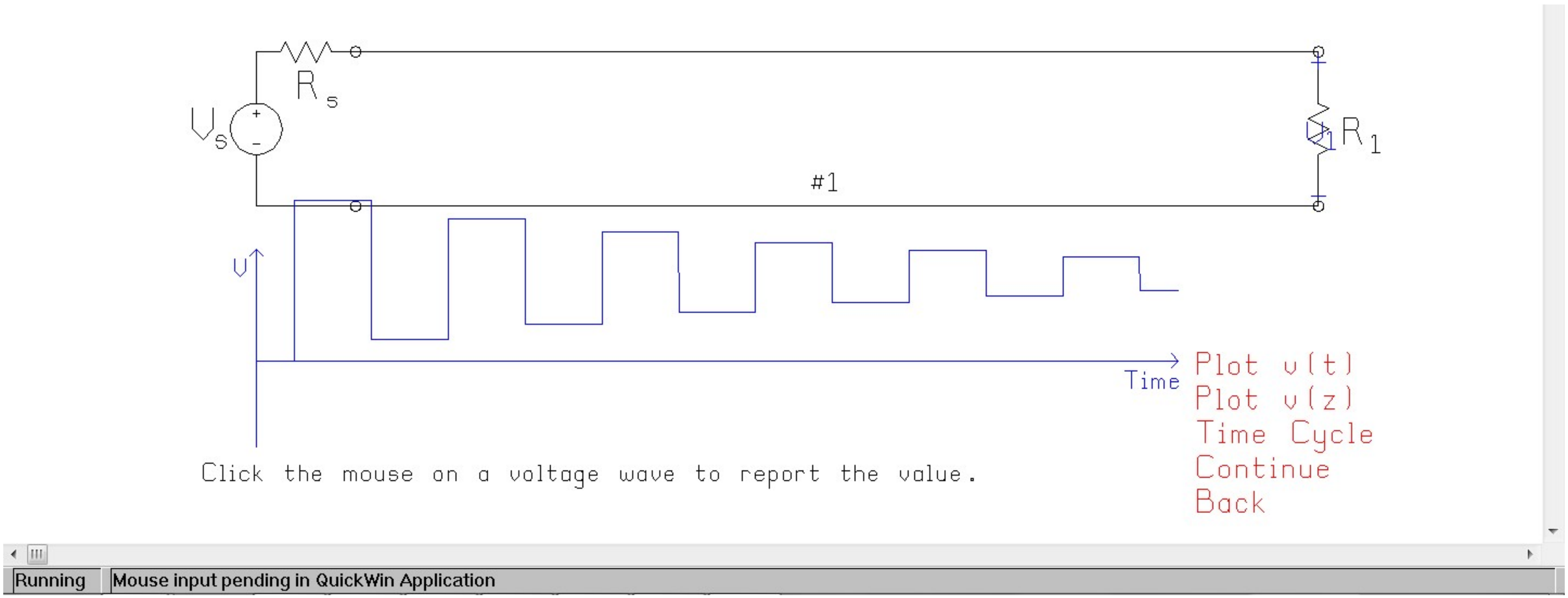
L = length of the interconnection path. Use 2 cm.

$Z_o = R_c$ = "characteristic resistance" of the interconnection path (see later lectures). Use 50 ohms.

u = speed of travel of a voltage on the interconnection path (see later lectures). Use 20 cm/ns .

R_L = input resistance of the "listener" chip, which is high for CMOS logic. Use 1000 ohms.

Step Response



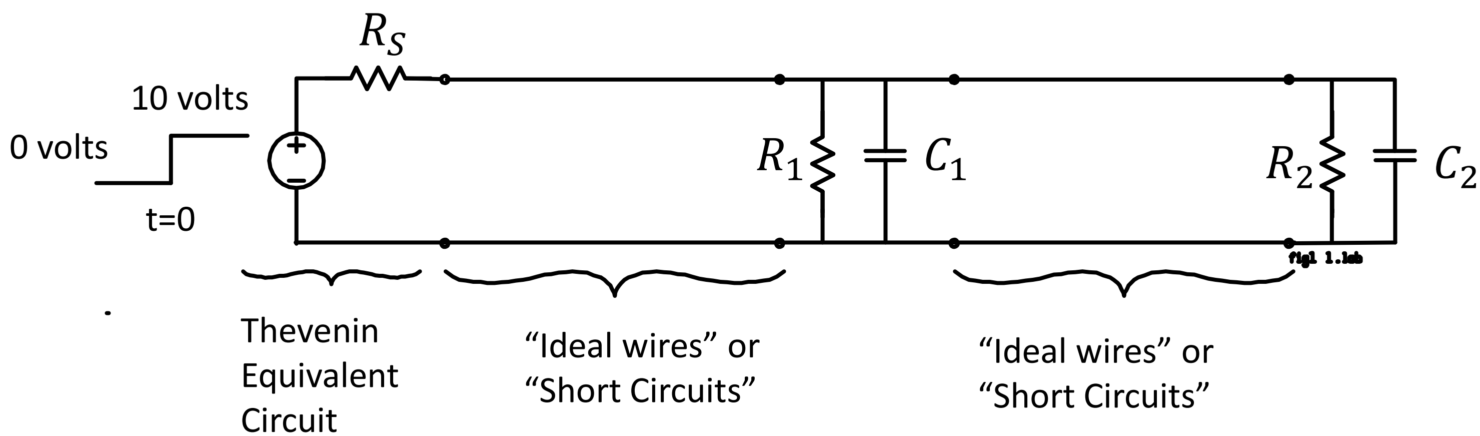
The slide shows one frame from an animation of the response of the circuit, obtained from the BOUNCE program.

Questions:

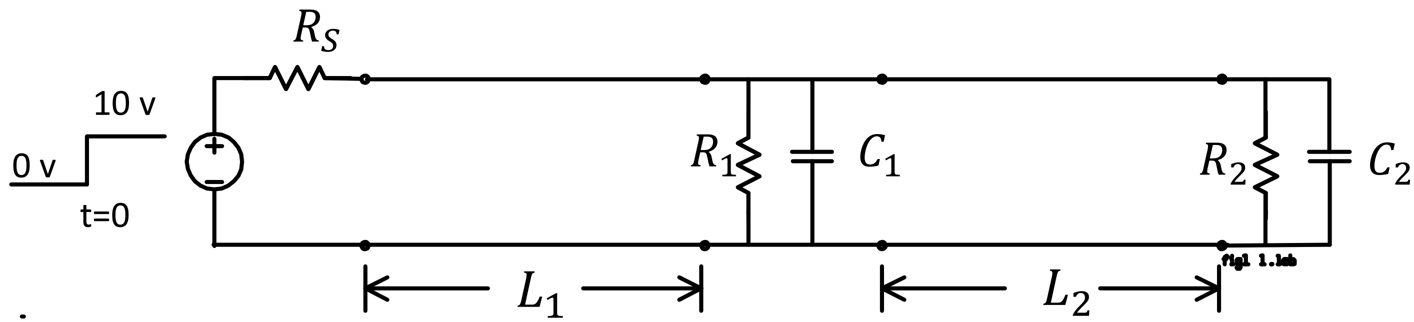
- What is the physics of this behavior?
- How does it arise from circuit analysis?
- How do you solve circuits such as this one?
  - Time domain?
  - Frequency domain?
- What determines the speed of travel?
- What is “characteristic resistance”?
- How do you design the circuit to avoid this behavior?

Lumped circuit analysis or distributed circuit analysis?

Lumped circuit analysis: ELEC 273



- R, L and C are discrete components.
- Circuit paths are "ideal" short circuits.
- There is *zero time delay* for a voltage to go from one end of a circuit to the other.



Time Delay

$$T_1 = \frac{L_1}{u}$$

Time Delay

$$T_2 = \frac{L_2}{u}$$

Distributed circuit analysis:

- Circuit paths are *not ideal short circuits*.
- Circuit paths have capacitance-per-unit-length and inductance-per-unit length
- Consequently circuit paths have a propagation velocity u m/s and so have *time delay* $T = \dfrac{L}{u}$, where L is the length of the circuit path.
- Voltages and currents behave as "traveling waves".
- These circuits are called "transmission line circuits".
- **Homework:** read about "distributed circuit analysis" in Inan and Inan.

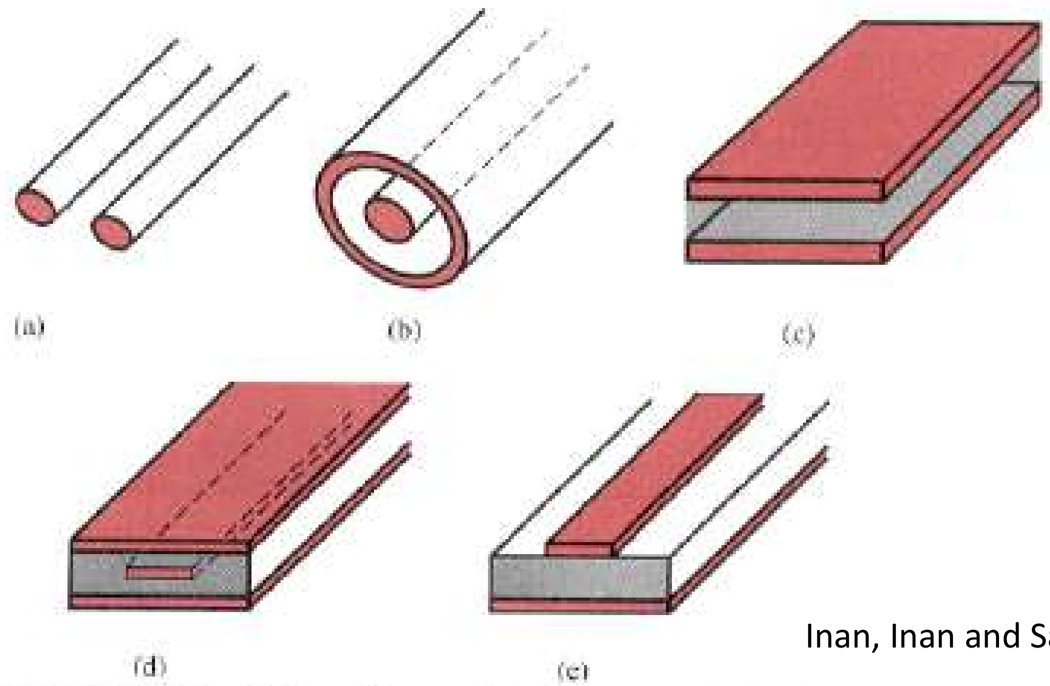
On a computer circuit board, circuit paths that connect the various chips have inductance-per-unit-length and capacitance-per-unit-length and therefore may have to be analyzed by distributed circuit analysis.

Learning objectives:

- What gives rise to capacitance-per-unit-length? To inductance-per-unit-length?
- How do we account for capacitance and inductance?
    - "distributed" circuit analysis.
- Learn that the voltages on a circuit interconnect behave as *travelling waves*.
- Learn to solve distributed circuits in the **time domain:**
    - Reflections at loads, re-reflections at the generator
- Learn to solve distributed circuits in the **frequency domain:**
    - Reflected waves and standing waves

Types of Transmission Lines

Inan, Inan and Said Sections
1.2 and 2.7



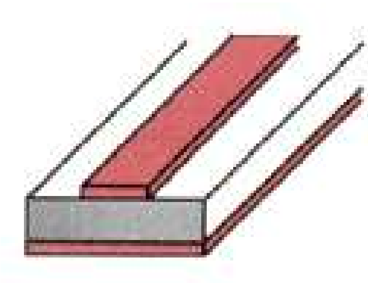
Inan, Inan and Said Fig. 2.1

FIGURE 2.1. **Different types of uniform transmission lines:** (a) parallel two-wire; (b) coaxial; (c) parallel-plate; (d) stripline; (e) microstrip.

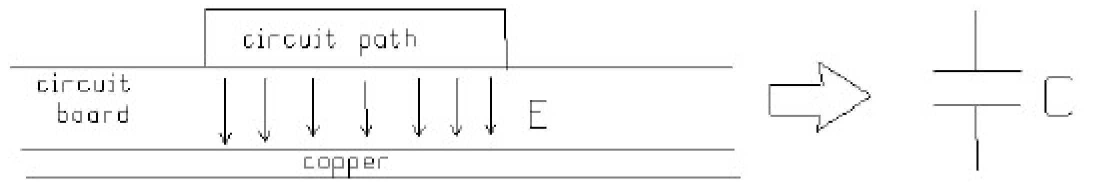
Transmission Line Properties

- Every transmission line has:
  - inductance-per-unit-length ℓ Henries/meter or H/m
  - capacitance-per-unit-length c Farads/meter or F/m
- Often ℓ and c are found by measurement in the lab.
- We can find formulas for ℓ and c for various transmission-line geometries in textbooks and handbooks-see Inan and Inan Section 2.7.

Capacitance and Inductance of a Transmission Line



Microstrip transmission line



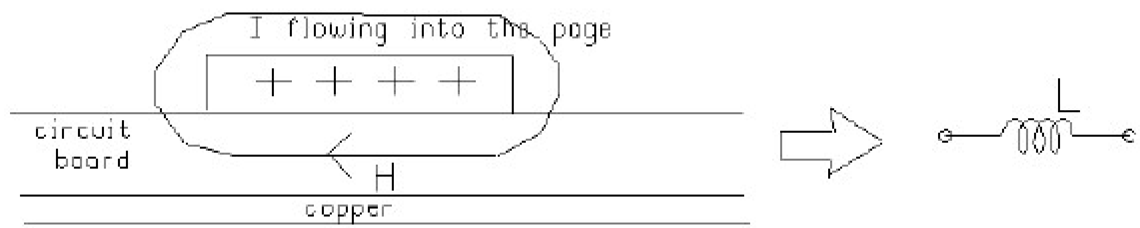
The capacitance is given by

$C = cp$ Farads

where

c =the capacitance-per-unit-length of the microstrip

p =the length of the interconnection path



The inductance of the interconnection path is given by

$L = \ell p$ Farads

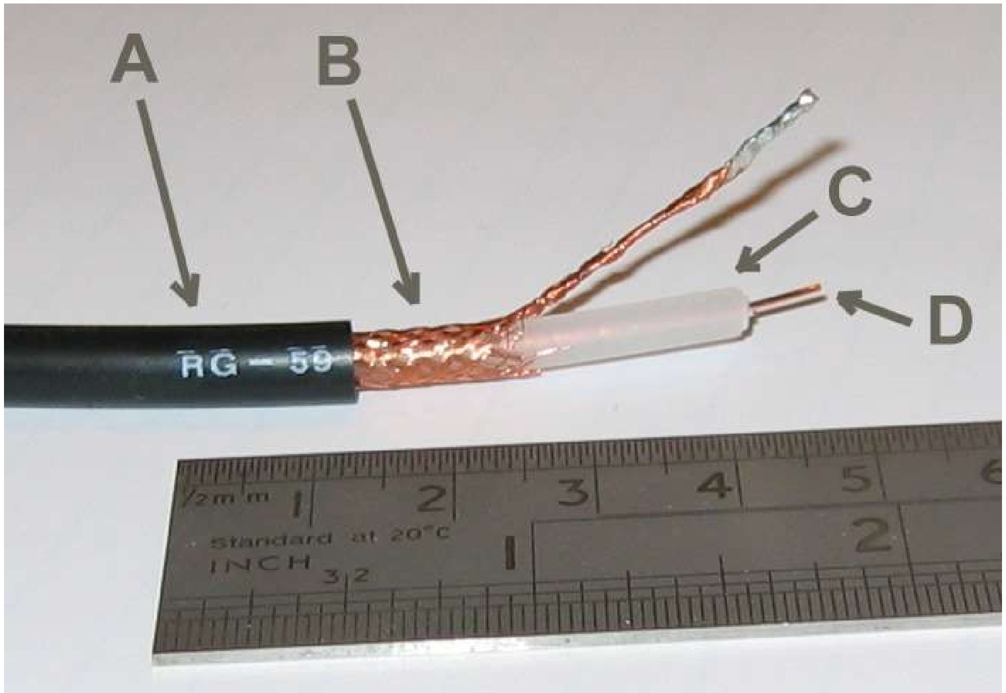
where

ℓ =the inductance-per-unit-length of the microstrip

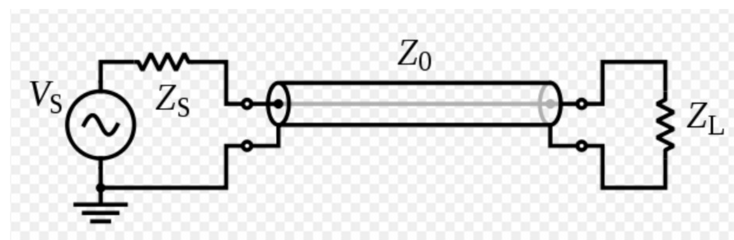
p =the length of the interconnection path

An interconnection path having capacitance-per-unit-length and inductance-per-unit-length is called a "transmission line".

Coaxial Cable Transmission Line

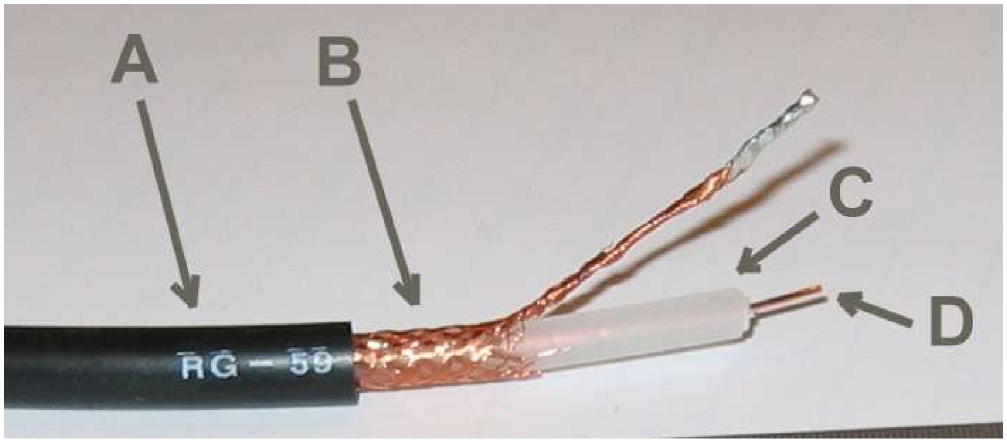


RG-59
A:Outer plastic sheath
B:Woven copper shield
C:Inner dielectric insulator
D:Copper core



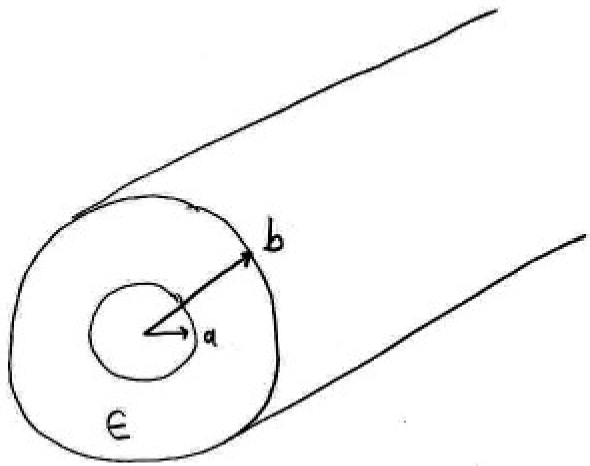
Source: Wikipedia
https://en.wikipedia.org/wiki/Coaxial_cable

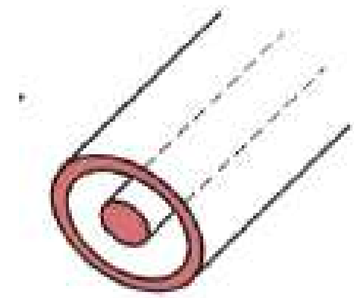
Transmission Line Properties



- $c =$ capacitance per unit length, F/m
- $\ell =$ inductance per unit length, H/m
- $r =$ series resistance per unit length, ohm/m, due to power dissiation in the copper conductors
- $g =$ shunt conductance per unit length, Siemens /m, due to power dissipation in the dielectric "insulator".

Coaxial Cable





- The inner conductor is a cylindrical metal wire of radius a
- The outer conductor is a hollow metal cylinder of inner radius b
- The outer conductor is usually made of braided wire so that the cable will be flexible
- The conductors are separated by an insulator or "dielectric" of permittivity ε
- Dielectrics are usually characterized by the "relative" permittivity, defined as $\varepsilon_r = \dfrac{\varepsilon}{\varepsilon_0}$, where $\varepsilon_0 = 8.854x10^{-12}$ F/m is the permittivity of empty space.
- A typical dielectric material is polyethylene, which has $\varepsilon_r = 2.26$

Transmission line properties:

The capacitance-per-unit-length is

$$c = \frac{2\pi\varepsilon}{\ln(b/a)} \ \text{F/m}$$

The inductance per unit length is

$$\ell = \frac{\mu}{2\pi}\ln(b/a) \ \text{H/m}$$

Hence, the speed-of-propagation is

$$u = \frac{1}{\sqrt{\ell c}} = \frac{1}{\sqrt{\mu\varepsilon}} = \frac{c}{\sqrt{\varepsilon_r}}$$

and the characteristic resistance is

$$R_c = \sqrt{\frac{\ell}{c}} = \frac{\ln(b/a)}{2\pi}\sqrt{\frac{\mu}{\varepsilon}}$$

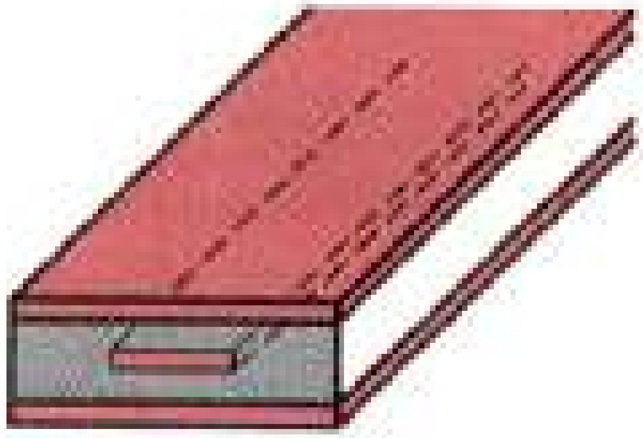
where

μ =permeability of the dielectric material

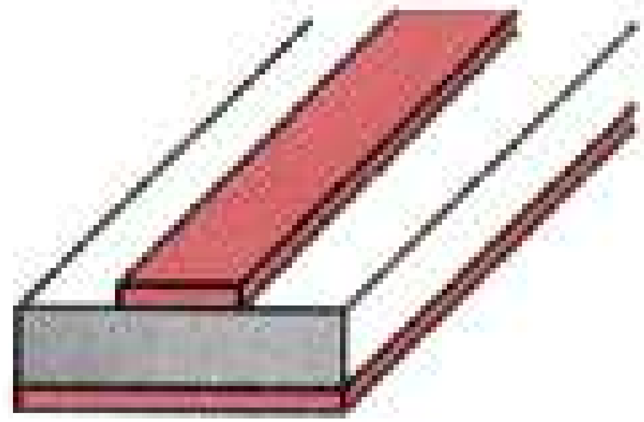
ε =permittivity of the dielectric material

Stripline and Microstrip

Inan, Inan and Said
Figure 2.1



Stripline



Microstrip

Stripline

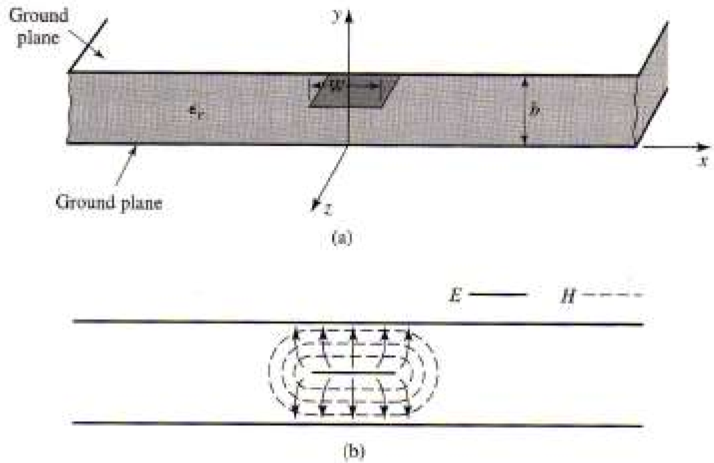
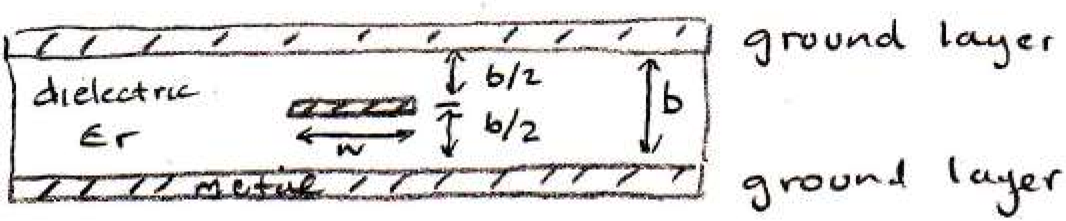


FIGURE 3.22 Stripline transmission line. (a) Geometry. (b) Electric and magnetic field lines.

From Pozar, "Microwave Engineering", Wiley, Fig. 3.22.



The speed of propagation is

$$u = \frac{c}{\sqrt{\varepsilon_r}}$$

The characteristic resistance is

$$R_c \approx \frac{30\pi}{\sqrt{\varepsilon_r}} \frac{b}{W_e + 0.441b}$$

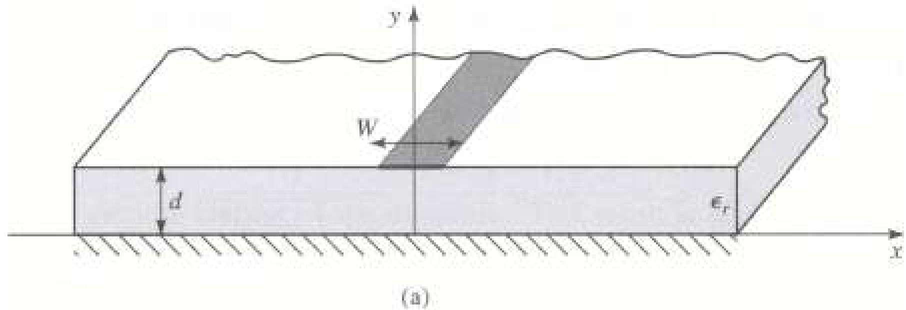
where

$$W_e = \begin{cases} W & for \dfrac{W}{b} > 0.35 \\ b\left(0.35 - \dfrac{W}{b}\right)^2 & for \dfrac{W}{b} < 0.35 \end{cases}$$

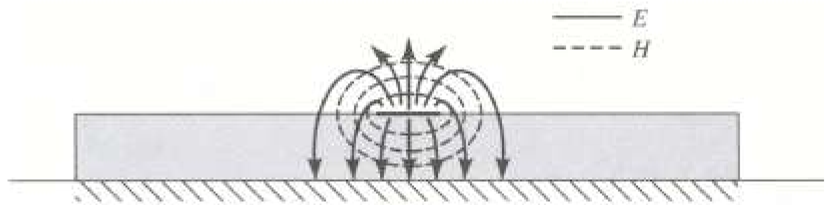
and W is the width of the circuit interconnect path

Pozar in "Microwave Engineering" (Wiley, 2004)

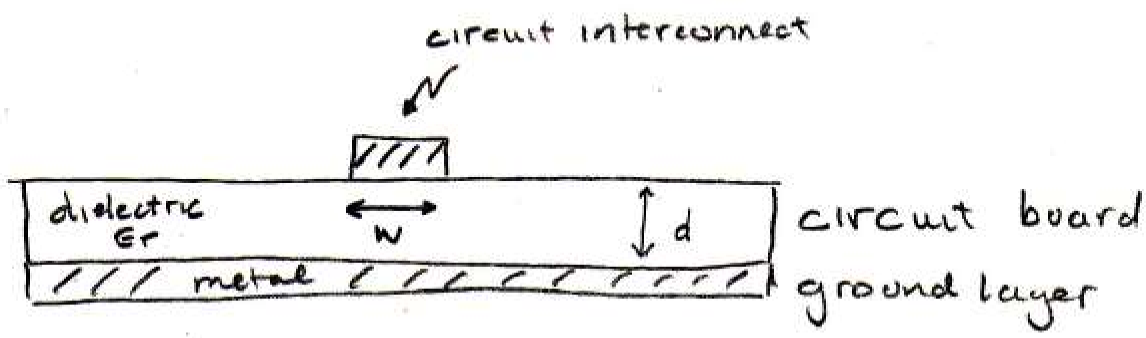
Microstrip



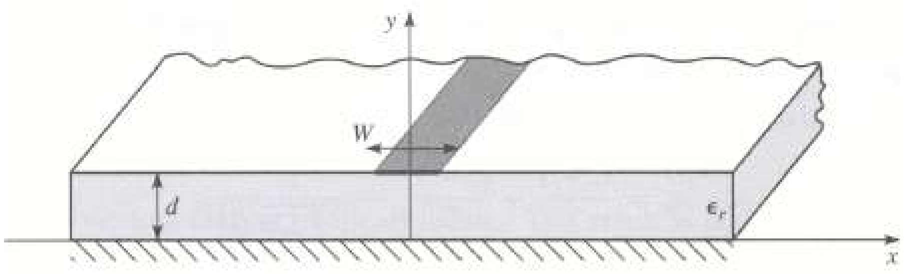
Pozar Fig. 3.25



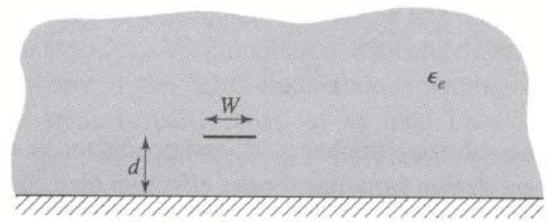
D.M. Pozar, "Microwave Engineering", 2nd edition, Wiley, 1998.



Formulas for Microstrip



Pozar Fig. 3.25



Pozar Fig. 3.26

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\frac{1}{\sqrt{1 + \frac{12d}{W}}}$$

$$u = \frac{c}{\sqrt{\varepsilon_e}}$$

$$R_c = \frac{60}{\sqrt{\varepsilon_e}}\ln\left(\frac{8d}{W} + \frac{W}{4d}\right) \qquad \text{for } \frac{W}{d} \le 1$$

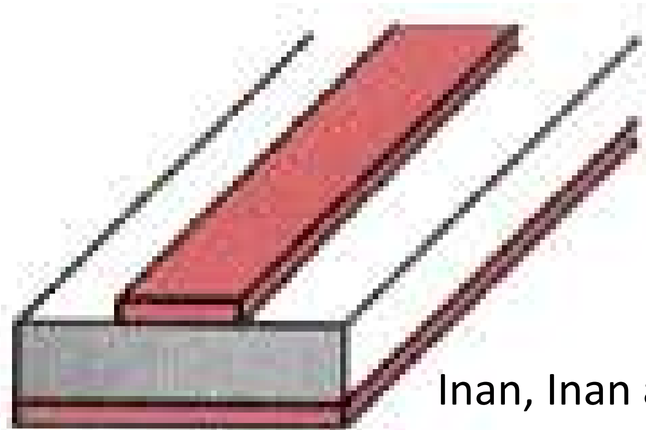
$$R_c = \frac{120\pi}{\sqrt{\varepsilon_e}\left[\frac{W}{d} + 1.393 + 0.667\ln\left(\frac{W}{d} + 1.444\right)\right]} \qquad \text{for } \frac{W}{d} \ge 1$$

Microstrip Transmission Line

50 ohm SMA connector

R_c =50 ohm microstrip line

R_L =50-ohm "chip" resistor as the load.



Inan, Inan and Said Figure 2.1

Later in the course we will look at some measurements made with this microstrip line.