

Release 14.7 - xst P.20131013 (nt64)
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--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 1.40 secs

--> Parameter xsthdmdir set to xst

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 1.41 secs

--> Reading design: even_detector.prj

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* Synthesis Options Summary *

---- Source Parameters

Input File Name	: "even_detector.prj"
Input Format	: mixed
Ignore Synthesis Constraint File	: NO

---- Target Parameters

Output File Name	: "even_detector"
Output Format	: NGC
Target Device	: xc3s1200e-4-fg320

---- Source Options

Top Module Name	: even_detector
Automatic FSM Extraction	: YES
FSM Encoding Algorithm	: Auto
Safe Implementation	: No
FSM Style	: LUT
RAM Extraction	: Yes
RAM Style	: Auto
ROM Extraction	: Yes
Mux Style	: Auto
Decoder Extraction	: YES
Priority Encoder Extraction	: Yes
Shift Register Extraction	: YES
Logical Shifter Extraction	: YES
XOR Collapsing	: YES

ROM Style : Auto
Mux Extraction : Yes
Resource Sharing : YES
Asynchronous To Synchronous : NO
Multiplier Style : Auto
Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES
Global Maximum Fanout : 500
Add Generic Clock Buffer (BUFG) : 24
Register Duplication : YES
Slice Packing : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Yes
Use Synchronous Set : Yes
Use Synchronous Reset : Yes
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
Verilog 2001 : YES
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

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* HDL Compilation *

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Compiling vhdl file "C:/Users/gabri/Documents/Xilinx/even_detector/list_0204_xor.vhd" in Library work.

Entity <my_xor2> compiled.

Entity <my_xor2> (Architecture <beh_arch>) compiled.

Entity <not1> compiled.

Entity <not1> (Architecture <beh_arch>) compiled.

Compiling vhdl file "C:/Users/gabri/Documents/Xilinx/even_detector/list_02_even_all.vhd" in Library work.

Entity <even_detector> compiled.

Entity <even_detector> (Architecture <str_arch>) compiled.

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* Design Hierarchy Analysis *

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Analyzing hierarchy for entity <even_detector> in library <work> (architecture <str_arch>).

Analyzing hierarchy for entity <my_xor2> in library <work> (architecture <beh_arch>).

Analyzing hierarchy for entity <not1> in library <work> (architecture <beh_arch>).

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*	HDL Analysis	*
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Analyzing Entity <even_detector> in library <work> (Architecture <str_arch>).
Entity <even_detector> analyzed. Unit <even_detector> generated.

Analyzing Entity <my_xor2> in library <work> (Architecture <beh_arch>).
Entity <my_xor2> analyzed. Unit <my_xor2> generated.

Analyzing Entity <not1> in library <work> (Architecture <beh_arch>).
Entity <not1> analyzed. Unit <not1> generated.

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*	HDL Synthesis	*
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Performing bidirectional port resolution...

Synthesizing Unit <my_xor2>.
 Related source file is
 "C:/Users/gabri/Documents/Xilinx/even_detector/list_0204_xor.vhd".
 Found 1-bit xor2 for signal <o1>.
Unit <my_xor2> synthesized.

Synthesizing Unit <not1>.
 Related source file is
 "C:/Users/gabri/Documents/Xilinx/even_detector/list_0204_xor.vhd".
Unit <not1> synthesized.

Synthesizing Unit <even_detector>.
 Related source file is
 "C:/Users/gabri/Documents/Xilinx/even_detector/list_02_even_all.vhd".
Unit <even_detector> synthesized.

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HDL Synthesis Report

Macro Statistics

# Xors	: 2
1-bit xor2	: 2

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*	Advanced HDL Synthesis	*
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Advanced HDL Synthesis Report

Macro Statistics

```
# Xors : 2
1-bit xor2 : 2
```

```
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*                               Low Level Synthesis                               *
```

Optimizing unit <even_detector> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block even_detector, actual ratio is 0.

Final Macro Processing ...

```
=====
Final Register Report
```

Found no macro

```
=====
*                               Partition Report                               *
```

```
Partition Implementation Status
-----
```

No Partitions were found in this design.

```
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*                               Final Report                               *
```

```
Final Results
```

```
RTL Top Level Output File Name      : even_detector.ngr
Top Level Output File Name          : even_detector
Output Format                        : NGC
Optimization Goal                    : Speed
Keep Hierarchy                      : No
```

```
Design Statistics
```

```
# IOs : 4
```

```
Cell Usage :
```

```
# BELS : 1
# LUT3 : 1
# IO Buffers : 4
# IBUF : 3
# OBUF : 1
```

```
Device utilization summary:
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```

Selected Device : 3s1200efg320-4

Number of Slices: 1 out of 8672 0%

Number of 4 input LUTs: 1 out of 17344 0%
Number of IOs: 4
Number of bonded IOBs: 4 out of 250 1%

Partition Resource Summary:

No Partitions were found in this design.

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TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -4

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 6.209ns

Timing Detail:

All values displayed in nanoseconds (ns)

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Timing constraint: Default path analysis
Total number of paths / destination ports: 3 / 1

Delay: 6.209ns (Levels of Logic = 3)
Source: a<0> (PAD)
Destination: even (PAD)

Data Path: a<0> to even

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	1	1.218	0.595	a_0_IBUF (a_0_IBUF)
LUT3:I0->O	1	0.704	0.420	unit3/o11 (even_OBUF)
OBUF:I->O		3.272		even_OBUF (even)
Total		6.209ns (5.194ns logic, 1.015ns route) (83.7% logic, 16.3% route)		

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Total REAL time to Xst completion: 19.00 secs
Total CPU time to Xst completion: 19.03 secs

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Total memory usage is 4506224 kilobytes

Number of errors	:	0	(0	filtered)
Number of warnings	:	0	(0	filtered)
Number of infos	:	0	(0	filtered)