2000 6TH IEEE International Workshop on Cellular Neural Networks and Their Applications Proceedings

A Compact and Universal Cellular Neural Network Cell Based on Resonant Tunneling Diodes: Circuit, Model, and Functional Capabilities

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ABSTRACT: *A novel Cellular Neural Network (CNN) cell and its circuit realization are proposed. The theory of the multi-nested universal cell [1] is applied, and the non-monotonic current-voltage characteristic of resonant tunneling diodes (RTD) is exploited to achieve a high functionality. The proposed cell has the potential of implementing arbitrary local Boolean functions with n inputs. The cell has a complexity of only O(n) in the number of devices and template elements. For comparison, the digital n-to-1 multiplexor, a functionally equivalent system has a complexity of $O(2^n)$. A simple, piecewise-linear mathematical model is derived and used to evaluate the functional capabilities of the RTD-CNN cell. The model was proved to be accurate enough, and, as shown in [2], only minor tuning of some of the parameters is necessary to achieve the same functionality using a Spice simulation of the same circuit, which is based on more refined physical device models.*

1. Introduction

The demand for high speed in signal processing parallels the increasing requirements for more memory and computing power embedded in a single chip. In the near future, a plateau is expected to be reached in Moore's law, which has accurately predicted the constant increase in density of components per chip over the last 3 decades. To overcome this problem, several new devices and technologies (often referred to as nano-technologies) were proposed in the last decade to reduce the size of the active components and achieve greater functionality. While some of them are, at present, described theoretically (e.g. the "quantum dots"), and others require special operating conditions, we focused on a relatively mature technology; namely the vertical integration of resonant tunneling diodes (RTD) with FETs in high speed III-V semiconductors [3]. This technology provides an increase in functionality while operating at room temperature. Our goal is to exploit the particularities of this technology to build a new generation of cellular neural networks (CNN) [4] with increased functional capability, a switching speed in the order of picoseconds, and a larger number of cells on a single CNN chip. Such intelligent chips with increased computational power and processing speed are essential to many high-tech applications, including microrobotics and integrated vision.

The CNN cell described in this paper exploits the non-monotone current-voltage (I-V) characteristic of the resonant tunneling diode (RTD) [5] to build a compact programmable system capable of representing any Boolean function with n inputs. Up-to-date RTD-based technologies were developed and tested for applications such as RTD-based logic gates [6,7] and memory cells [8]. However, the most advanced RTD-based logic gates families reported in the literature are *neither* programmable *nor* universal. They are usually circuits designed to implement a set of basic two-inputs gates (e.g. AND, NOT, OR, XOR) which are the building blocks of more sophisticated digital systems. Our solution is radically different and leads to a tremendous increase in functionality. Indeed, while most of the RTD-based systems reported in the literature exploit only the switching properties resulting from the region with negative differential resistance in the RTD characteristic, we exploit the *entire non-monotonic* I-V characteristic $I = f_{RTD}(V)$ applying the results of a theory on "multi-nested" universal CNN cells [1]. The *analog and recurent nonlinear* nature of computation in the proposed cell leads to a dramatic decrease in complexity, and, at the same time, an increase in functionality. Compared to the *standard CNN cell* [4], our design has several advantages: (a) It uses a simple synapse made of only two n-FET transistors, where the synaptic weights (or CNN templates) are always positive; (b) It expands the domain of realizable Boolean functions beyond the small class of *linearly separable* Boolean functions, while it uses exactly the same number of parameters ($n+1$) to code the template; (c) It targets a promising nanotechnology, from which very high processing speeds and densities are expected.

The proposed RTD-CNN cell circuit and its piecewise-linear model are introduced in Section 2. After briefly reviewing the "nesting" theory in [1], we show how it can be implemented using RTD-based devices and what is

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the role of each sub-circuit composing the RTD-CNN cell. The functional capabilities of the RTD-CNN cell are discussed in Section 3. Conclusions and topics of further research are given in Section 4.

2. The generic RTD-CNN cell circuit

The schematic of the generic RTD-CNN cell circuit is presented in Fig. 1. The circuit, its model and design principles apply to any RTD-based technology. The numerical values considered herein apply for a particular RTD-FET technology [3], which has been implemented and tested and for which measurements of the devices were made available. Consequently, the RTD and FET device parameters used herein correspond to the same technology. Due to limitations of space we provide here only the basic concepts. More details about the design rules and modeling techniques can be found in [9].

A piecewise-linear model is used for the RTDs and the simple generic heterojunction FET model in [10,p.330] is used for the FET transistors. The parameters of both models were determined to achieve the best match with the measured characteristics given in [3]. The threshold voltages for all FET transistors are $V_T = 0$.

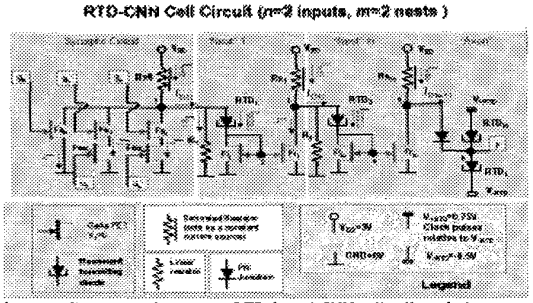

Figure 1: The schematic diagram of the generic RTD-based CNN cell. All symbols are standard except the "saturated resistor", which is defined as an active load acting as a current stabilizer or constant current source [12].

As shown in Fig.1, all signals used for inputs (u_i), output (y) and control (g_i), are *voltages.* However, internally, the circuit is divided into three functionally distinct sub-circuits, where currents are used as coupling signals.

Our goal is to define a circuit modeled by the nonlinear function F so that $Y = F(U_i, g_i, g_0)$ implements programmable Boolean functions of the inputs U_i. Here, a binary code was assigned to the input and output signals. The *binary variable* U_i is used to code the binary inputs, where $U_i = \begin{cases} 0, \text{if } u_i < V_T \\ 1, \text{if } u_i > V_T \end{cases}$, and $u_i, i = 1,...,n$, are the *effective input voltage* signals. The output binary variable Y is defined similarly with respect to the output y. The *n+1 control* or *gene inputs,* are labeled g_0 and $g_i, i = 1,...,n$, (corresponding to the bias z, and the B template parameters b_i, in the standard CNN cell). A set of parameters defining a particular Boolean realization is called a *gene* [4]. The design problem consists in finding the whole set of (robust) genes associated with the entire set of Boolean functions (identified by an integer ID number) admitting RTD-CNN cell realizations. The cell is said to be *universal* if a gene exists for all arbitrary Boolean functions.

In defining our RTD-CNN circuit, we apply the theory of universal CNN cells [1]. This theory shows that a cell is *universal* in the sense mentioned above if F is of the form:

$$Y = F(U_i, b_i, b_0) = \text{sgn}(w(\sigma)),\ \sigma = b_0 + \sum_{i=1}^{n} b_i U_i \qquad (1)$$

In the RTD-CNN circuit, the evaluation of σ is performed by the *synaptic sub-circuit,* and the evaluation of the sign function in the *output* or *"axon" sub-circuit.* The *discriminant function* $w(\sigma)$ is a one-dimensional, multiple-folded function which plays a fundamental role in achieving the *universality* [1]. This function is

implemented in our cell circuit by exploiting the non-monotone I-V characteristic of the RTDs when arranged in a cascade of similar *nesting sub-circuits.* If the discriminant function has only one root $w(\sigma)=0$ (e.g., in the linear case of a standard CNN cell), only a very small fraction of the Boolean functions (the linearly separable ones) admit realizations, therefore the standard CNN cell is *not universal.* In what follows we define the *folding degree* f_w of a *discriminant function* w as the maximum number of roots of the equation $w(\sigma)=z$, where z is any real number. It is conjectured that if $f_w \geq 2^{n-1}$, then there *exists* a set of parameters b_i (gene) for any of the 2^{2^n} Boolean functions so that (1) is a realization of that Boolean function. This conjecture was proved for $n \leq 4$ in [1] by enumerating all Boolean functions and their associate genes. For compact realizations it is essential to find an efficient way of implementing a function with a *folding degree* of 2^{n-1}, while minimizing the number of nonlinear devices. A solution to this problem was given in the framework of the "multi-nested" universal CNN cell theory in [1]. In the next sub-section we generalize this idea and apply it to the case of RTD devices, exploiting their non-monotone characteristic.

2.1 The "nesting" principle and its RTD realization

For a properly chosen set of parameters $z_0, z_1, .., z_m$, the discriminant function $w^m(x)$ defined by the iterative mapping

$$w^0(\sigma)=z_0+\sigma, \quad w^1(\sigma)=z_1+g(w^0(\sigma)), .., \; w^m(\sigma)=z_k+g(w^{m-1}(\sigma)) \qquad (2)$$

has a folding degree equal to p^m, where p is the folding degree of the *seed* function $g(\cdot)$ which is non-monotonic (e.g., a polynomial of *degree p,* or a canonical piecewise linear representation [11] with *p-1* absolute value terms). In [1] we called each iteration in (2) a "nesting". We do not give here the proof due to space limitations; however one may easily see it thinking of *g(x)* as polynomials of degree p.

The I-V characteristic of the RTD (Fig. 2) can be modeled by the following seed function with $p=3$ (where x plays the role of the voltage):

$$g_{RTD}(x)=\alpha x+\beta+\gamma\left(|x-V_p|-|x-V_v|\right), \qquad (3)$$

where α, β, γ and V_p, V_v are technology specific parameters.

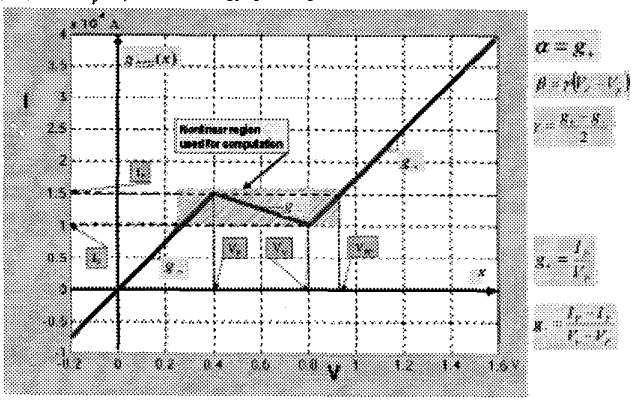

Figure 2: The current-voltage characteristic of the RTD (a canonical piecewise linear model)

Observe that the RTD alone cannot implement the "nesting principle". The reason is that in the case of the RTD, the output in (3) is a current, while the input variable x is a voltage. Therefore a "nesting" sub-circuit (Fig.1) is designed, having a similar input-output characteristic as in Fig 2, but now both the input and the output are current signals. Cascading m such circuits is functionally equivalent to implementing Eq. (2), where w^m is

substituted by $I_{IN\,m+1}$ in our circuit diagram. This will lead to the realization of a discriminant function with a folding degree of 3^m. In addition, the m parameters $I_{ref1},...,I_{refm}$ corresponding to $z_1,...,z_m$ in (2) should be optimized globally (for the whole chain of "nesting" units) so that the degree of folding reaches its maximum of 3^m and the roots of $I_{INm+1}(I_{IN1})$ are as uniformly distributed as possible.

2.2. Circuit description and model

The **synaptic circuit** (Fig.1) has the advantage of being very simple in the sense that it requires only positive synapses. This advantage comes from the use of a non-monotone discriminant and leads to a significant reduction in the number of components, compared with the standard CNN cells where the circuitry should be designed to accommodate both negative and positive synapses. The positive synaptic parameters b_i in the mathematical model $\sigma = z - b_0 - \sum_{i=1}^{n} b_i u_i$ correspond to the currents I_i flowing through the synaptic transistors Fs_i. The magnitude of these currents is controlled by the gate voltages g_i, which correspond to the cloning template (or gene) parameters. The synaptic currents are turned ON or OFF by the serially connected switch transistors Fsw_i, depending on the binary input signal applied to their control gates. The mathematical model of the synaptic circuit is given by

$$I_{IN1} = I_{ref0} - I_0 - \sum_{i=1}^{n} I_i U_i \tag{5}$$

The purpose of a **"nesting" unit** is to implement one step of the iteration (2), while both the input and the output are coded as currents. Therefore, a cascade of m nesting units will implement the entire iteration (2). In what follows we will discuss the first nesting unit in Fig.1. The other units are similar. The nonlinear discriminant $w^0(\sigma)$ in (2) corresponds to the input current I_{IN1} in our nesting sub-circuit, and the output current I_{INm+1} of the whole cascade of m nesting circuits corresponds to $w^m(\sigma)$ in (2).

The resistors $R_1, R_2, ..R_m$ play an important role, and they are subject to a design trade-off. A larger value of the resistance leads to lower power consumption but it increases the risk of unstable behavior due to the negative differential resistance of the RTD. If the value is too small, all other components should drive larger currents and therefore the *compactness* of the cell depreciates. The functional role of these resistors is to convert the input current flowing within a nesting unit into a voltage, so that the nonlinear voltage-current characteristic of the RTDs can be efficiently exploited. The current through the RTD is then sensed and mirrored (with a certain amplification factor k) using the current mirror formed by the two FET transistors in each "nesting" unit. The input-output current characteristic of each "nesting" unit is similar to the voltage-current characteristic of the RTD but now, since both the input and the output signals are of the same type, the nesting operation can be effectively implemented.

The simplified piecewise-linear model of a nesting unit was derived in [9] and is given by

$$g'_{RTD}(x) = \alpha' x + \beta' + \gamma'\left(|x - V'_p| - |x - V'_v|\right) \tag{6}$$

$$I_{IN2}(I_{IN1}) = I_{ref1} - k \cdot \mathrm{rect}\left(g'_{RTD}(R_1 I_{IN1})\right), \tag{7}$$

where k is the current mirror gain (in our example $k=10$) and the function $\mathrm{rect}(x) = (x + |x|)/2$ models the rectification property of the current mirror (i.e., only positive currents I_{RTD1} entering the current mirror are reflected and amplified). The function $g'_{RTD}(x)$ describes the current I_{RTD1} through the RTD when x is the voltage on the input node of the "nesting" sub-circuit and of an equivalent RTD. Its expression is similar to (3) and its parameters can be readily determined [9] knowing the value of the linear resistor R_1 and the specific parameters of the RTD model in (2). Equations similar to (6) and (7) should be considered for any additional nesting circuit.

The output or "axon" circuit is implementing the sign function, being inspired by the MOBILE circuit reported elsewhere [13]. The output sub-circuit acts like a neural axon: when the input current exceeds a certain threshold value I_{TH}, the output will switch to an "ON" state otherwise, it remains "OFF". It is assumed that before each new operating cycle the output state is reset to the "OFF" state, by turning the power supply off

($V_{+RTD} = V_{-RTD}$; The power supply is acting as a clock signal to avoid hysteresis). The model derived in [9] is described by:

$$Y = 0.5 + 0.5\,\mathrm{sgn}\left(I_{INm+1} - I_{TH}\right) \tag{8}$$

The value of the threshold current is influenced by the specific parameters of the RTDs and by the voltage difference $V_{+RTD} - V_{-RTD}$. For our example, $I_{TH} = 0.044mA$. Two independent power supplies are used for the output circuit to ensure an output voltage y which can be interpreted as a binary code by the inputs of neighboring RTD-CNN cell. By using high quality FET transistors it was shown in [2] that the "axon" unit can be simplified, by eliminating the two RTDs and the clocked voltage supply.

3. Functional capabilities of the RTD-CNN cell

The piecewise-linear model of the *generic RTD-CNN cell* circuit represented by the equations (5)-(8) was found to be accurate enough to capture the essential characteristic of our RTD-CNN cell; namely, its capability to provide a discriminant function with 3^m folds while using only $O(m)$ devices. As the theory of the universal CNN cell predicts, the use of such a discriminant function greatly enhances the number of realizable Boolean functions. Spice simulations described in [2] show that the same characteristic is obtained when our simplified model is replaced by a more accurate physical model of the devices. However, the piecewise-linear model has the advantage of shortening the computation time needed to evaluate the functional capabilities of the RTD-CNN cell. By functional capabilities here we mean the number of realizable Boolean functions for a cell with a given number of inputs and nests. The *function selection* problem is defined as an analytical or algorithmic procedure to find all Boolean function realizations, and give for each one at least one (if possible the most robust) associated parameter point $\left(I_i \mid_{i=0,n}\right)$, or gene. The algorithm is applied only once for a given cell model and the result is stored in a list (or a table) which then allows to *select* a specified Boolean function realization using the predetermined gene. The geometrical complexity of the partitioning induced by the piecewise-linear model in the parameter space impedes analytical approaches. Another possibility is to treat it as a nonlinear optimization problem and solve it with specific methods, e.g. using evolutionary algorithms or algorithms from the Simulated Annealing family. The solution for this hard optimization problem is effective only when one wants to determine the realization for a specific Boolean function, but it leads to very large computation times when used to estimate the number of different potential Boolean functions realized by the cell. Surprisingly, it turns out that for small values of *n*, the fastest method to evaluate the functional capabilities is the *random exploration* of the parameter space. Each step of this process consists of randomly generating a set of parameters $\left(I_i \mid_{i=0,n}\right), 0 < I_i < \frac{I_{ref\,0}}{n+1}$, and evaluating the piecewise-linear cell model to determine the Boolean function ID which corresponds to our randomly generated parameter point. Each time a new function is discovered, a list is updated with the new function ID, its actual realization, and its robustness. The algorithm evaluates the degree of robustness *rbs* for the realization associated with a given parameter point and updates the list with the most robust realization found for each function. For the case *n=3* inputs and *m=3* nests the algorithm required only two minutes to run, a list of all 256 Boolean functions and their realizations being generated and made available at ftp://bayview.eecs.berkeley.edu/pub/rd/all_2bool3.mat. Observe that *all* 256 Boolean functions with 3 inputs have RTD-CNN realizations having only *positive* synaptic parameters $I_i \mid_{i=0,n}$, and therefore a very simple and compact synaptic circuit. For the case *n=4* and *m=2* nests, the theory predicts that all 65536 Boolean functions should have an RTD-CNN cell realization. In practice, the random search algorithm was found to follow a logarithmic rule in the rate of newly discovered Boolean functions as a function of time and, therefore, it is not efficient to find the entire set of genes. At this moment we have a list of 50664 realizations made available at ftp://bayview.eecs.berkeley.edu/pub/rd/all_2bool4.mat. The realizations are not equally robust, which is a shortcoming that should be considered in further designs. However, it is impressive that almost 77% of the Boolean functions with 4 inputs have been found to have a realization when using a circuit with a very simple synaptic unit and only 2 additional "nesting" units. For comparison, a standard uncoupled CNN cell with 4 inputs (and 12 CMOS transistors per synapse [4]) can implement only about 2% of the whole set of Boolean functions; namely, the linearly separable Boolean ones.

4. Conclusions and perspectives

A highly compact and versatile RTD-CNN cell is proposed based on the theory of multi-nested universal CNN cells [1], and the full description of its circuit realization is given. Our circuit supports recently reported nano-technologies allowing operation at room temperature, such as monolithic and vertical integration of RTDs with FET transistors using III-V semiconductors [3]. A simple piecewise-linear model for our cell is provided and the functional capabilities of the RTD-CNN cell were evaluated. The results are consistent with the theory in [1], the proposed cell exhibiting a higher functionality than obtained in standard CNN cells. Further simulations in Spice using realistic device models [2] confirm that the simple piecewise linear model is accurate enough to capture the main features and for a first design of the circuit parameters. The functional capabilities of our cell are far beyond those of the standard CNN cell while having a reduced number of devices and the same number of gene parameters. The vertical integration of RTDs offers the advantage of a significant increase in the density of cells per chip, since the RTD devices do not occupy additional area. Several issues have to be addressed in the future: (i) The development of an efficient optimization method to provide a realization in short time; (ii) Additional optimization of the RTD-CNN circuit for speed, power, and area; (iii) The investigation of potential advantages of adding recurrent synapses to our CNN cell.

Acknowledgments: This work was supported in part by the ONR grant N00014-99-1-0339 and by the MURI ONR grant N00014-98-1-0594. We would also like to thank Dr. D. M. Chow and Dr. J. N. Schulman for helpful discussions during the initial phase of the work.

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