

Universidade de Brasília
Organização e Arquitetura de Computadores
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Projeto de uma ULA em VHDL

– código ULA

Entidade: ulaMIPS

Arquiteturas: ulaMIPS_if_then_else – implementação da ULA utilizando if-then-else em processo.

ulaMIPS_concorrente – implementação da ULA com with-select (concorrente).

ulaMIPS_case – implementação da ULA usando case em processo.

Configurações: conf_ulaMIPS_if_then_else

conf_ulaMIPS_concorrente

conf_ulaMIPS_case

– código de teste

Entidade: ulaMIPS_tb

Arquitetura: ulaMIPS_tb_arch

Labels: U1 – instancia teste para a configuração conf_ulaMIPS_if_then_else.

U2 – instancia teste para a configuração conf_ulaMIPS_concorrente .

U3 – instancia teste para a configuração conf_ulaMIPS_case.

1. Dados da Análise e Síntese

Flow Summary	
Flow Status	Successful - Mon Nov 16 15:34:02 2015
Quartus II 64-Bit Version	13.0.0 Build 156 04/24/2013 SJ Web Edition
Revision Name	ula
Top-level Entity Name	ulaMIPS
Family	Cyclone II
Device	EP2C70F896C6
Timing Models	Final
Total logic elements	389
Total combinational functions	389
Dedicated logic registers	0
Total registers	0
Total pins	101
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0

Fig1. Resultado da análise e síntese.

2. Dados da simulação no ModelSim

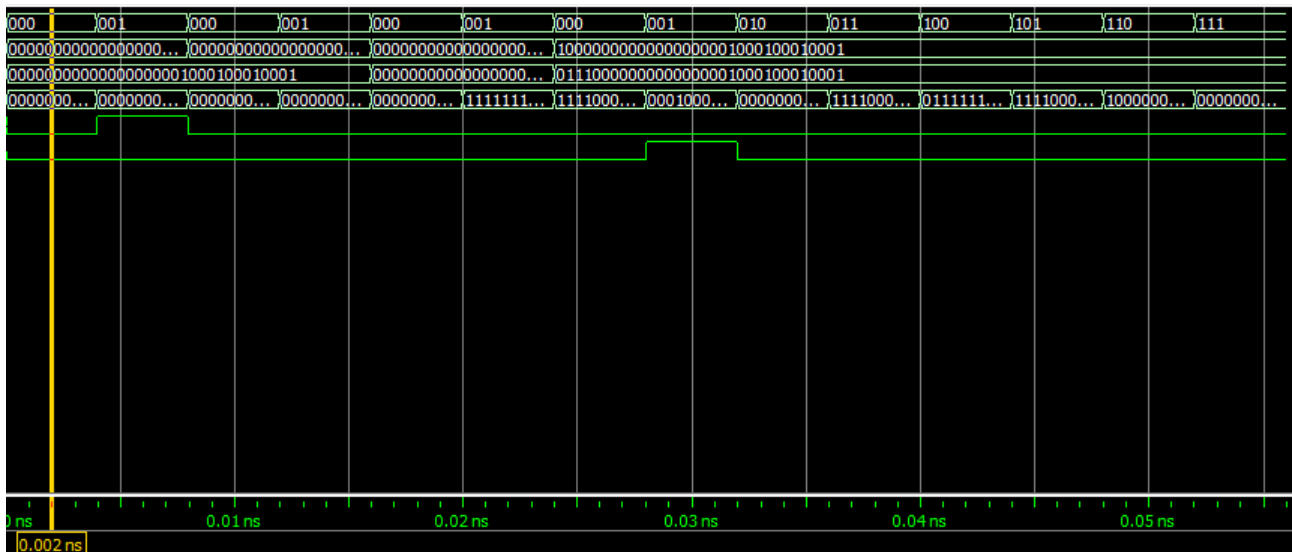


Fig2. Formas de onda da simulação no ModelSim.

+ /ulamips_tb/op	000
+ /ulamips_tb/inA	0000000000000000000000001000100010001
+ /ulamips_tb/inB	0000000000000000000000001000100010001
+ /ulamips_tb/outZ	00000000000000000000000010001000100010
/ulamips_tb/outZero	0
/ulamips_tb/outOvfl	0

Fig3. Opcode 000 – soma $A = B$

+ /ulamips_tb/op	001
+ /ulamips_tb/inA	0000000000000000000000001000100010001
+ /ulamips_tb/inB	0000000000000000000000001000100010001
+ /ulamips_tb/outZ	000
/ulamips_tb/outZero	1
/ulamips_tb/outOvfl	0

Fig4. Opcode 001 – subtração $A = B$

+ /ulamips_tb/op	000
+ /ulamips_tb/inA	00000000000000000000000010001000100010
+ /ulamips_tb/inB	0000000000000000000000001000100010001
+ /ulamips_tb/outZ	00000000000000000000000011001100110011
/ulamips_tb/outZero	0
/ulamips_tb/outOvfl	0

Fig5. Opcode 000 – soma $A > B$

+ /ulamips_tb/op	001
+ /ulamips_tb/inA	00000000000000000000000010001000100010
+ /ulamips_tb/inB	0000000000000000000000001000100010001
+ /ulamips_tb/outZ	0000000000000000000000001000100010001
/ulamips_tb/outZero	0
/ulamips_tb/outOvfl	0

Fig6. Opcode 001 – subtração $A > B$

+ /ulamips_tb/op	000
+ /ulamips_tb/inA	0000000000000000000000001000100010001
+ /ulamips_tb/inB	00000000000000000000000010001000100010
+ /ulamips_tb/outZ	00000000000000000000000011001100110011
/ulamips_tb/outZero	0
/ulamips_tb/outOvfl	0
0.018 ns	

Fig7. Opcode 000 – soma $A < B$

+ /ulamips_tb/op	001
+ /ulamips_tb/inA	0000000000000000000000001000100010001
+ /ulamips_tb/inB	00000000000000000000000010001000100010
+ /ulamips_tb/outZ	1111111111111111111111101110111011101111
/ulamips_tb/outZero	0
/ulamips_tb/outOvfl	0
0.022 ns	

Fig8. Opcode 001 – subtração $A < B$

+ /ulamips_tb/op	000
+ /ulamips_tb/inA	1000000000000000000000001000100010001
+ /ulamips_tb/inB	0111000000000000000000001000100010001
+ /ulamips_tb/outZ	11110000000000000000000010001000100010
/ulamips_tb/outZero	0
/ulamips_tb/outOvfl	0
0.026 ns	

Fig9. Opcode 000 – soma neg + pos = neg

+ /ulamips_tb/op	001
+ /ulamips_tb/inA	1000000000000000000000001000100010001
+ /ulamips_tb/inB	0111000000000000000000001000100010001
+ /ulamips_tb/outZ	0001000000000000000000000000000000000
/ulamips_tb/outZero	0
/ulamips_tb/outOvfl	1
0.03 ns	

Fig10. Opcode 001 – subtração neg – pos = pos

+ /ulamips_tb/op	010
+ /ulamips_tb/inA	1000000000000000000000001000100010001
+ /ulamips_tb/inB	0111000000000000000000001000100010001
+ /ulamips_tb/outZ	0000000000000000000000001000100010001
/ulamips_tb/outZero	0
/ulamips_tb/outOvfl	0
0.034 ns	

Fig11. Opcode 010 – and

+ /ulamips_tb/op	011
+ /ulamips_tb/inA	1000000000000000000000001000100010001
+ /ulamips_tb/inB	0111000000000000000000001000100010001
+ /ulamips_tb/outZ	1111000000000000000000001000100010001
/ulamips_tb/outZero	0
/ulamips_tb/outOvfl	0
0.038 ns	

Fig12. Opcode 011 – or

+ /ulamips_tb/op	100
+ /ulamips_tb/inA	1000000000000000000 1000 1000 1000 1
+ /ulamips_tb/inB	01110000000000000000 1000 1000 1000 1
+ /ulamips_tb/outZ	01111111111111111110 1110 1110 1110 1110
/ulamips_tb/outZero	0
/ulamips_tb/outOvfl	0

0.042 ns

Fig13. Opcode 100 – not

[illegible]

Fig14. Opcode 101 – xor

+ /ulamips_tb/op	110
+ /ulamips_tb/inA	10000000000000000000 1000 1000 1000 1
+ /ulamips_tb/inB	01110000000000000000 1000 1000 1000 1
+ /ulamips_tb/outZ	10000000000000000000 1000 1000 1000 1
/ulamips_tb/outZero	0
/ulamips_tb/outOvfl	0

0.05 ns

Fig15. Opcode 110 – bypass

[illegible]

Fig16. Opcode 111 – slt

Todas as arquiteturas apresentaram as mesmas formas de onda.