Digital I/O

Entradas e saídas

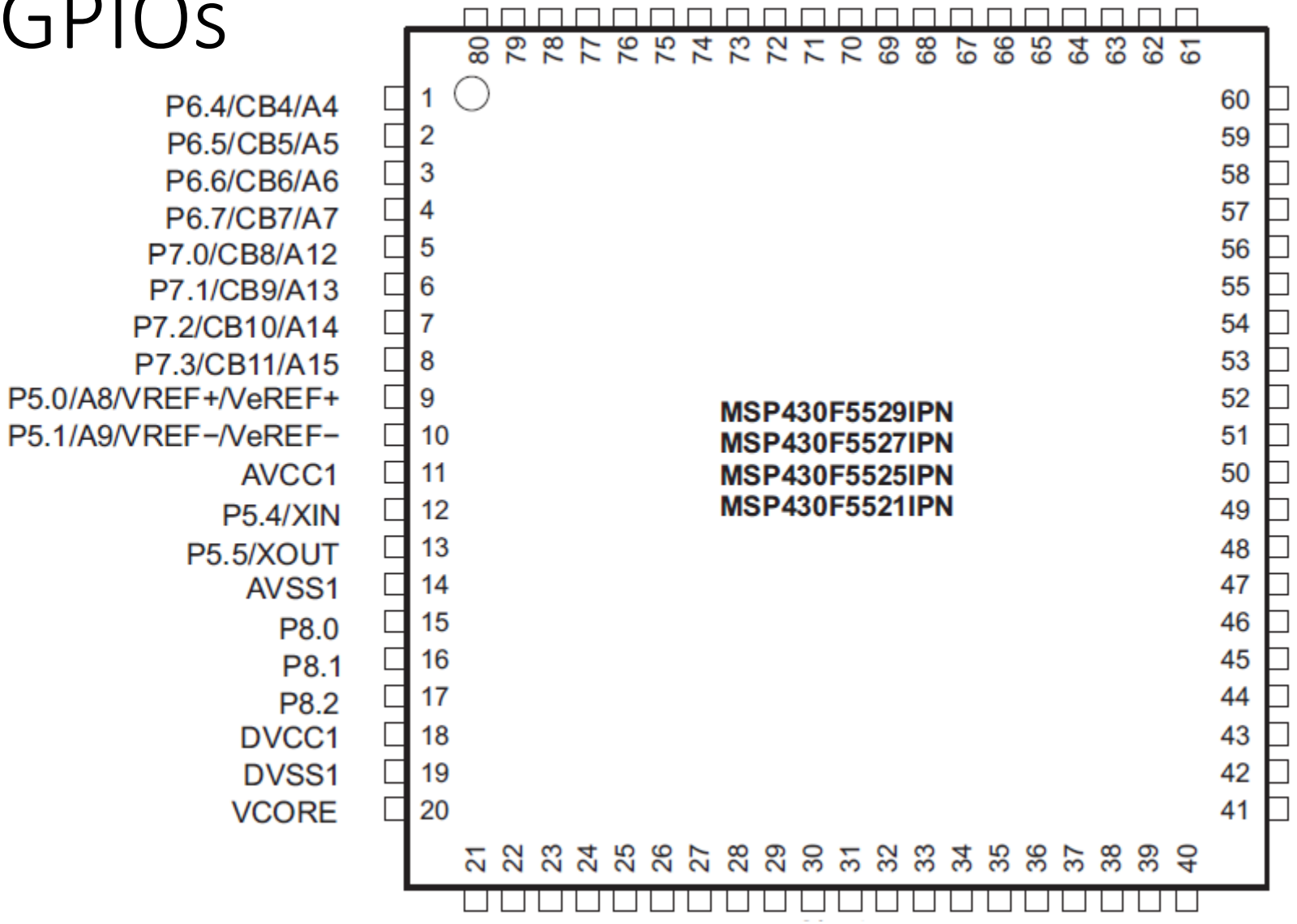
Agenda

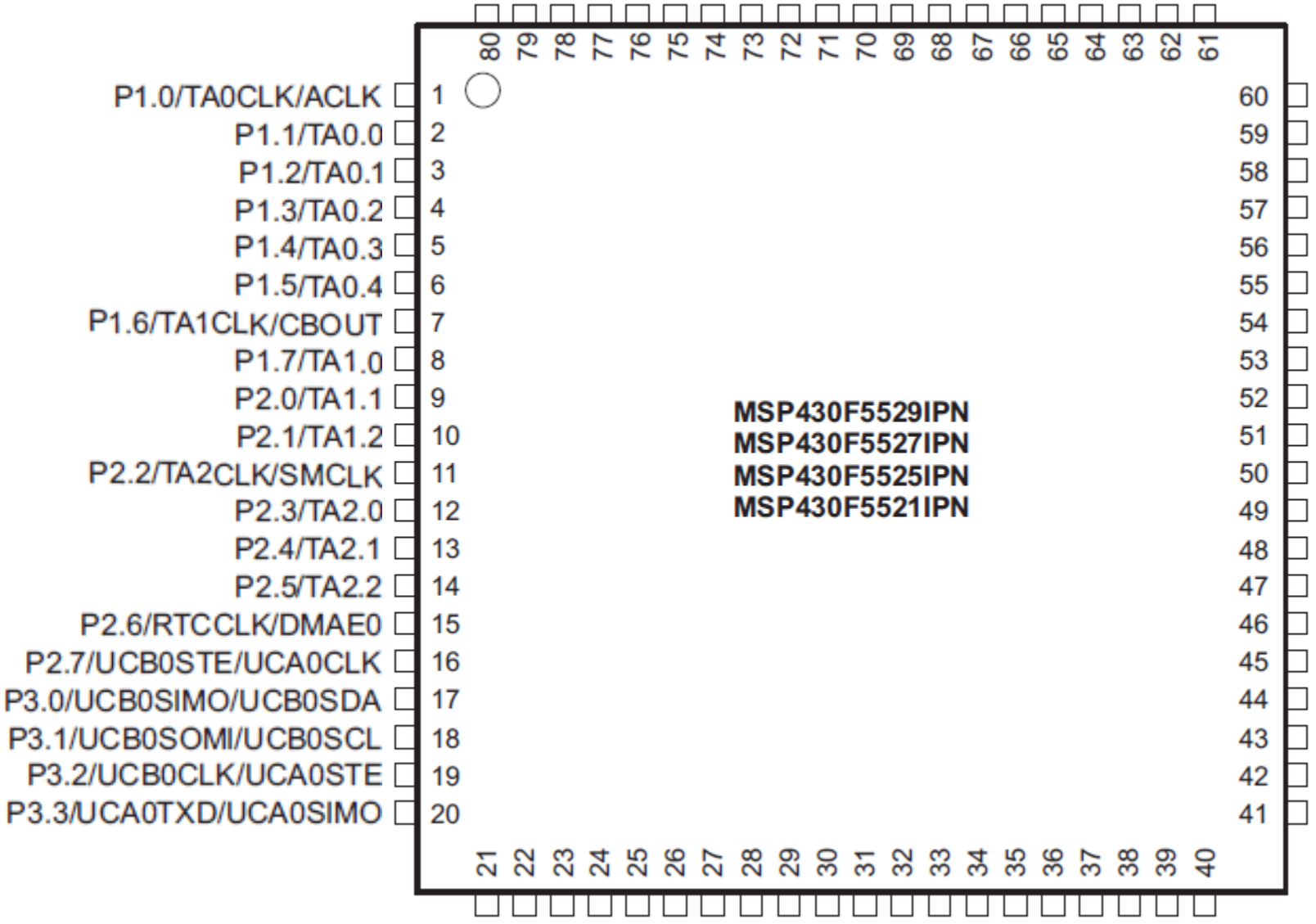
- GPIOs
- Configuração
- Vetores de interrupção
- Dicas de operação
- Aspectos “analógicos” de pinos digitais

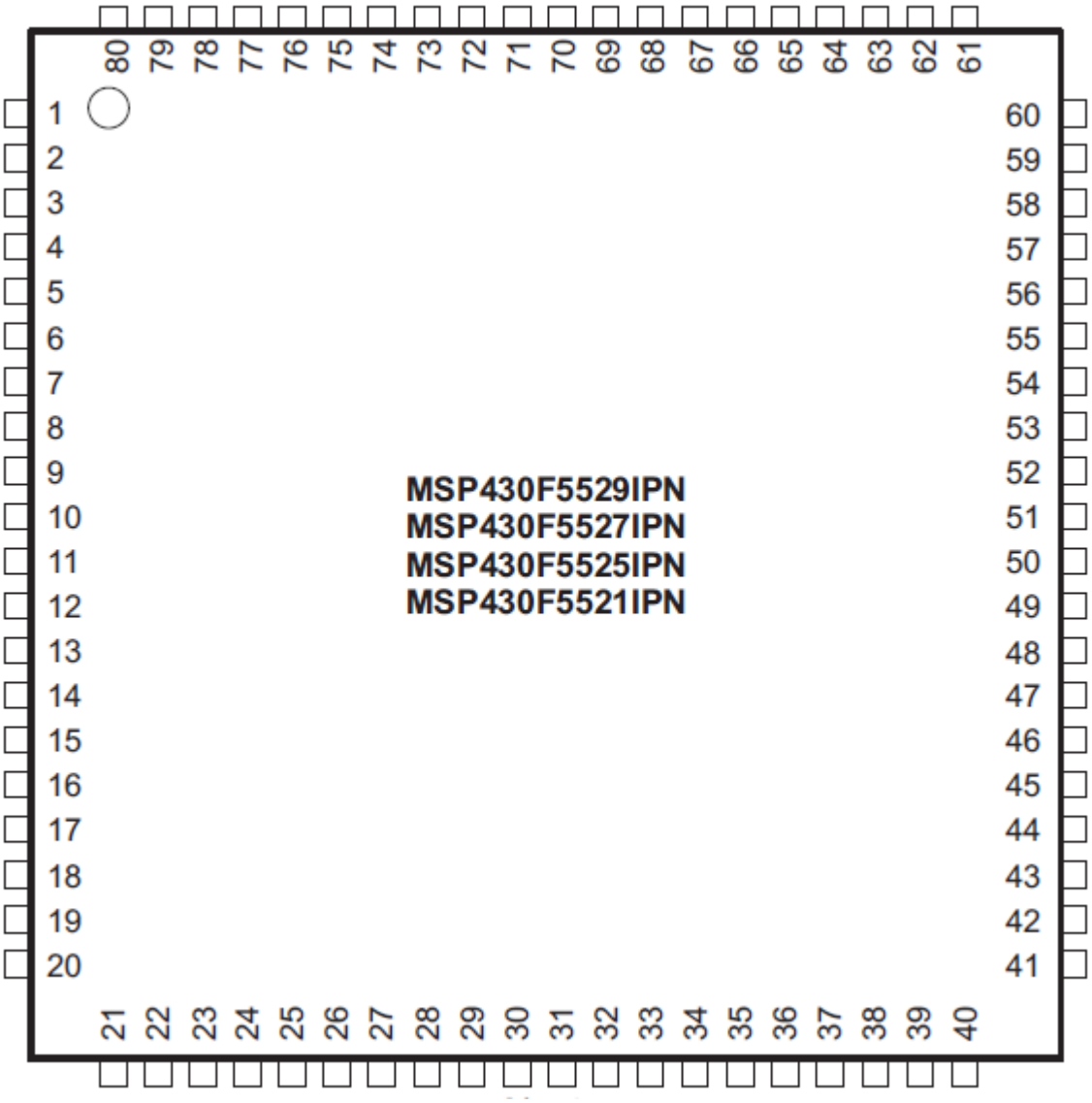
GPIOs

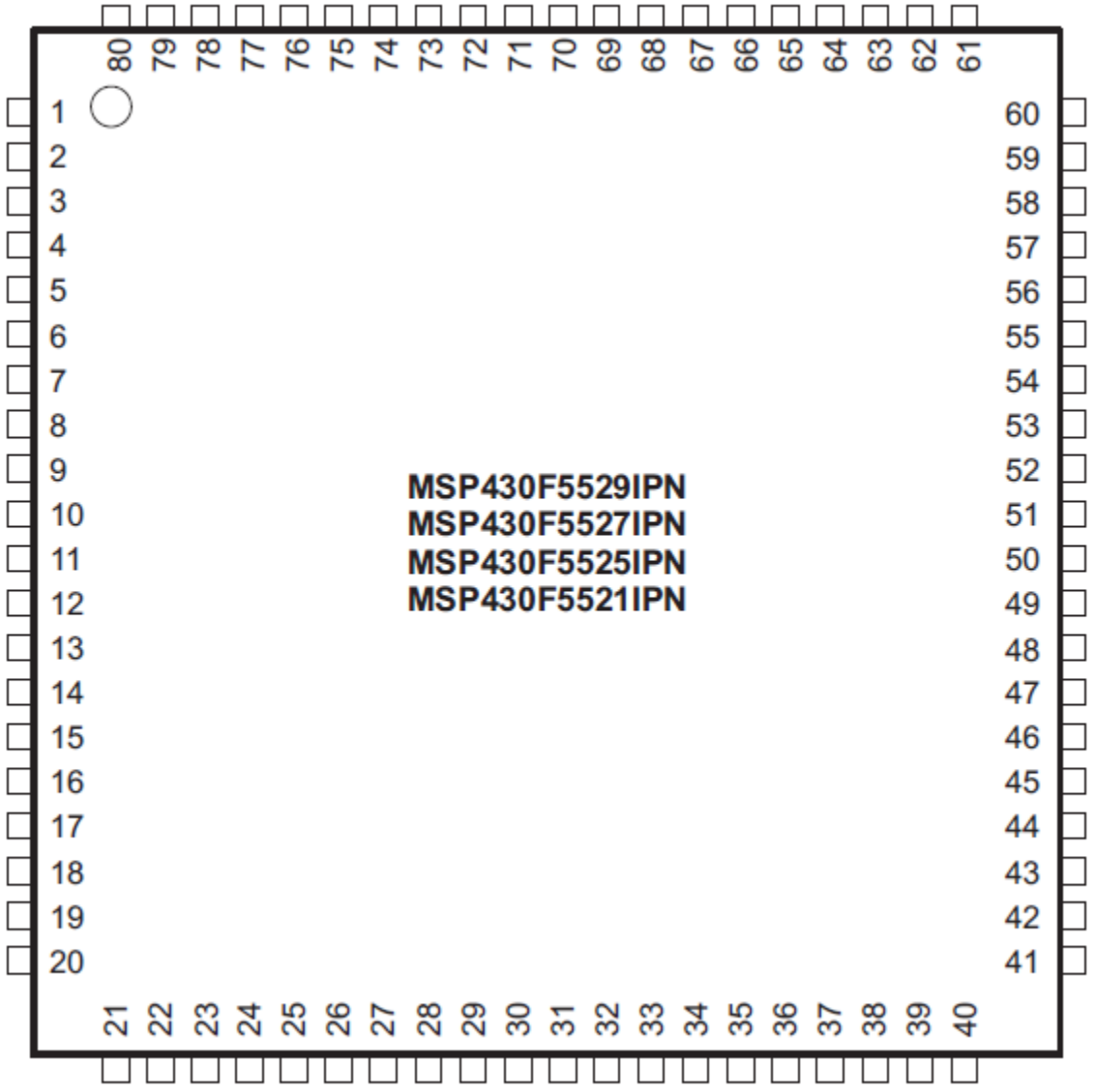
- Portas de entrada/saída configuráveis
- Tamanho : 8-bits
- Cada pino é controlado individualmente
- Alguns pinos podem gerar interrupção
- Pinos controlados por registros mapeados em memória
  - PxIN
  - PxOUT
  - PxDIR
  - PxREN
  - PxSEL
  - PxDS

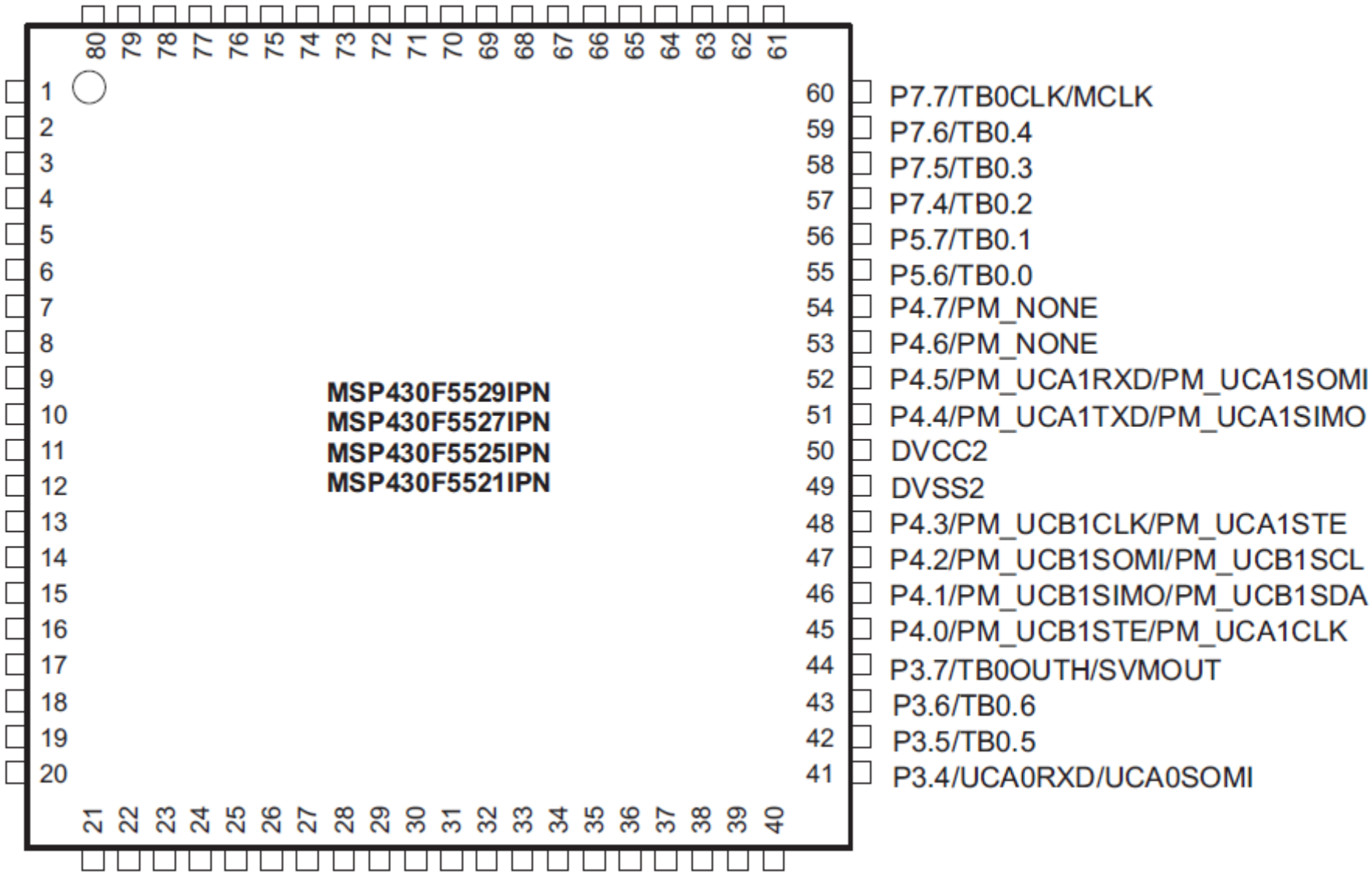
GPIOs

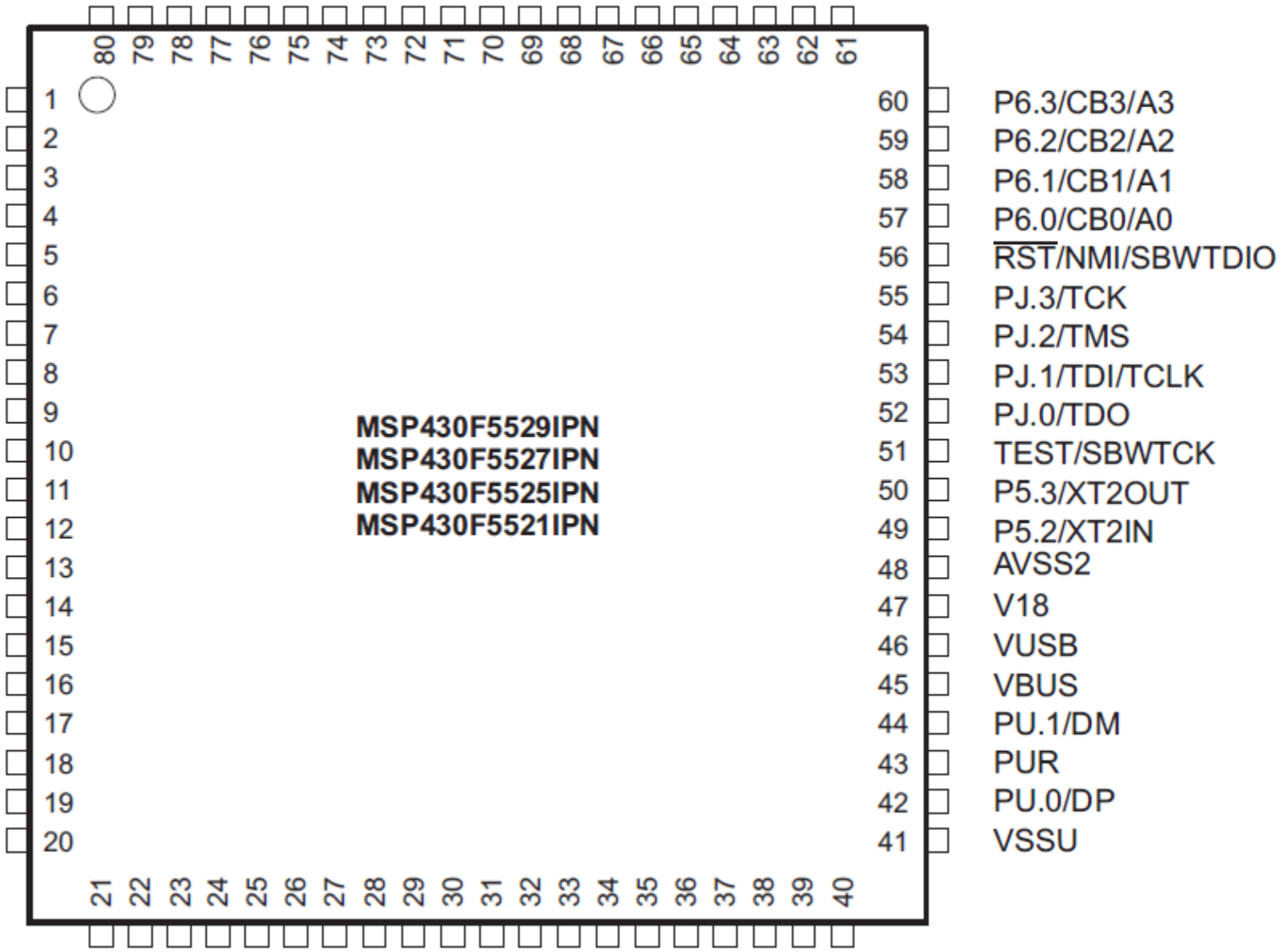

P6.4/CB4/A4
P6.5/CB5/A5
P6.6/CB6/A6
P6.7/CB7/A7
P7.0/CB8/A12
P7.1/CB9/A13
P7.2/CB10/A14
P7.3/CB11/A15
P5.0/A8/VREF+/VeREF+
P5.1/A9/VREF−/VeREF−
AVCC1
P5.4/XIN
P5.5/XOUT
AVSS1
P8.0
P8.1
P8.2
DVCC1
DVSS1
VCORE
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40
41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60
61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80
MSP430F5529IPN
MSP430F5527IPN
MSP430F5525IPN
MSP430F5521IPN

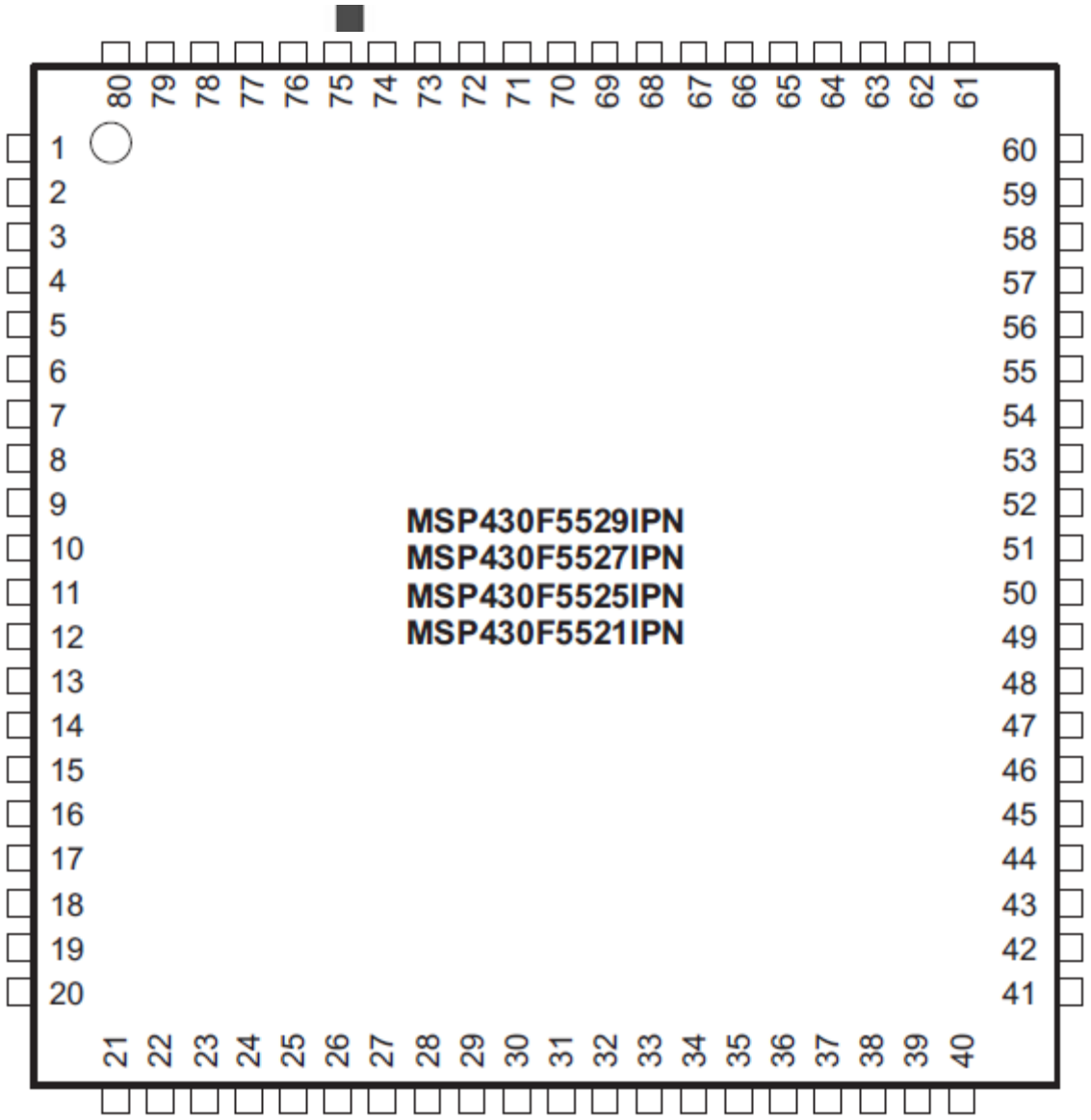

P1.0/TA0CLK/ACLK 1
P1.1/TA0.0 2
P1.2/TA0.1 3
P1.3/TA0.2 4
P1.4/TA0.3 5
P1.5/TA0.4 6
P1.6/TA1CLK/CBOUT 7
P1.7/TA1.0 8
P2.0/TA1.1 9
P2.1/TA1.2 10
P2.2/TA2CLK/SMCLK 11
P2.3/TA2.0 12
P2.4/TA2.1 13
P2.5/TA2.2 14
P2.6/RTCCLK/DMAE0 15
P2.7/UCB0STE/UCA0CLK 16
P3.0/UCB0SIMO/UCB0SDA 17
P3.1/UCB0SOMI/UCB0SCL 18
P3.2/UCB0CLK/UCA0STE 19
P3.3/UCA0TXD/UCA0SIMO 20
21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40
41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60
61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80
MSP430F5529IPN
MSP430F5527IPN
MSP430F5525IPN
MSP430F5521IPN


MSP430F5529IPN
MSP430F5527IPN
MSP430F5525IPN
MSP430F5521IPN


MSP430F5529IPN
MSP430F5527IPN
MSP430F5525IPN
MSP430F5521IPN


MSP430F5529IPN
MSP430F5527IPN
MSP430F5525IPN
MSP430F5521IPN
1 P7.7/TB0CLK/MCLK
2 P7.6/TB0.4
3 P7.5/TB0.3
4 P7.4/TB0.2
5 P5.7/TB0.1
6 P5.6/TB0.0
7 P4.7/PM_NONE
8 P4.6/PM_NONE
9 P4.5/PM_UCA1RXD/PM_UCA1SOMI
10 P4.4/PM_UCA1TXD/PM_UCA1SIMO
11 DVCC2
12 DVSS2
13 P4.3/PM_UCB1CLK/PM_UCA1STE
14 P4.2/PM_UCB1SOMI/PM_UCB1SCL
15 P4.1/PM_UCB1SIMO/PM_UCB1SDA
16 P4.0/PM_UCB1STE/PM_UCA1CLK
17 P3.7/TB0OUTH/SVMOUT
18 P3.6/TB0.6
19 P3.5/TB0.5
20 P3.4/UCA0RXD/UCA0SOMI
21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40
41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60
61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80


MSP430F5529IPN
MSP430F5527IPN
MSP430F5525IPN
MSP430F5521IPN
1 P6.3/CB3/A3
2 P6.2/CB2/A2
3 P6.1/CB1/A1
4 P6.0/CB0/A0
5 RST/NMI/SBWTDIO
6 PJ.3/TCK
7 PJ.2/TMS
8 PJ.1/TDI/TCLK
9 PJ.0/TDO
10 TEST/SBWTCK
11 P5.3/XT2OUT
12 P5.2/XT2IN
13 AVSS2
14 V18
15 VUSB
16 VBUS
17 PU.1/DM
18 PUR
19 PU.0/DP
20 VSSU


MSP430F5529IPN
MSP430F5527IPN
MSP430F5525IPN
MSP430F5521IPN
1
2
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4
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10
11
12
13
14
15
16
17
18
19
20
21
22
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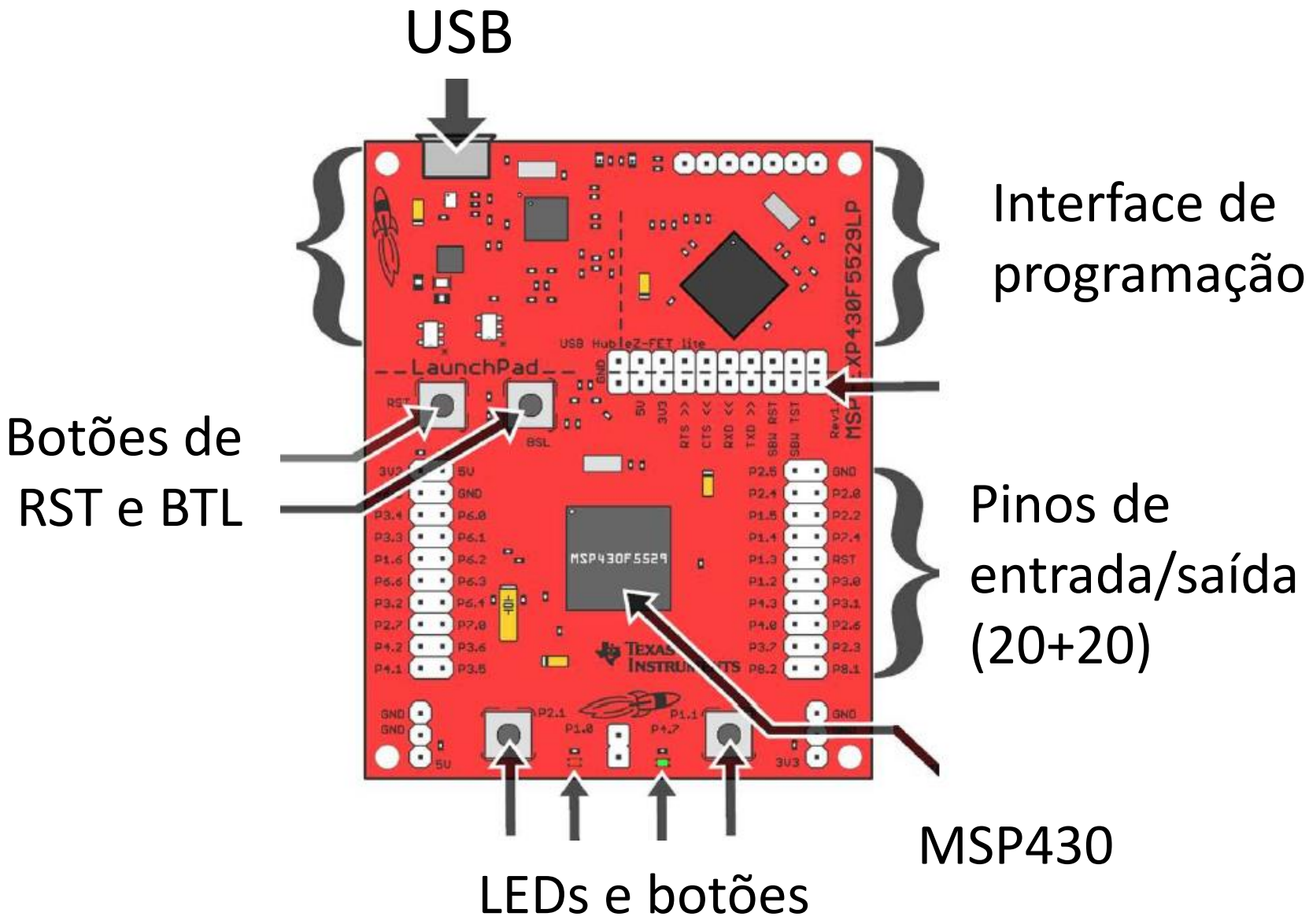
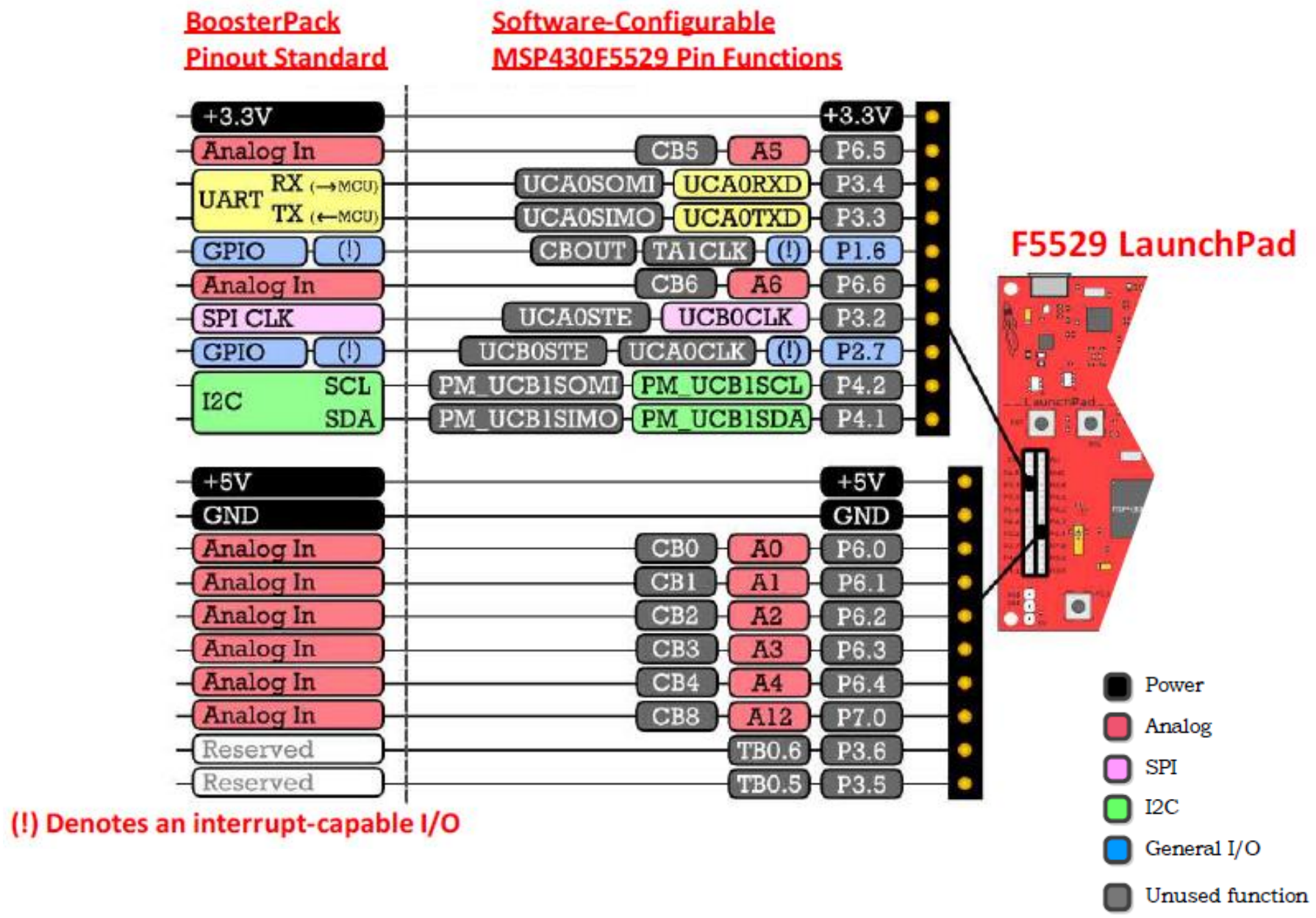
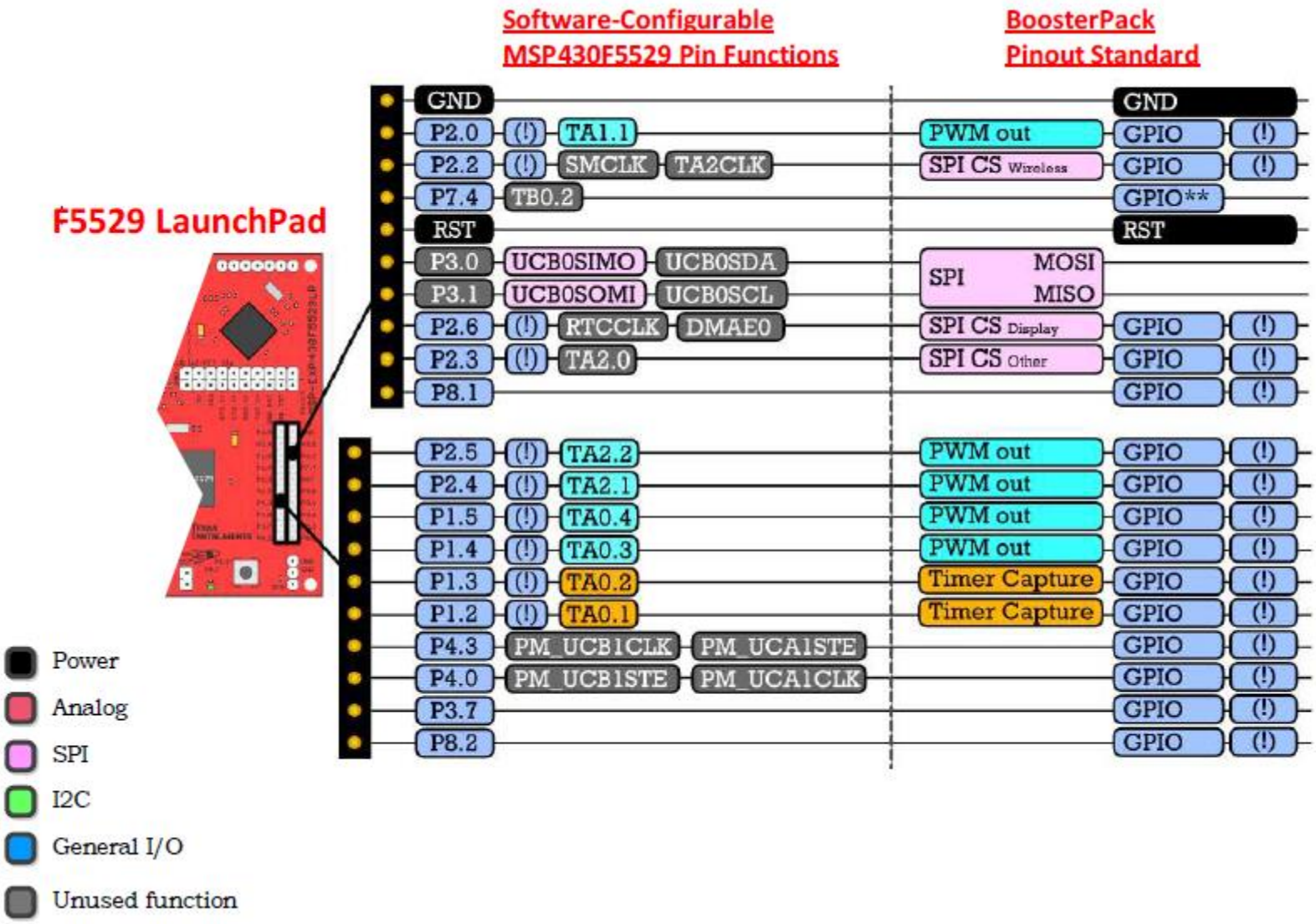
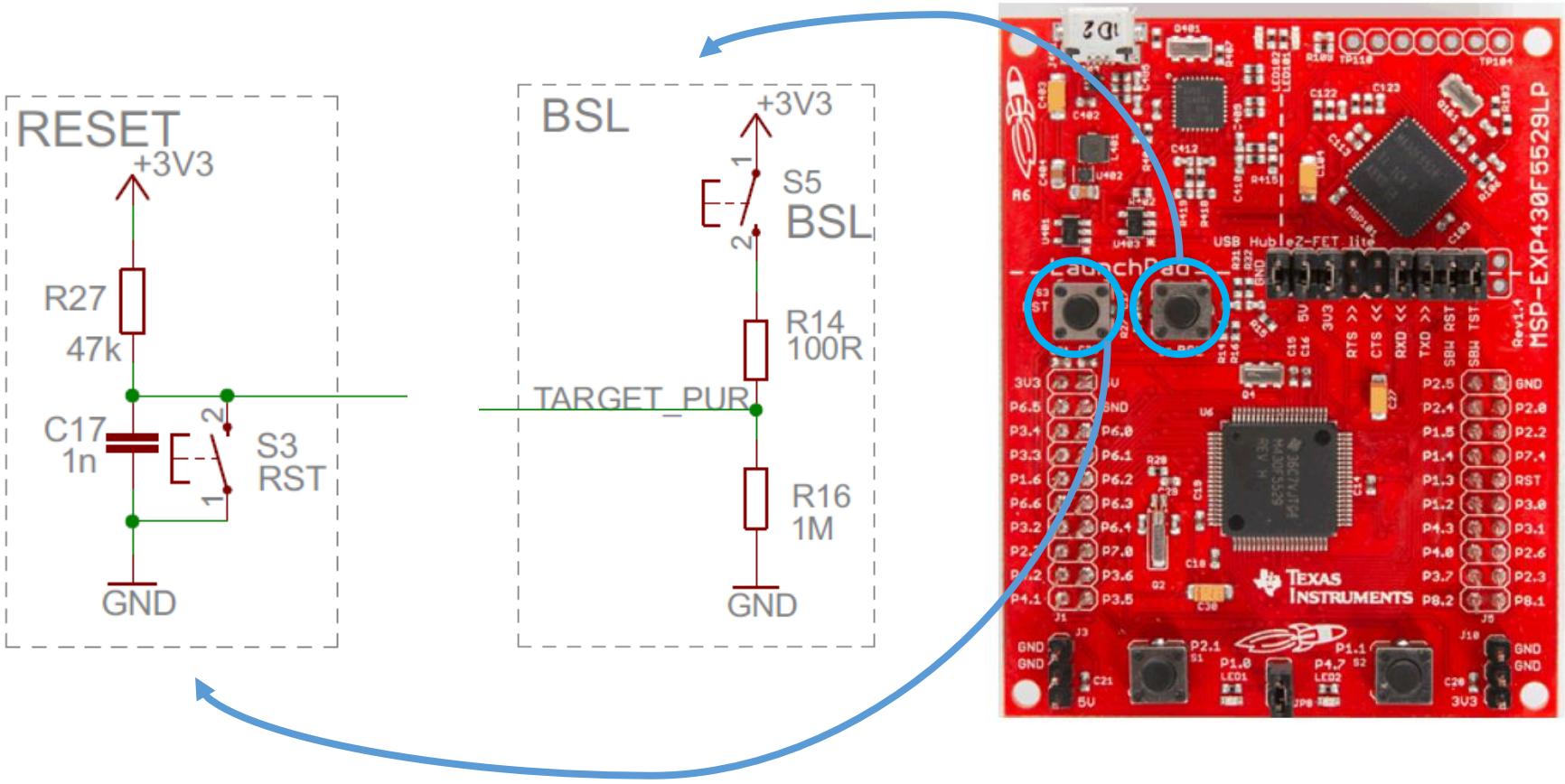

USB
Interface de programação
Botões de RST e BTL
Pinos de entrada/saída (20+20)
MSP430
LEDs e botões
LaunchPad
MSP430F5529
MSP-EXP430F5529LP


BoosterPack
Pinout Standard
Software-Configurable
MSP430F5529 Pin Functions
+3.3V
Analog In
UART RX (→MCU)
TX (←MCU)
GPIO (!)
Analog In
SPI CLK
GPIO (!)
I2C SCL
SDA
+5V
GND
Analog In
Analog In
Analog In
Analog In
Analog In
Reserved
Reserved
+3.3V
CB5 A5 P6.5
UCA0SOMI UCA0RXD P3.4
UCA0SIMO UCA0TXD P3.3
CBOUT TA1CLK (!) P1.6
CB6 A6 P6.6
UCA0STE UCB0CLK P3.2
UCB0STE UCA0CLK (!) P2.7
PM_UCB1SOMI PM_UCB1SCL P4.2
PM_UCB1SIMO PM_UCB1SDA P4.1
+5V
GND
CB0 A0 P6.0
CB1 A1 P6.1
CB2 A2 P6.2
CB3 A3 P6.3
CB4 A4 P6.4
CB8 A12 P7.0
TB0.6 P3.6
TB0.5 P3.5
F5529 LaunchPad
Power
Analog
SPI
I2C
General I/O
Unused function
(!) Denotes an interrupt-capable I/O


Software-Configurable
MSP430F5529 Pin Functions
BoosterPack
Pinout Standard
F5529 LaunchPad
GND
P2.0 (!) TA1.1
P2.2 (!) SMCLK TA2CLK
P7.4 TB0.2
RST
P3.0 UCB0SIMO UCB0SDA
P3.1 UCB0SOMI UCB0SCL
P2.6 (!) RTCCLK DMAE0
P2.3 (!) TA2.0
P8.1
P2.5 (!) TA2.2
P2.4 (!) TA2.1
P1.5 (!) TA0.4
P1.4 (!) TA0.3
P1.3 (!) TA0.2
P1.2 (!) TA0.1
P4.3 PM_UCB1CLK PM_UCA1STE
P4.0 PM_UCB1STE PM_UCA1CLK
P3.7
P8.2
PWM out
SPI CS Wireless
SPI MOSI MISO
SPI CS Display
SPI CS Other
Timer Capture
GPIO
GPIO**
(!)
Power
Analog
SPI
I2C
General I/O
Unused function

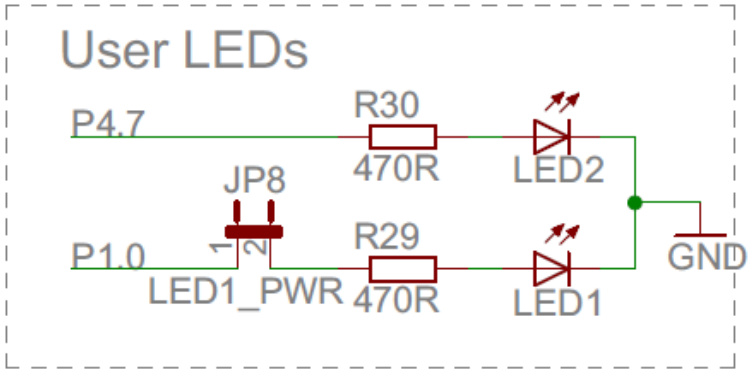
GPIOs

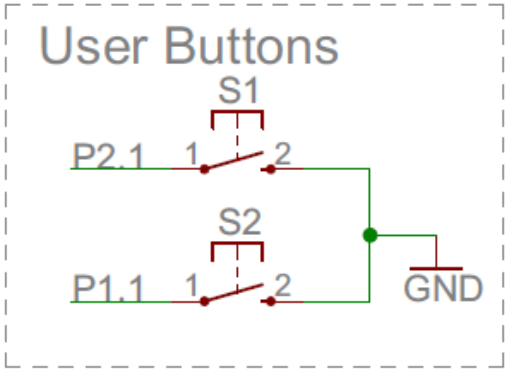
- Botões e LEDs

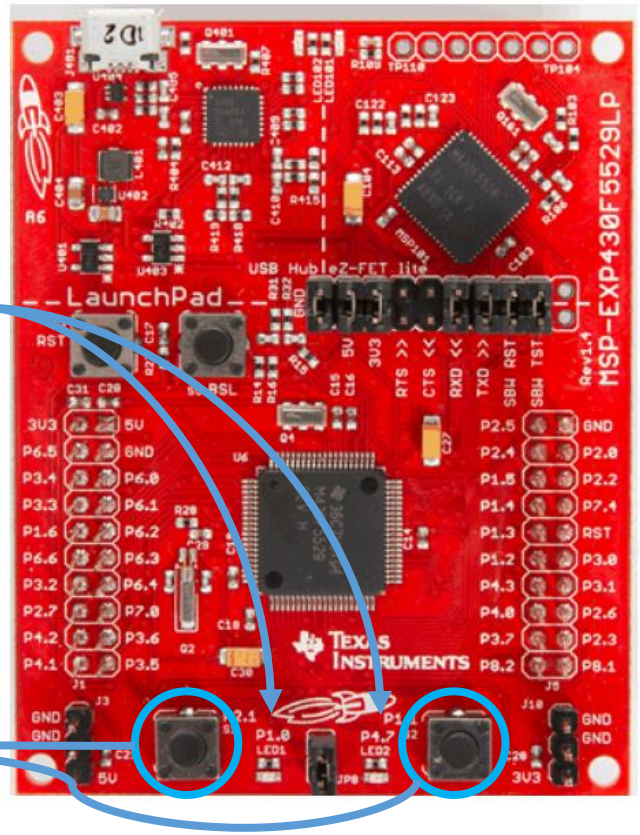


GPIOs

- Botões e LEDs

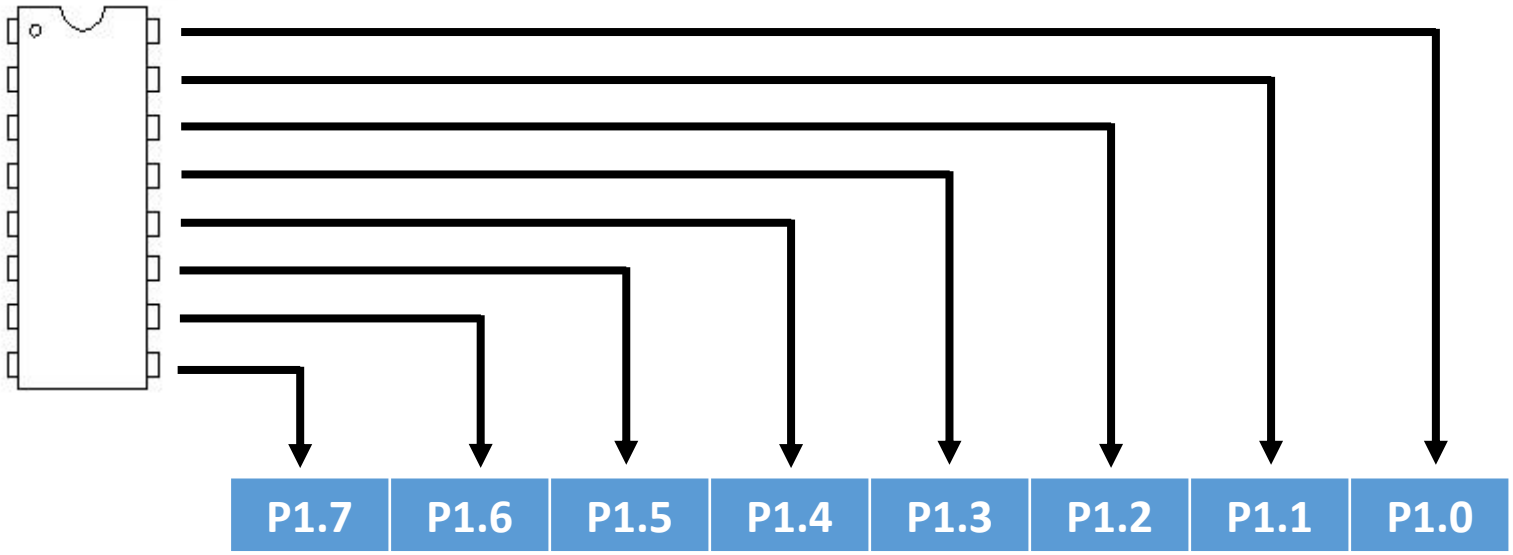






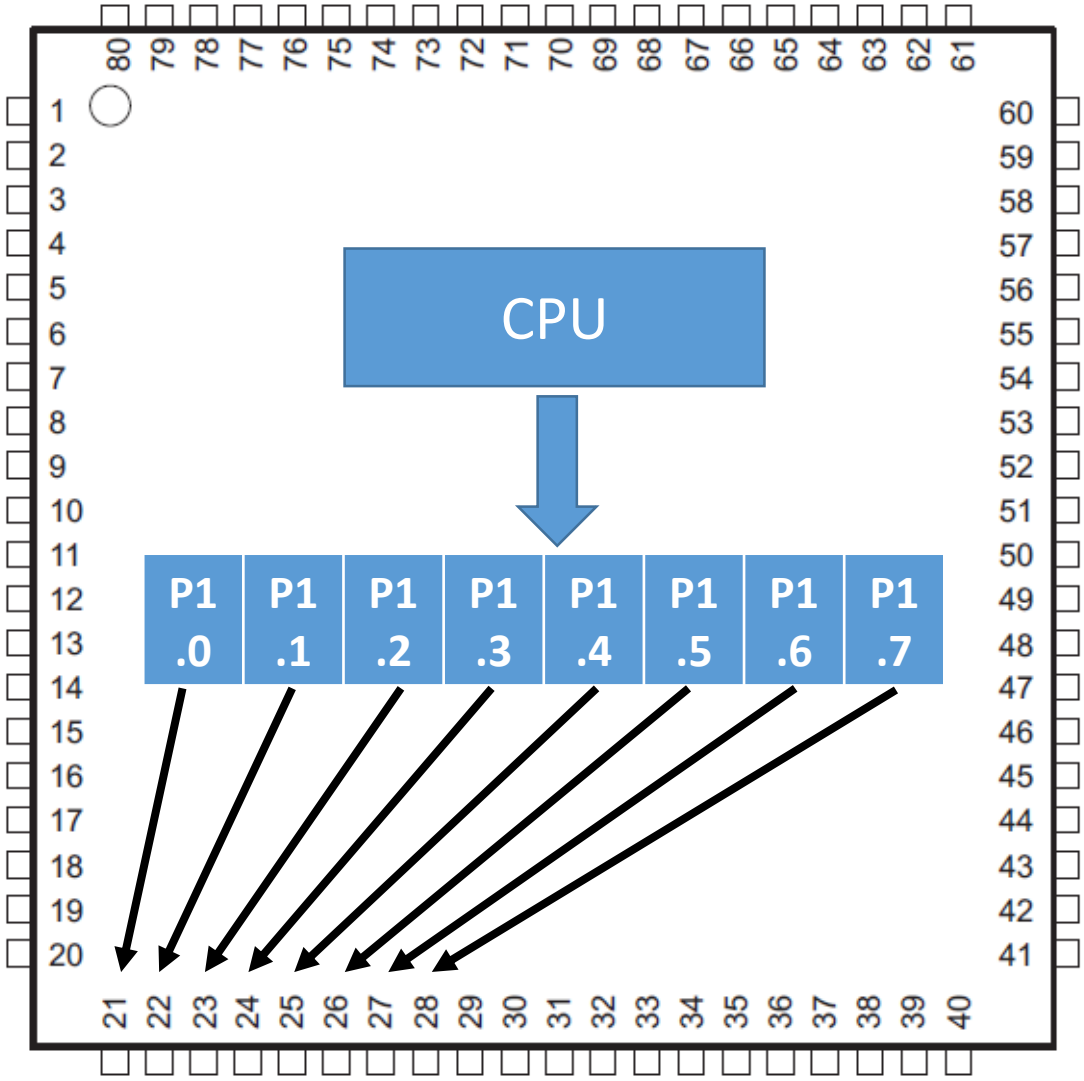
GPIOs

- Configuração a base de registros

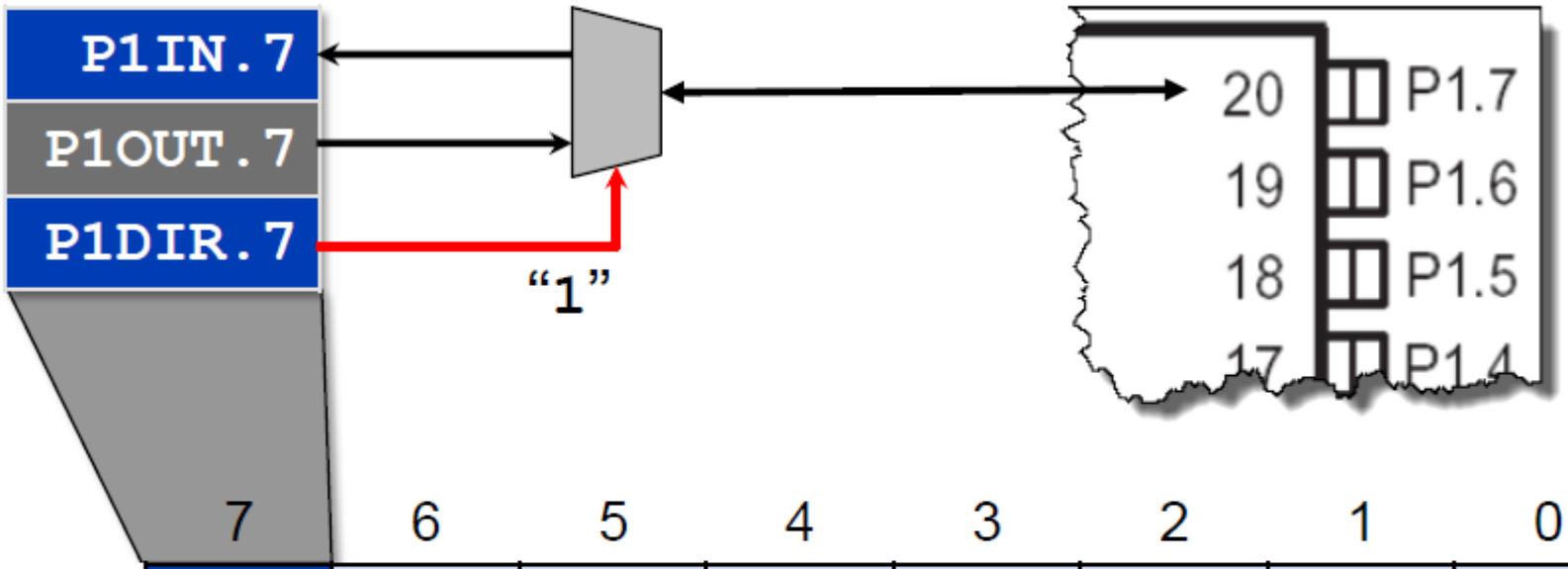


GPIOs

- Configuração a base de registros

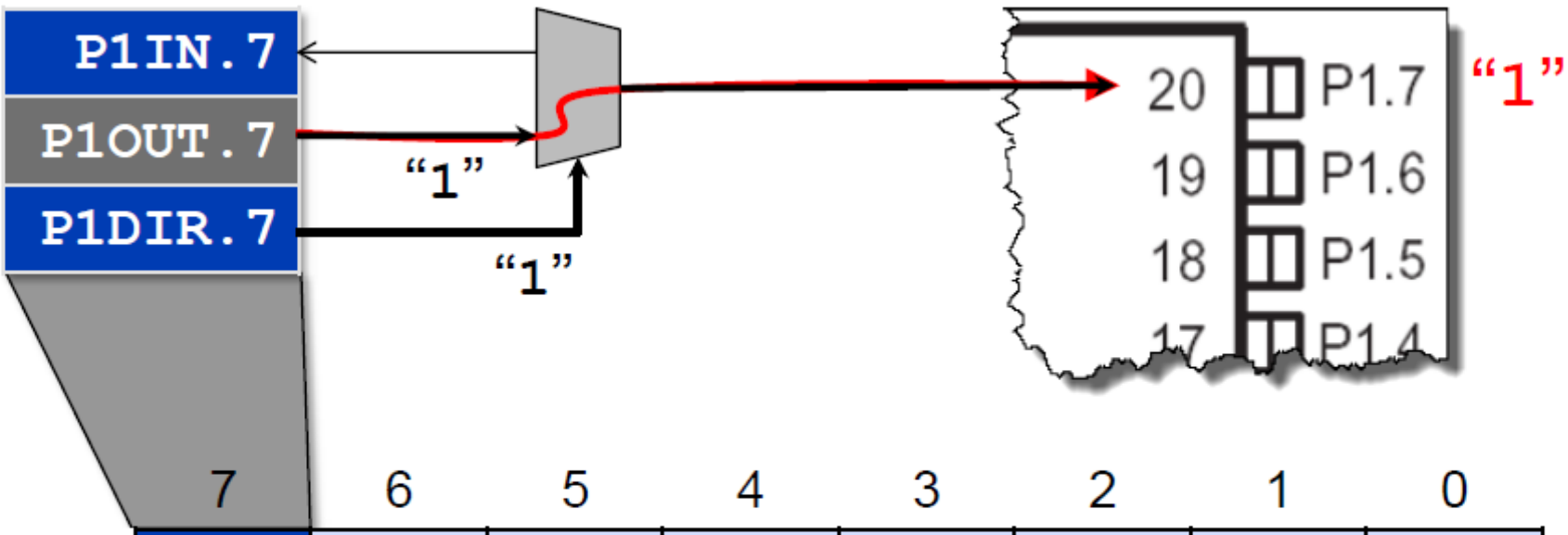


GPIOs



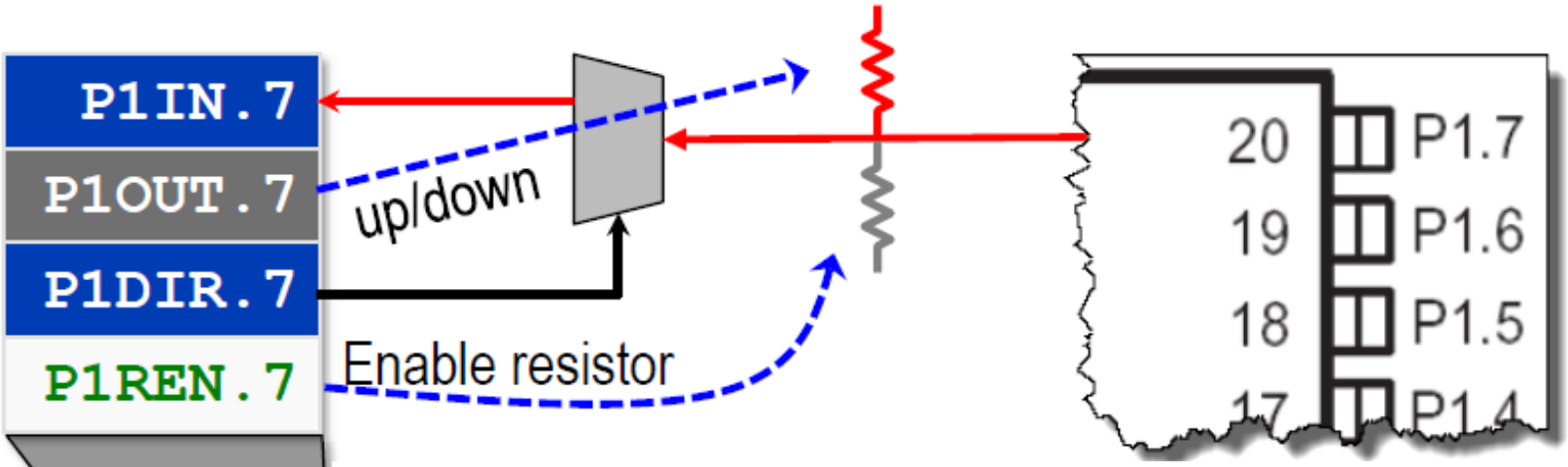
	7	6	5	4	3	2	1	0
P1IN								
P1OUT								
P1DIR	1							

GPIOs



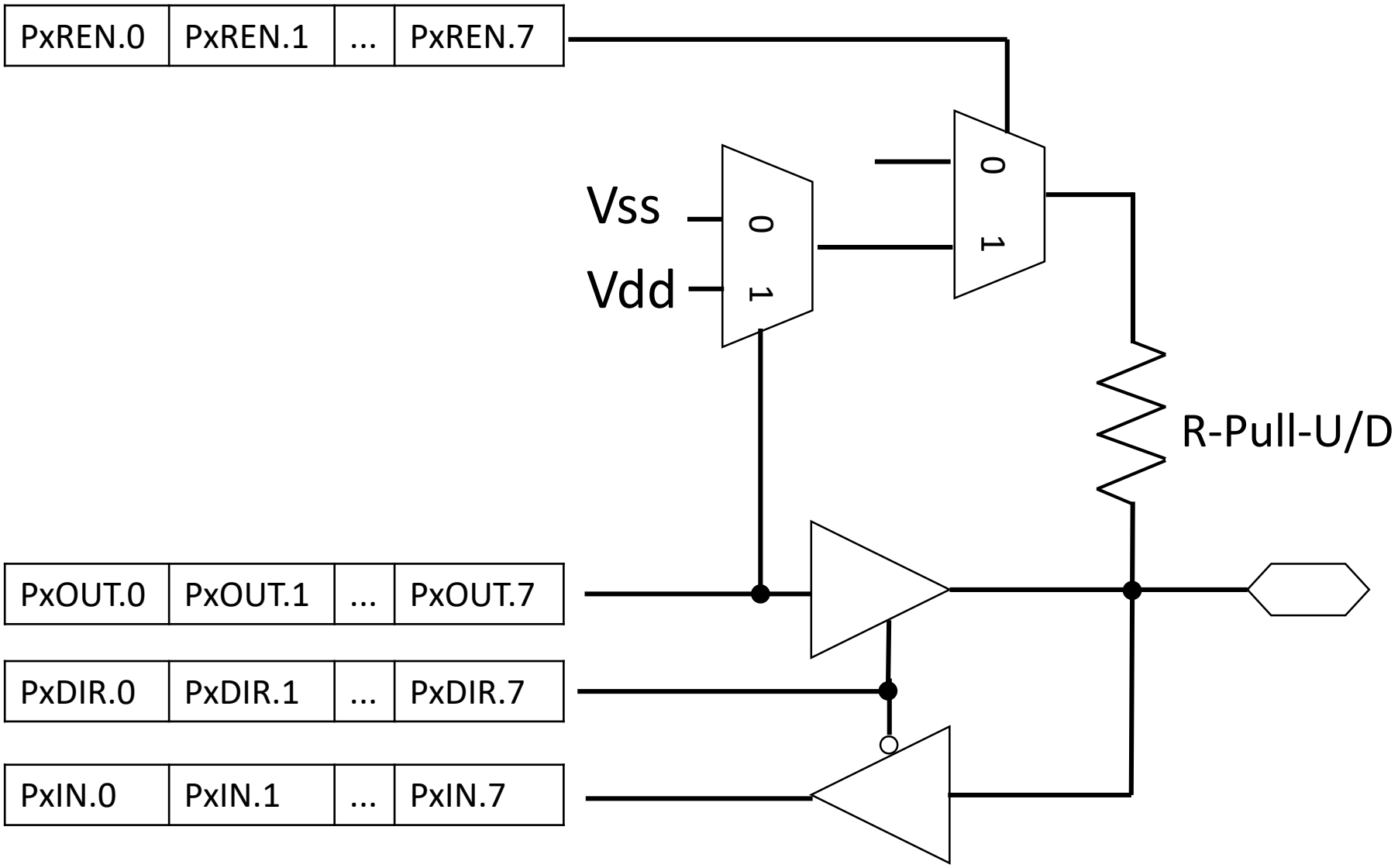
	7	6	5	4	3	2	1	0
P1IN	x							
P1OUT	1							
P1DIR	1							

GPIOs



	7
P1IN	x
P1OUT	1
P1DIR	0
P1REN	1

- Quando configurados como entrada, pode-se escolher um resistor de pull-up ou pull-down.
- Se não houver nada conectado no pino, esses resistores determinam um valor “padrão” de leitura


PxREN.0
PxREN.1
...
PxREN.7
Vss
Vdd
0
1
0
1
R-Pull-U/D
PxOUT.0
PxOUT.1
...
PxOUT.7
PxDIR.0
PxDIR.1
...
PxDIR.7
PxIN.0
PxIN.1
...
PxIN.7

PxREN.0	PxREN.1	...	PxREN.7

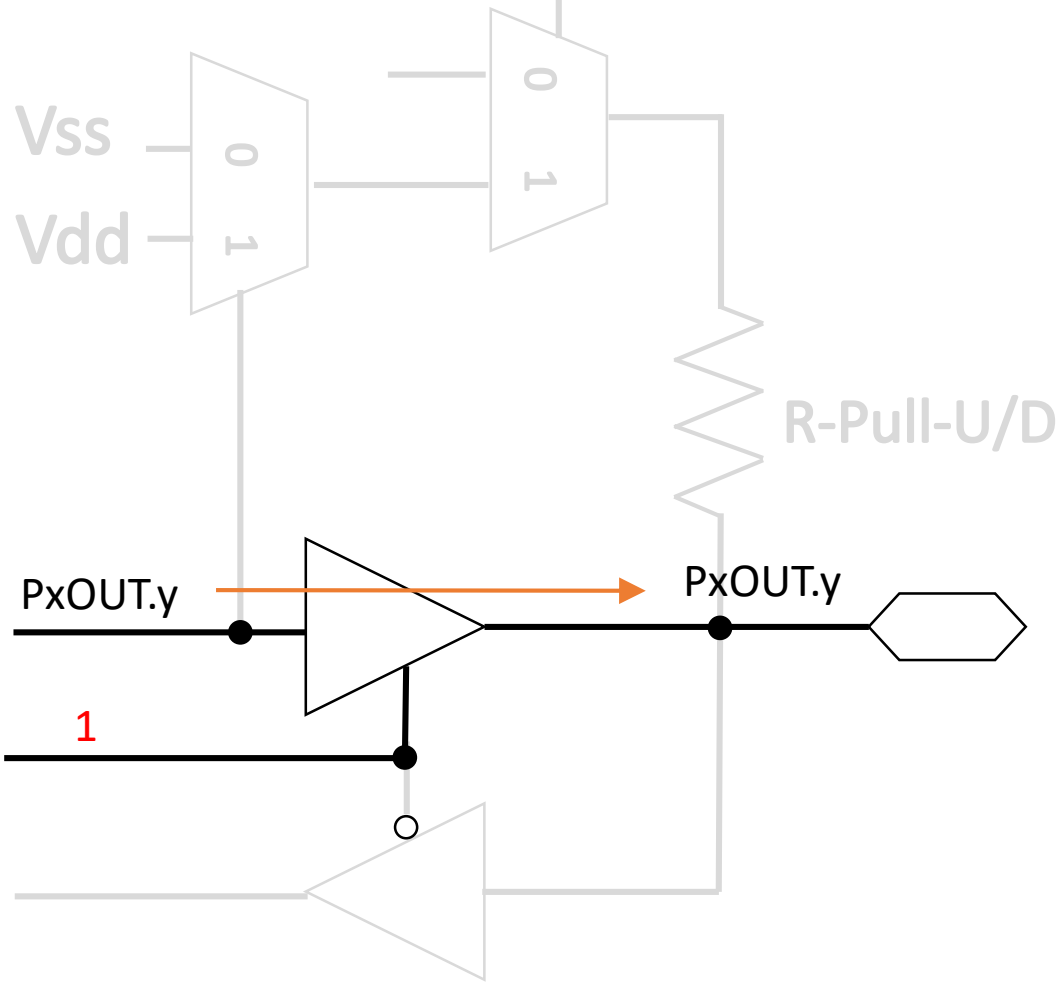
- Configurando como saída

- PxDIR.y = 1
- Output = PxOUT.y

PxOUT.0	PxOUT.1	...	PxOUT.7

PxDIR.0	PxDIR.1	...	PxDIR.7

PxIN.0	PxIN.1	...	PxIN.7



PxREN.0	PxREN.1	...	PxREN.7

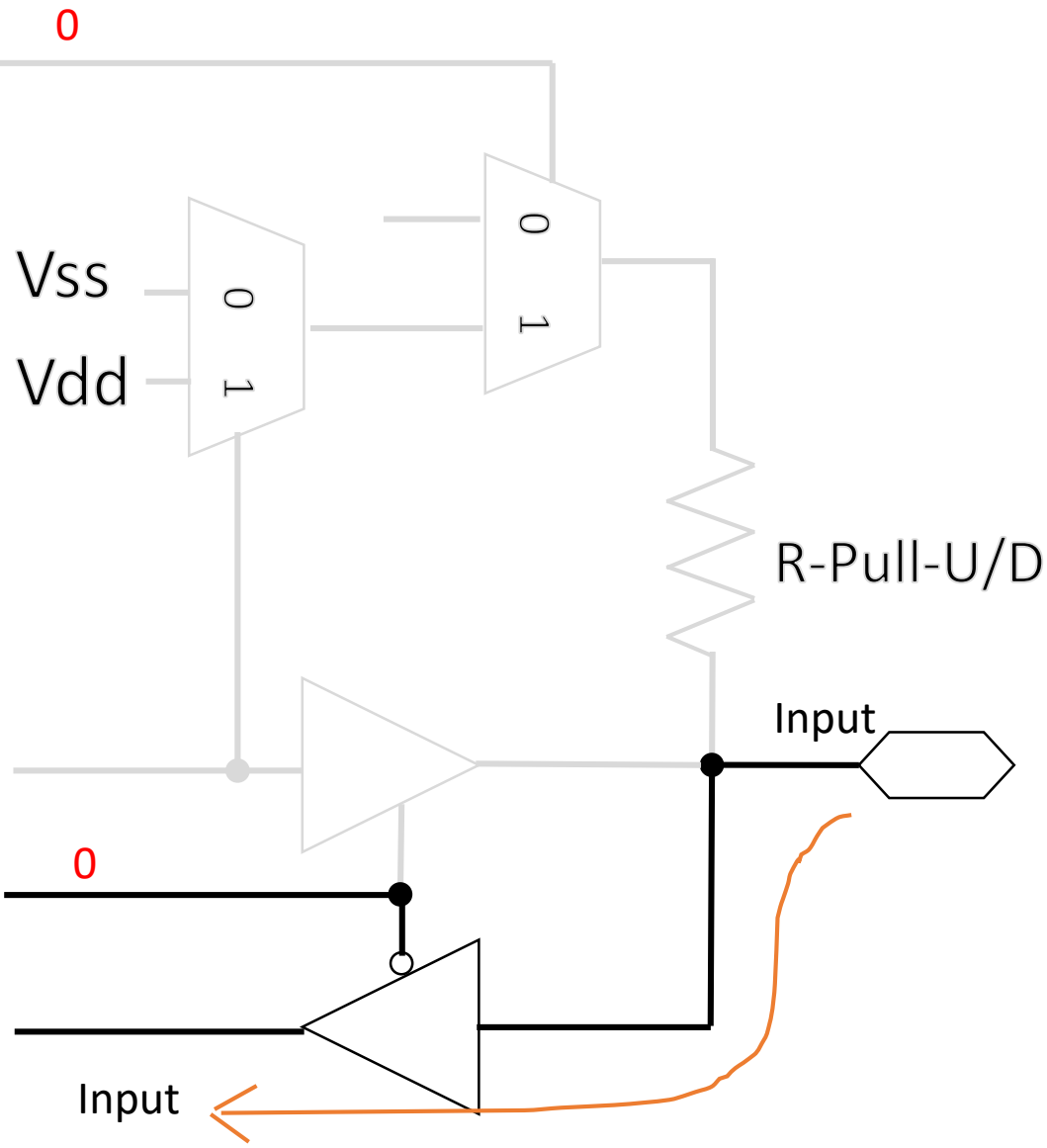
- Configurando como entrada sem resistor de pull-up/down

- PxDIR.y = 0
- PxREN.y = 0
- PxOUT.y = x
- PxIN.y = Input

PxOUT.0	PxOUT.1	...	PxOUT.7

PxDIR.0	PxDIR.1	...	PxDIR.7

PxIN.0	PxIN.1	...	PxIN.7



PxREN.0	PxREN.1	...	PxREN.7

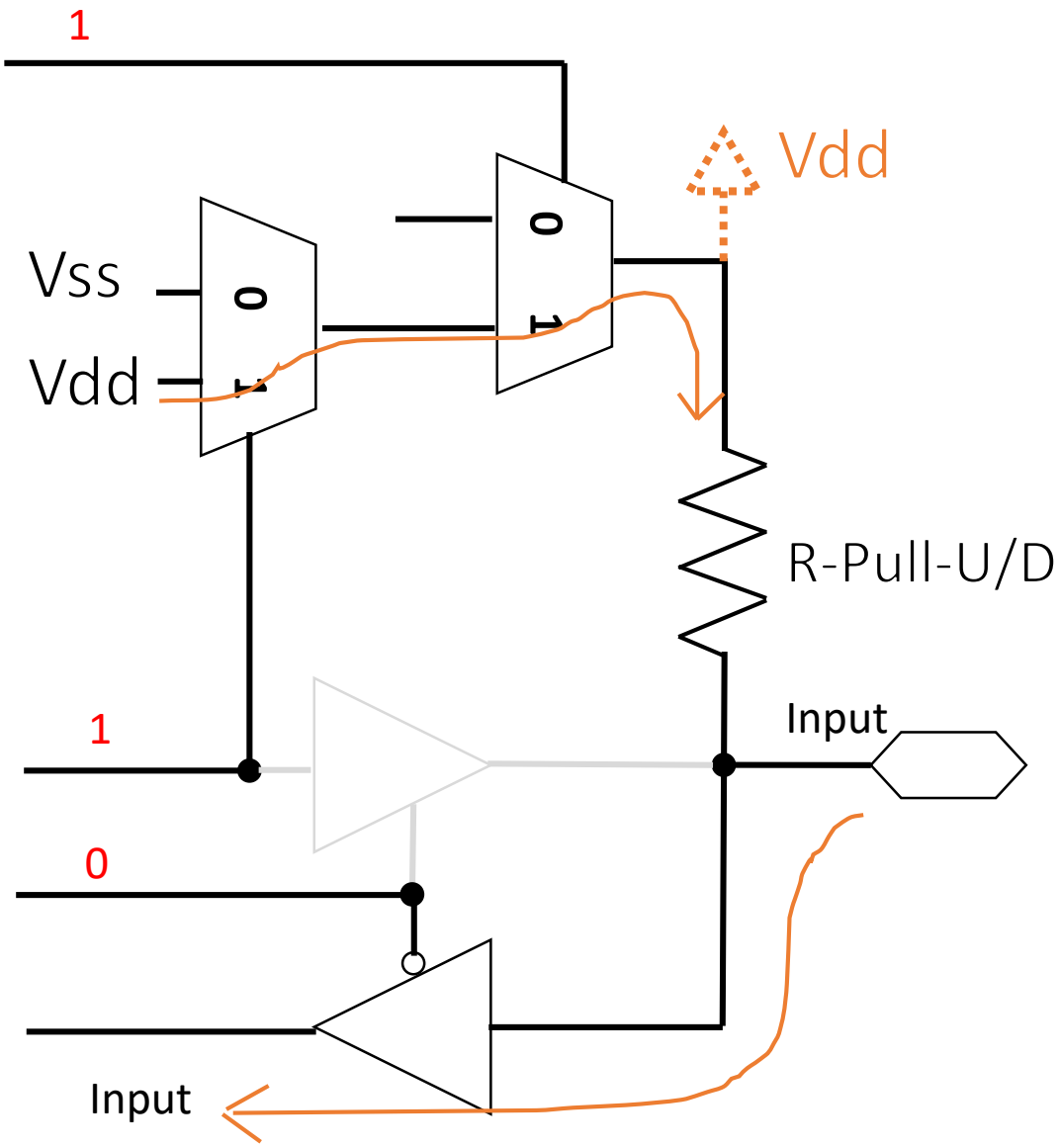
- Entrada com resistor de **pull-up**

- PxDIR.y = 0
- PxREN.y = 0
- PxOUT.y = 1
- PxIN.y = Input

PxOUT.0	PxOUT.1	...	PxOUT.7

PxDIR.0	PxDIR.1	...	PxDIR.7

PxIN.0	PxIN.1	...	PxIN.7



PxREN.0	PxREN.1	...	PxREN.7

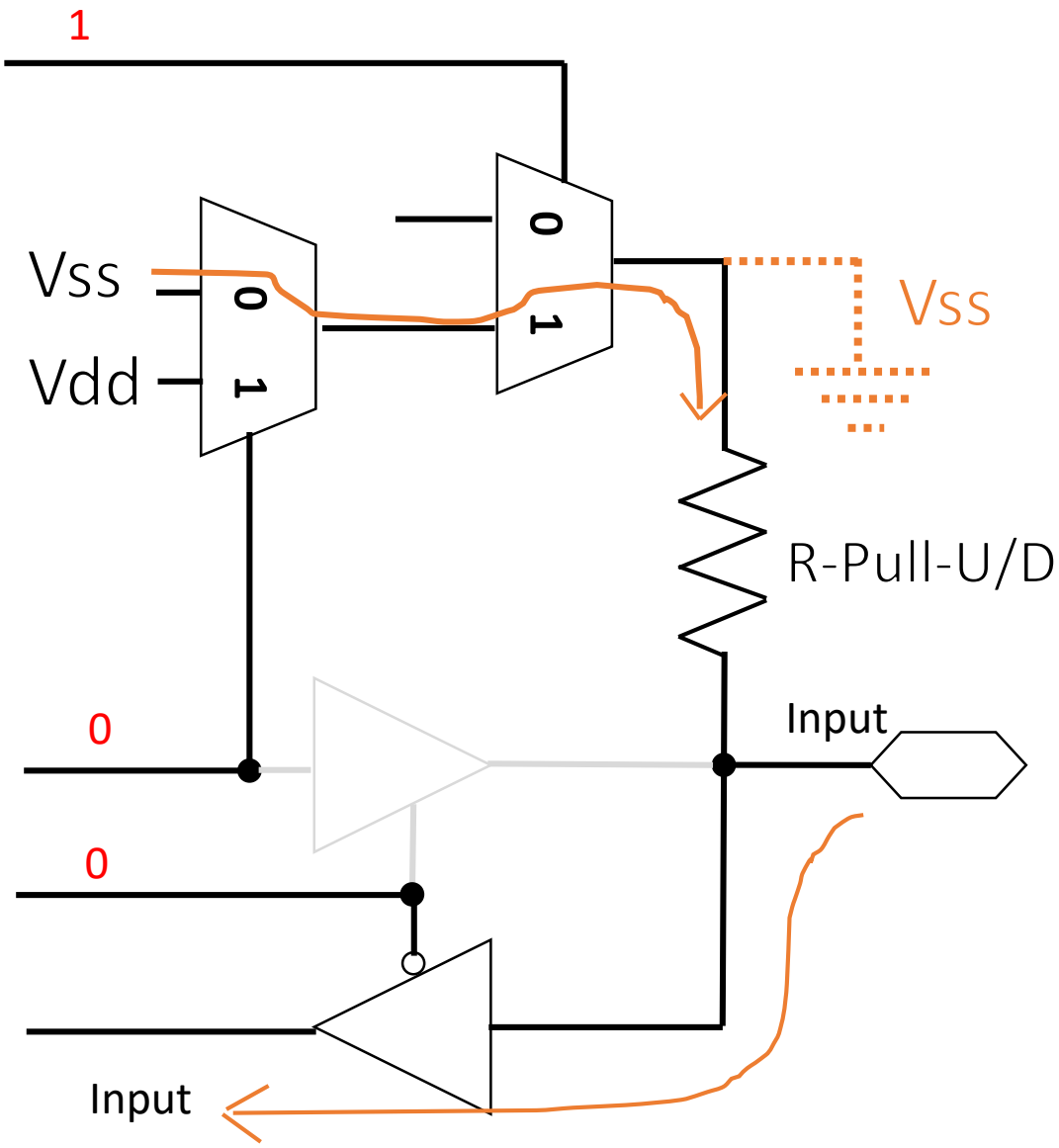
- Entrada com resistor de **pull-down**

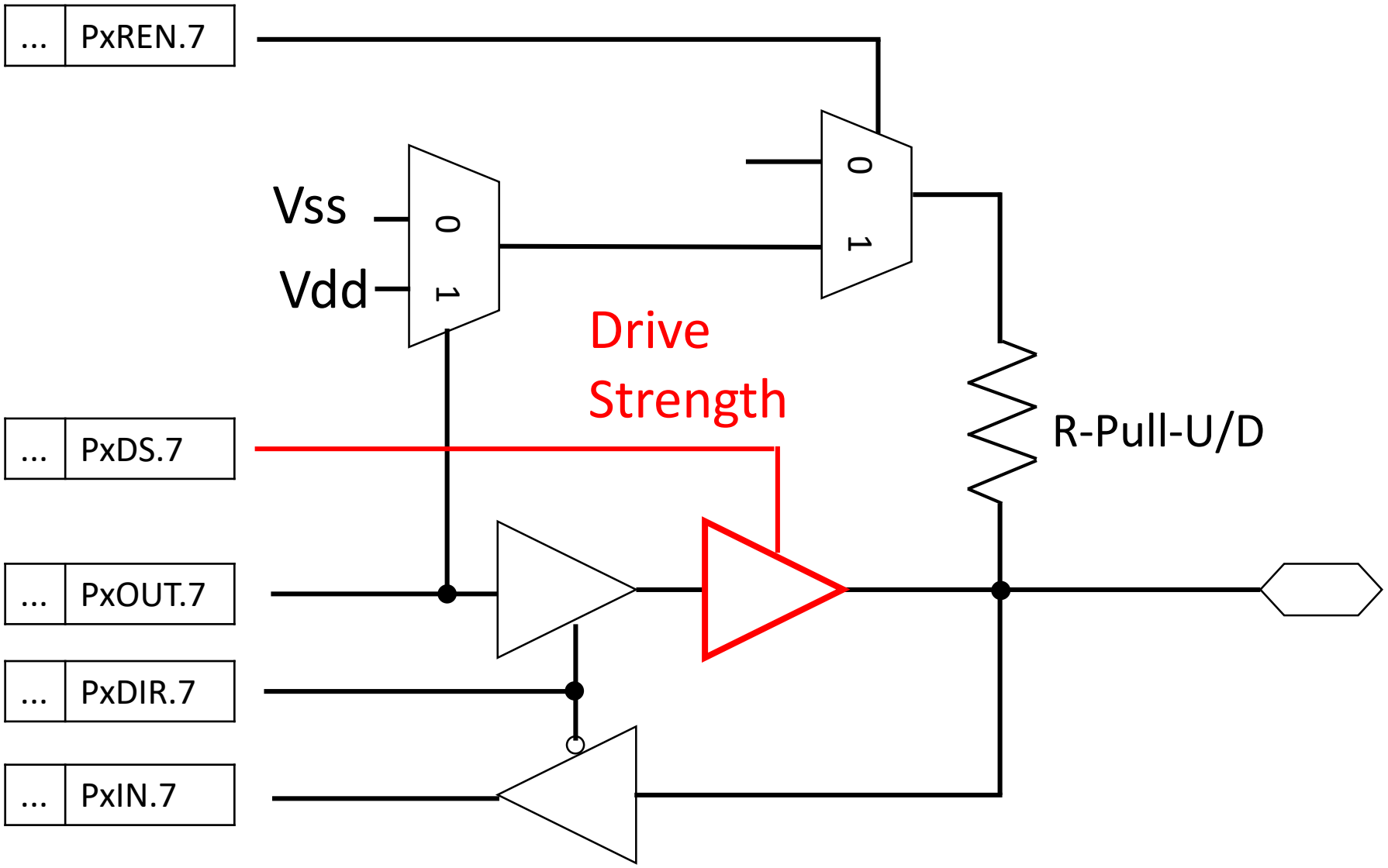
- PxDIR.y = 0
- PxREN.y = 0
- PxOUT.y = 1
- PxIN.y = Input

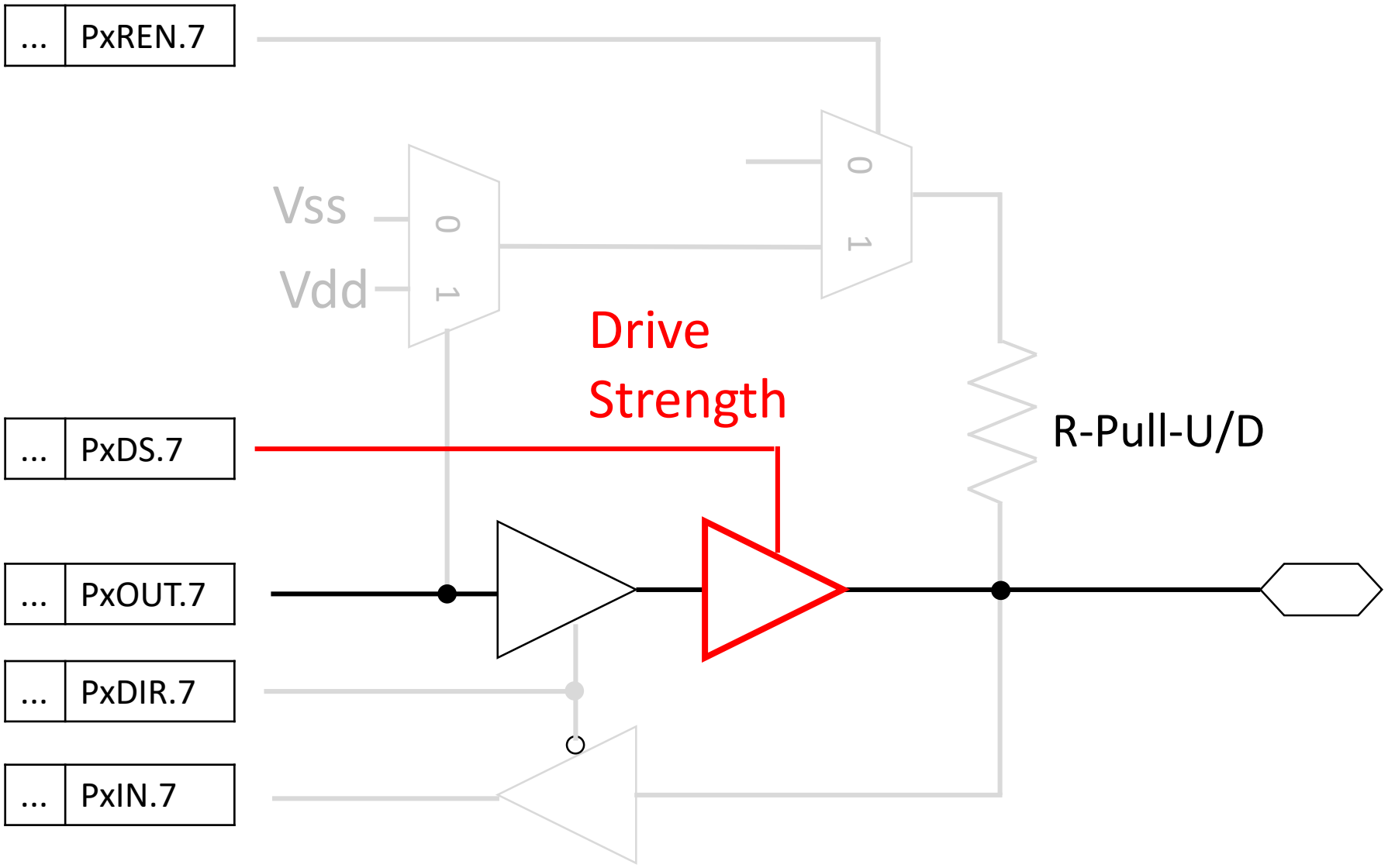
PxOUT.0	PxOUT.1	...	PxOUT.7

PxDIR.0	PxDIR.1	...	PxDIR.7

PxIN.0	PxIN.1	...	PxIN.7

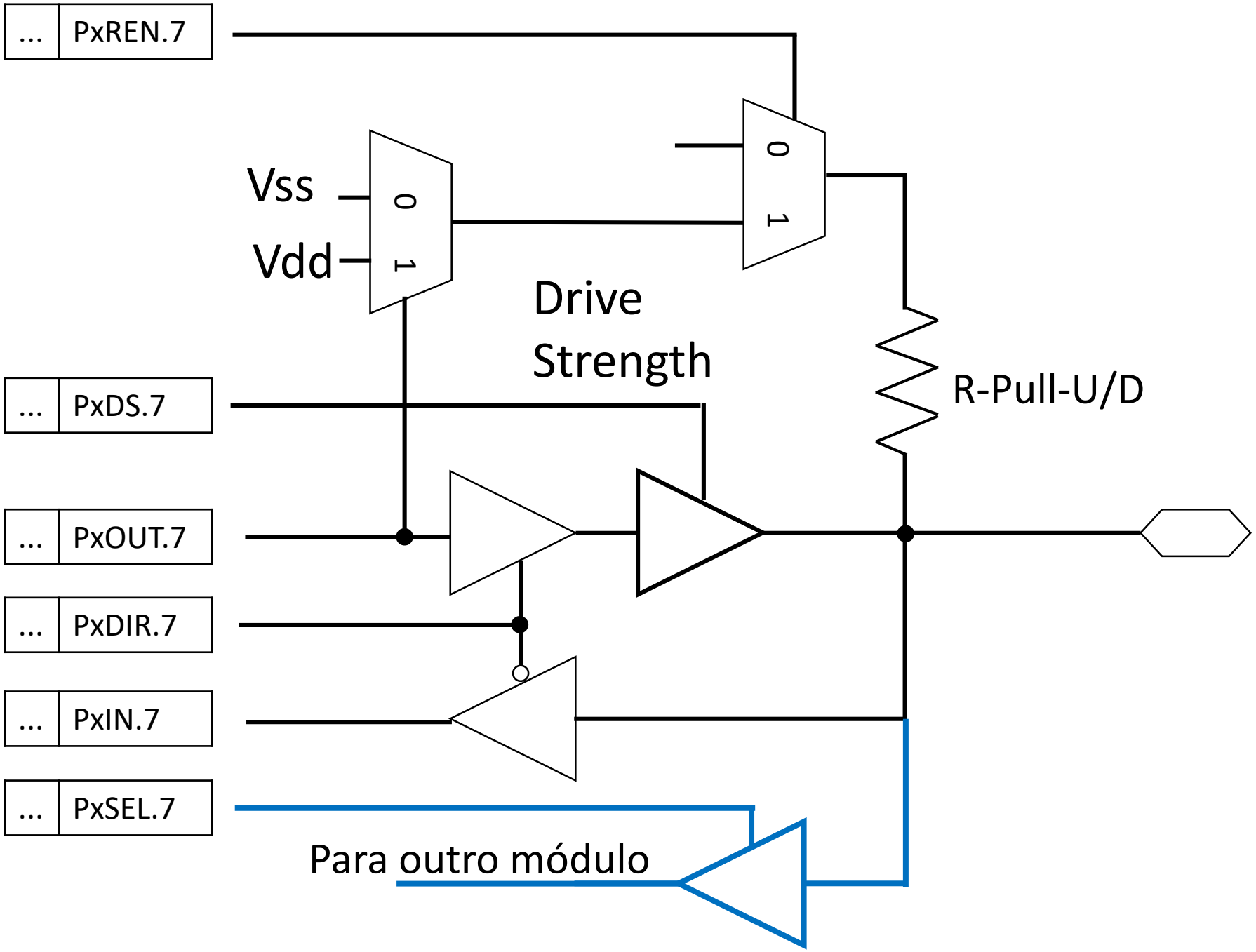


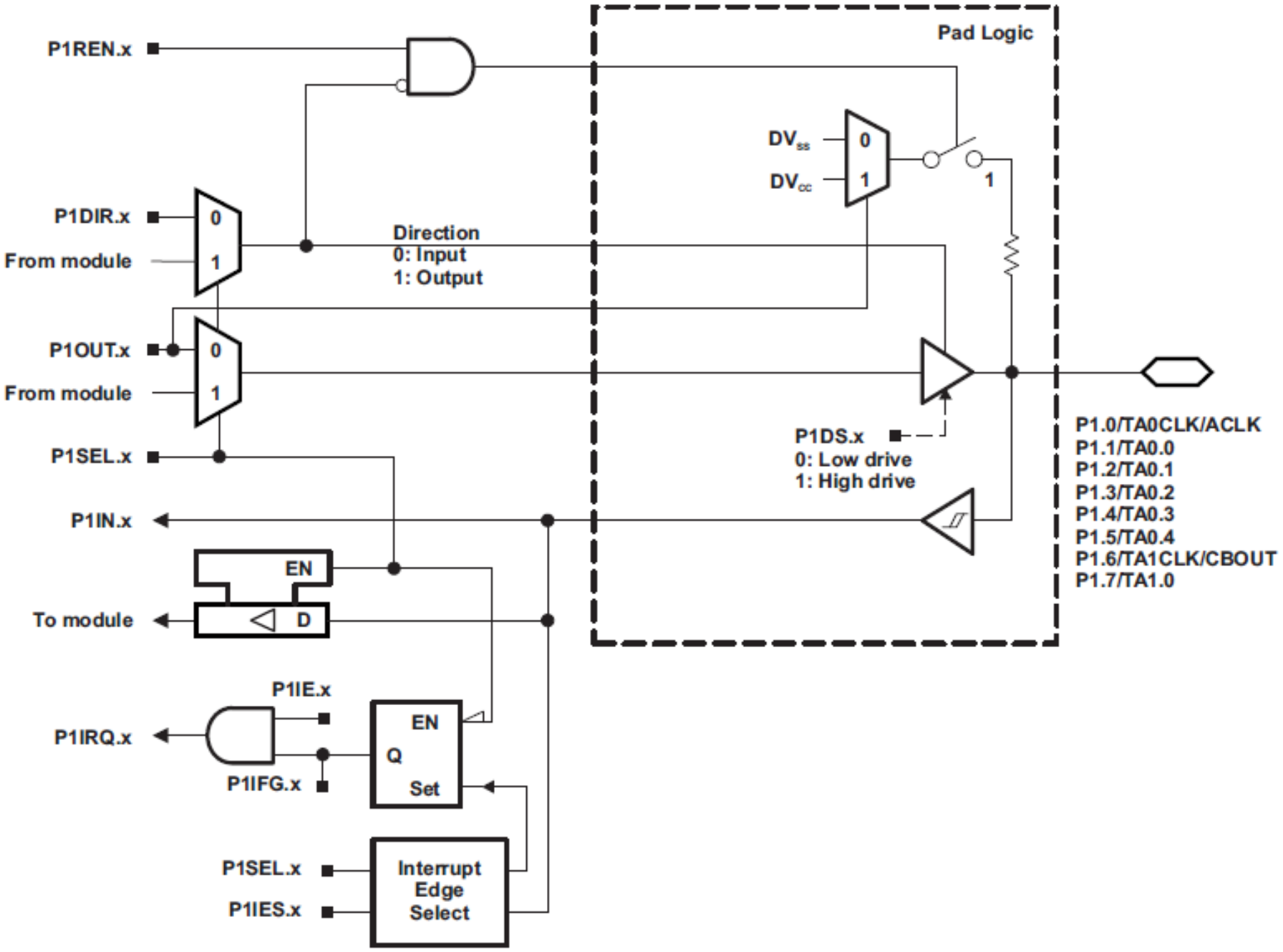

...
PxREN.7
Vss
Vdd
0
1
0
1
Drive
Strength
R-Pull-U/D
...
PxDS.7
...
PxOUT.7
...
PxDIR.7
...
PxIN.7


... PxREN.7
Vss
Vdd
0
1
0
1
Drive
Strength
R-Pull-U/D
... PxDS.7
... PxOUT.7
... PxDIR.7
... PxIN.7

GPIOs

- Alguns pinos são compartilhados entre GPIO e algum outro bloco.
- O pino P1 é compartilhado com o TimerA, por exemplo.


... PxREN.7
Vss
Vdd
0
1
0
1
Drive
Strength
R-Pull-U/D
... PxDS.7
... PxOUT.7
... PxDIR.7
... PxIN.7
... PxSEL.7
Para outro módulo


Pad Logic
P1REN.x
P1DIR.x
From module
Direction
0: Input
1: Output
P1OUT.x
From module
P1SEL.x
P1IN.x
EN
To module
D
P1IE.x
P1IRQ.x
P1IFG.x
EN
Q
Set
P1SEL.x
P1IES.x
Interrupt
Edge
Select
DVss
DVcc
0
1
1
P1DS.x
0: Low drive
1: High drive
P1.0/TA0CLK/ACLK
P1.1/TA0.0
P1.2/TA0.1
P1.3/TA0.2
P1.4/TA0.3
P1.5/TA0.4
P1.6/TA1CLK/CBOUT
P1.7/TA1.0

GPIOs - Resumo

- Portas controladas por registros de 8 bits.
  - PxIN
  - PxOUT
  - PxDIR
  - PxREN
  - PxSEL
  - PxDS

- Pinos são controlados individualmente com operações de set, clear e toggle (usando máscaras)

Vetores de interrupção (P1 e P2)

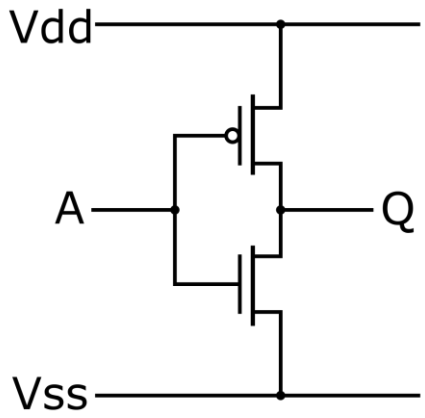
- Uma atividade pode ser ativada por um sinal de um pino qualquer.
- Essa atividade pode ser iniciada através de uma *interrupção*
- Interrupções são geradas por **variações** nos pinos GPIO
- Registros :
  - PxIFG – Interrupt Flag (r/w → swi)
  - PxIE – Interruption Enable
  - PxIES – Interrupt Edge Select (0 → rising, 1 → falling)
  - PxIV – Interrupt Vector

Vetores de interrupção (P1 e P2)

- PxIV – Interrupt Vector
  - Posição na memória que se encontra o programa de interrupção 16-bits (word – 2 bytes)
  - PxIV_H indica o byte mais significativo
  - PxIV_L indica o byte menos significativo

Dicas de operação

- Nunca deixe os pinos desconectados.
  - Conecte externamente os pinos a Vss ou Vdd
  - Configure os pinos como entradas e use um resistor de pull-up ou pull-down para forçar a entrada num valor conhecido (recomendado)
  - Configure os pinos como saídas se seu uC não tiver resistores de pull-up/down (não recomendo)



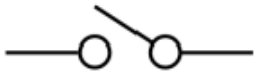
Aspectos analógicos de pinos digitais

Aspectos analógicos de pinos digitais

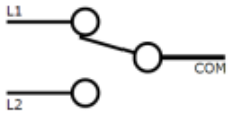
- Switch bouncing
  - Chaves "flutuam" antes do contato e provocam ruído de chaveamento pós contato

Aspectos analógicos de pinos digitais

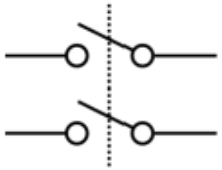
- Switch bouncing
  - Nomenclatura (Número de polos e terminais)
    - SPST – Single Pole, Single Throw



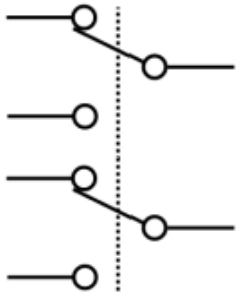
    - SPDT – Single Pole, Double Throw



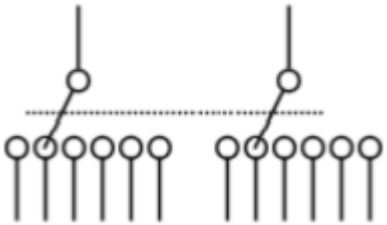
    - DPST – Double Pole, Single Throw



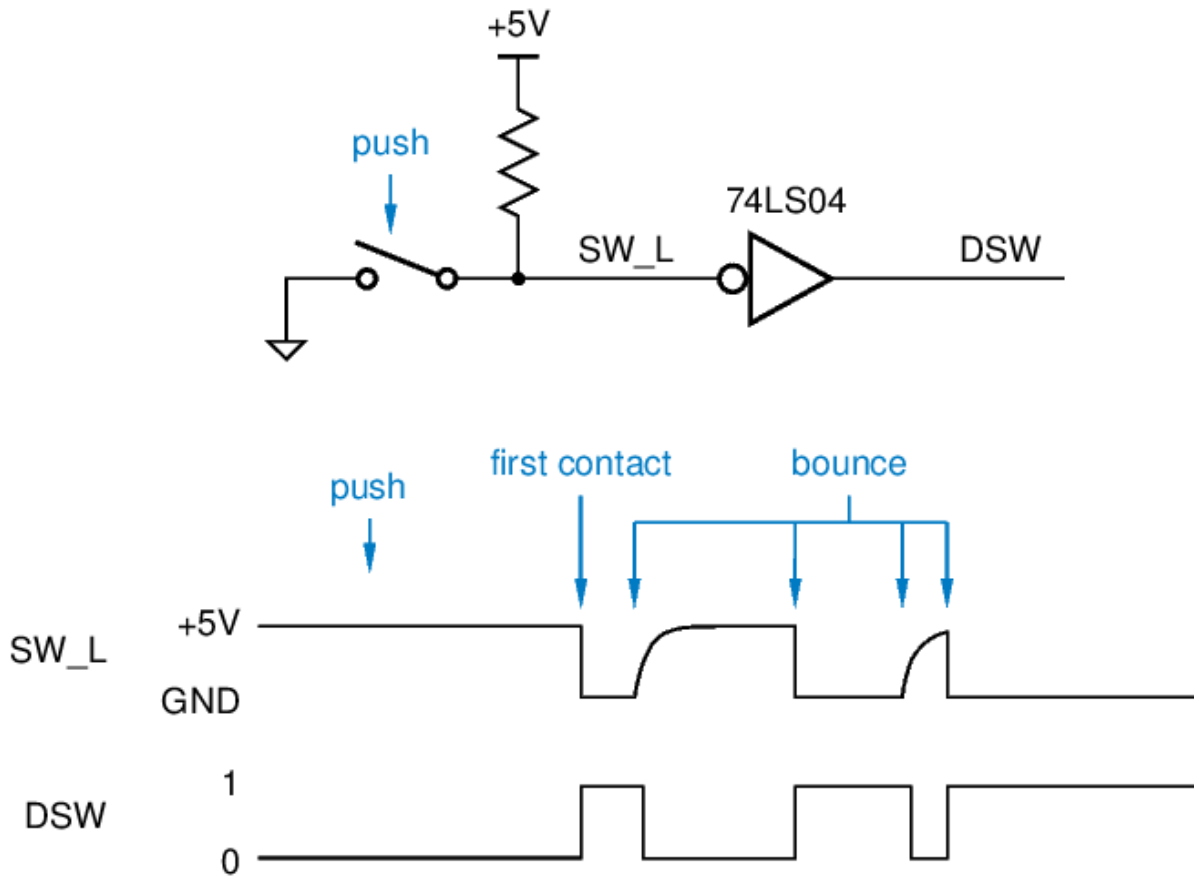
    - DPDT – Single Pole, Double Throw



    - ...
    - 2P6T

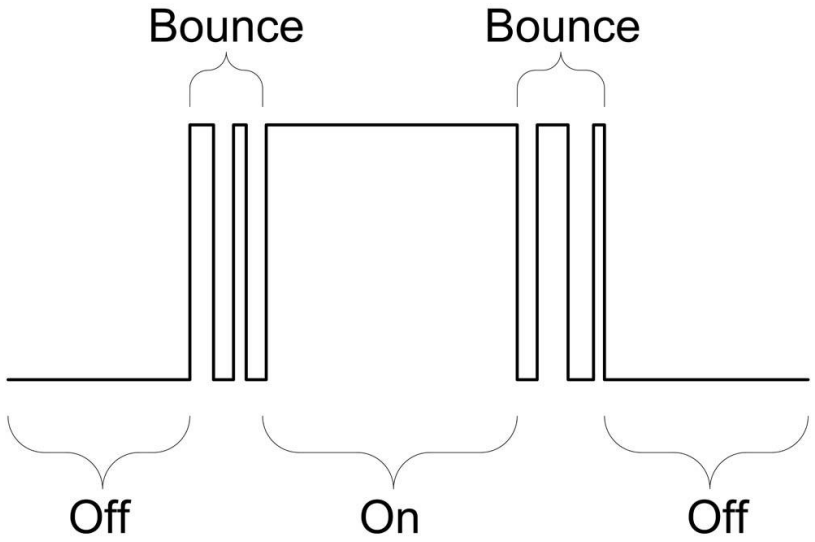


Aspectos analógicos de pinos digitais

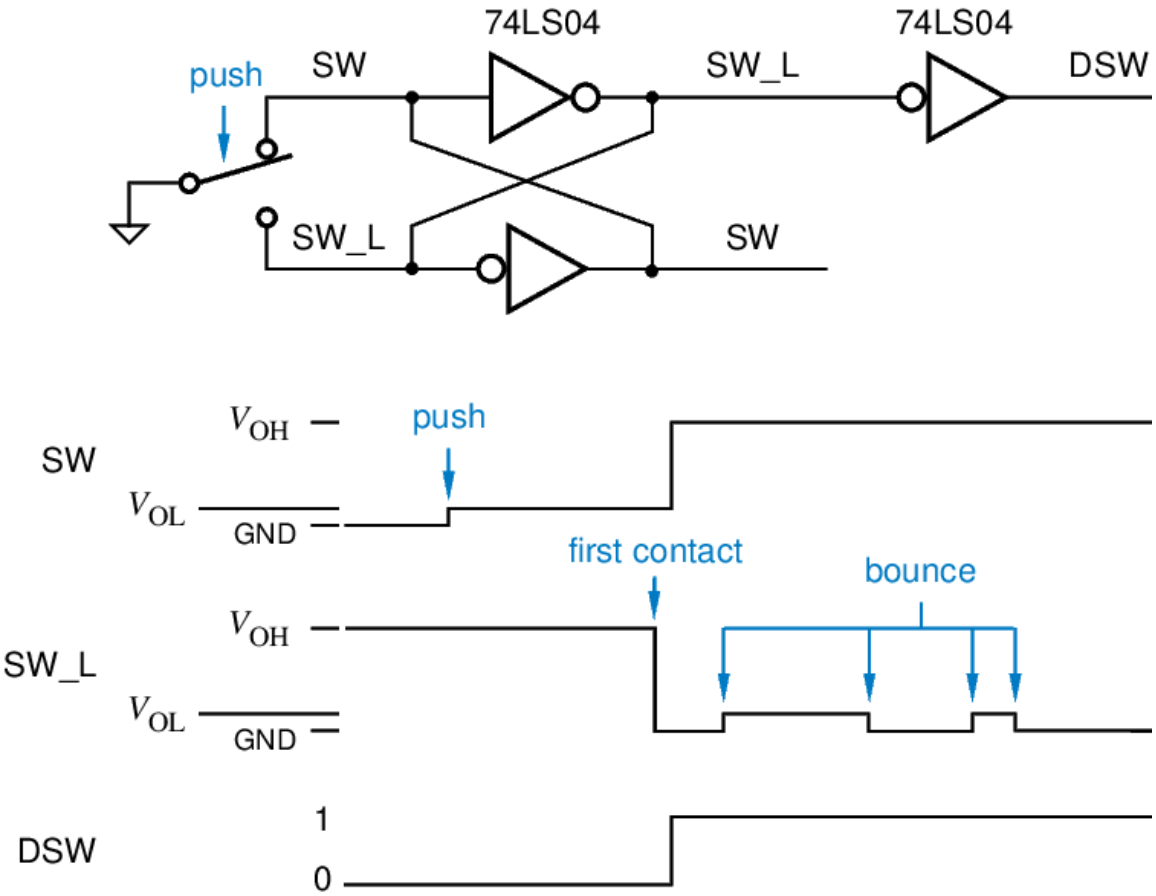


Aspectos analógicos de pinos digitais

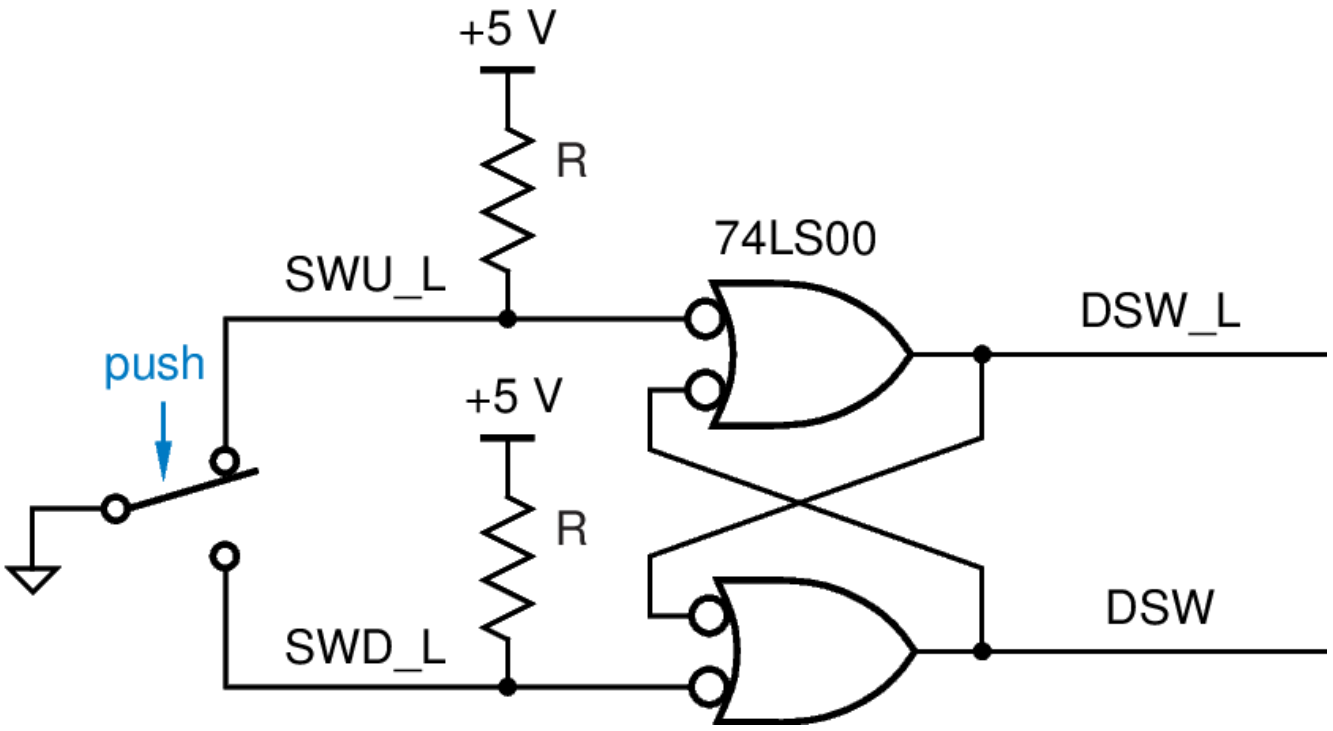
- Debouncing



Aspectos analógicos de pinos digitais

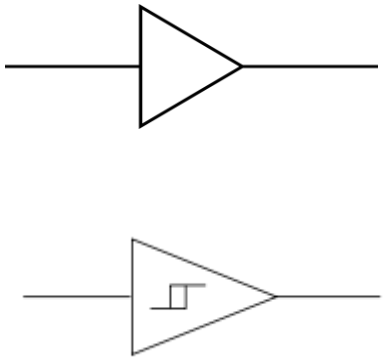


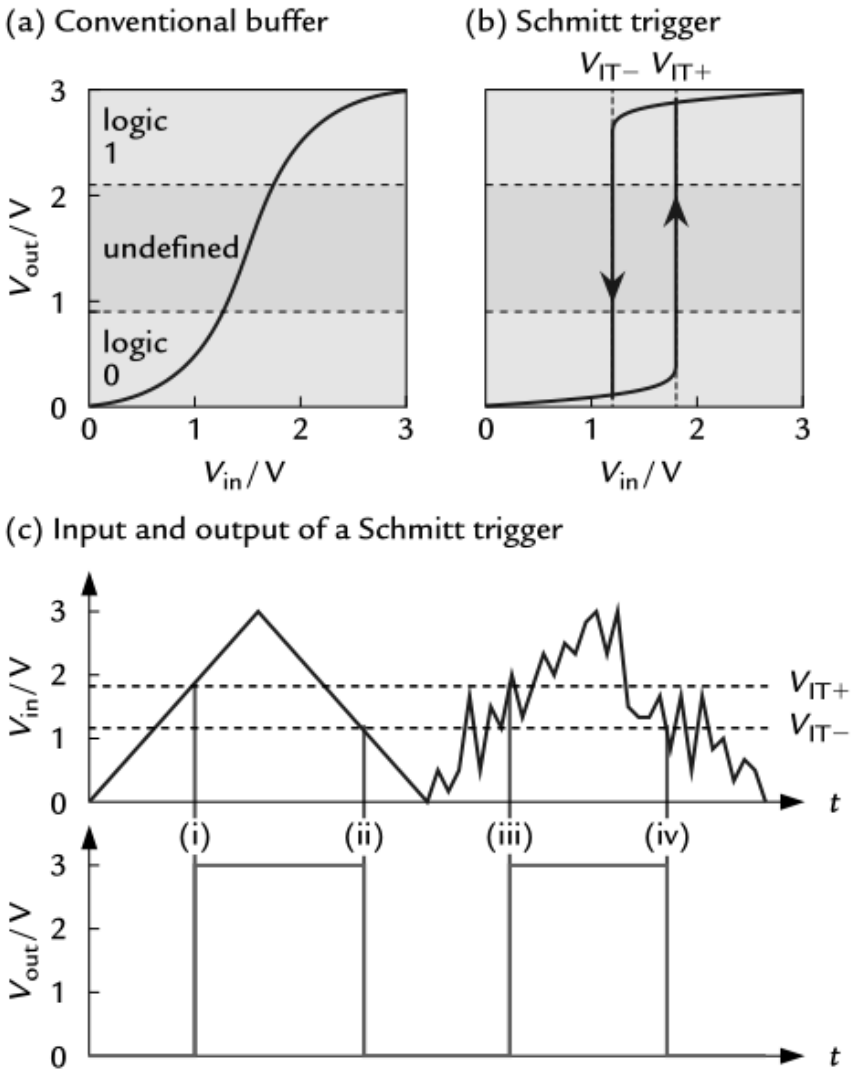
Aspectos analógicos de pinos digitais

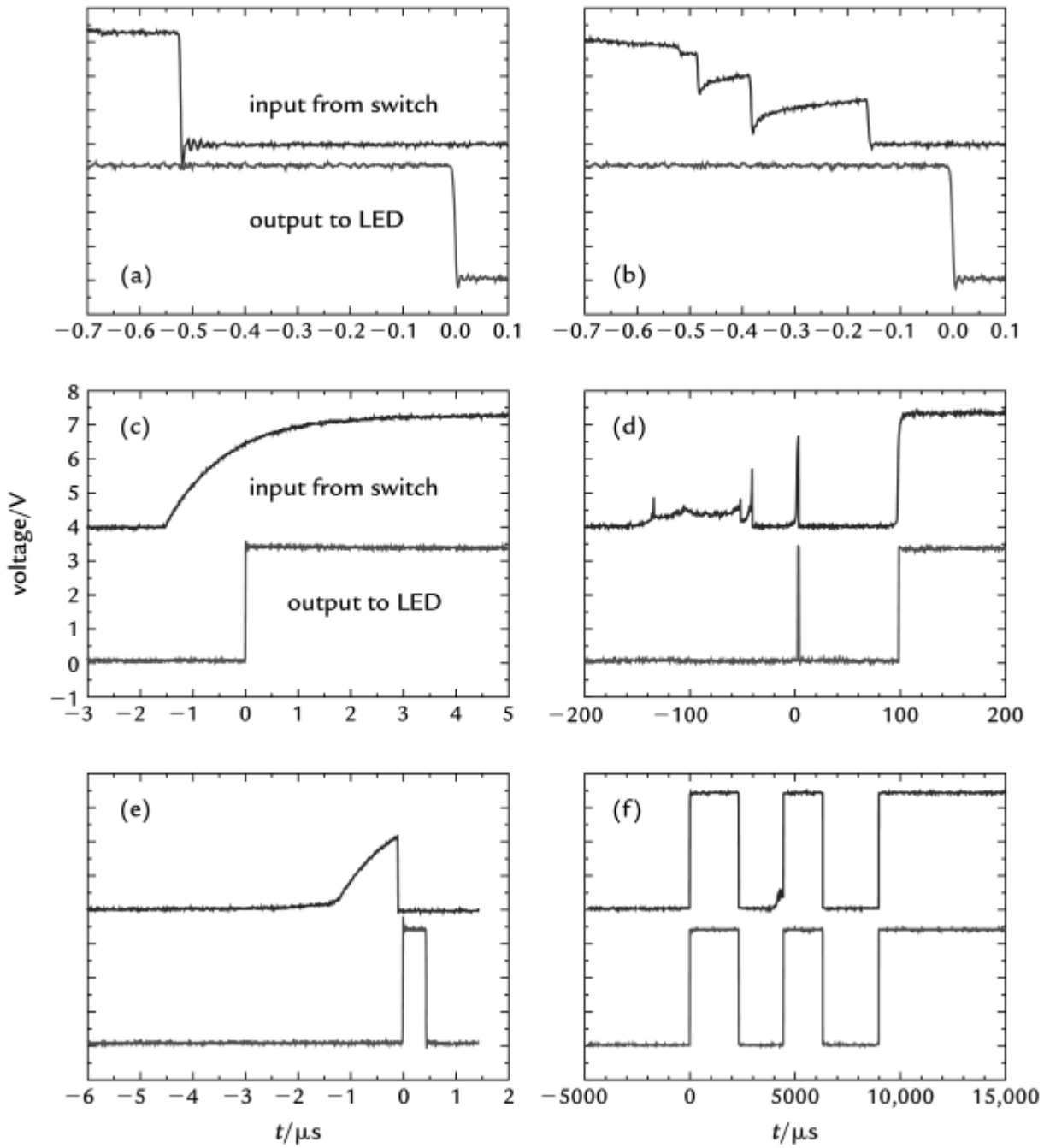


Aspectos analógicos de pinos digitais

- Ruído de entradas digitais.






input from switch
output to LED
(a)
(b)
(c)
(d)
(e)
(f)
voltage/V
t/μs
t/μs