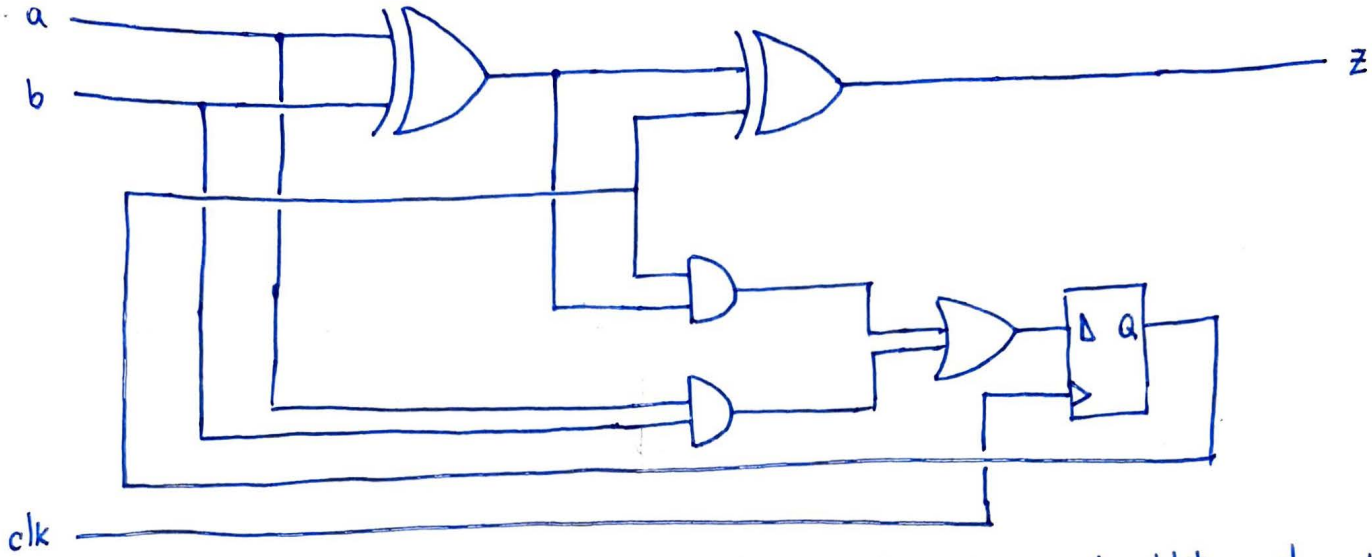
3. (a) A bit-serial adder can be designed as



Notice that the carry from the previous inputs is used in the current addition at each clock cycle.

(b) A bit-serial comparator with inputs a_t and b_t and outputs u_t, v_t and w_t has the following rules:

- $u_t = (a_t > b_t) \vee ((a_t = b_t) \wedge u_{t-1})$
- $v_t = \neg u_t \wedge \neg w_t$ (can't be $(a_t = b_t) \wedge v_{t-1}$, because that would fail on the first clock cycle)
- $w_t = (a_t < b_t) \vee ((a_t = b_t) \wedge w_{t-1})$

Therefore, we'll have the following design: