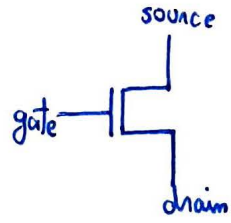
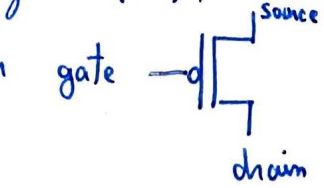
3. [2010/2]

(a) The n-type MOS transistor 

has the following behaviour:

- if the gate is connected to the positive power supply terminal (3.3 V), then the source and the drain are connected together
- if the gate is connected to the ground (0 V), then they are not connected

The p-type MOS transistor 

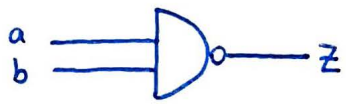
has the following behaviour:

- if the gate is connected to the Vdd, then the source and the drain are not connected
- if the gate is connected to the ground, then they are connected

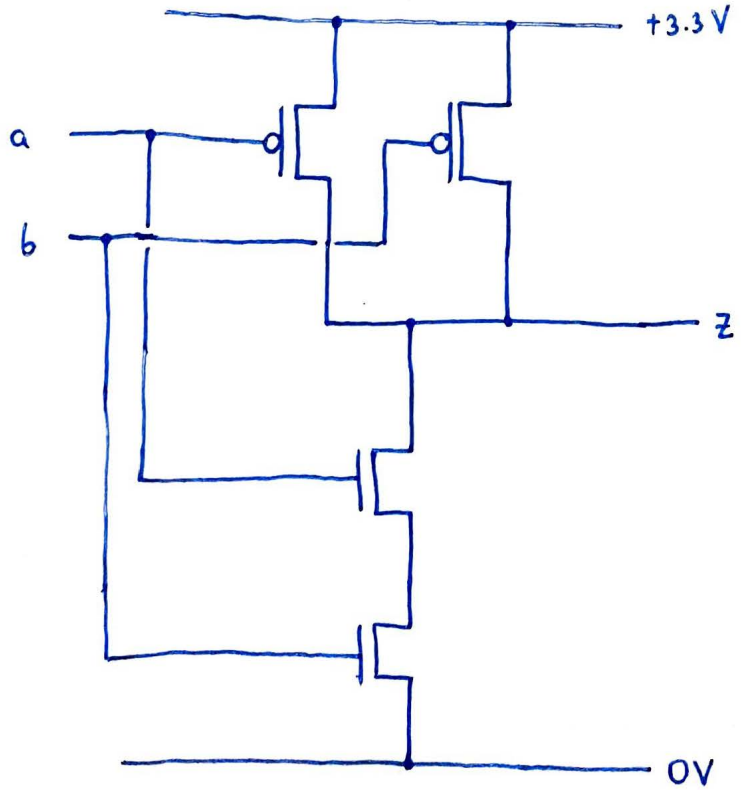
They are both used in designing CMOS (complementary MOS) gate: there is an equal number of n-type and p-type transistors in a CMOS gate, the p-type are in the top half connected to the Vdd and the bottom half are consisting of n-type, which are connected to the ground and they are connected in the middle for the output.

(b) The truth table for NAND is

a	b	z
0	0	1
0	1	1
1	0	1
1	1	0



and can be designed as a CMOS gate as:



When a and b are both 1, the top half is not connected because none of the 2 p-type gates conduct electricity from the Vdd, so z is set to 0 (n-types conduct so it is connected to 0V).

When either a or b (or both) are 0, at least one p-type gate conducts, so z is set to 1 (and the n-types are not conducting as they are connected in series).

(c) $z = \neg((a \wedge b) \vee (c \wedge d))$

This is equivalent to (using $\neg(P \vee Q) = \neg P \wedge \neg Q$)

$z = \neg(a \wedge b) \wedge \neg(c \wedge d)$

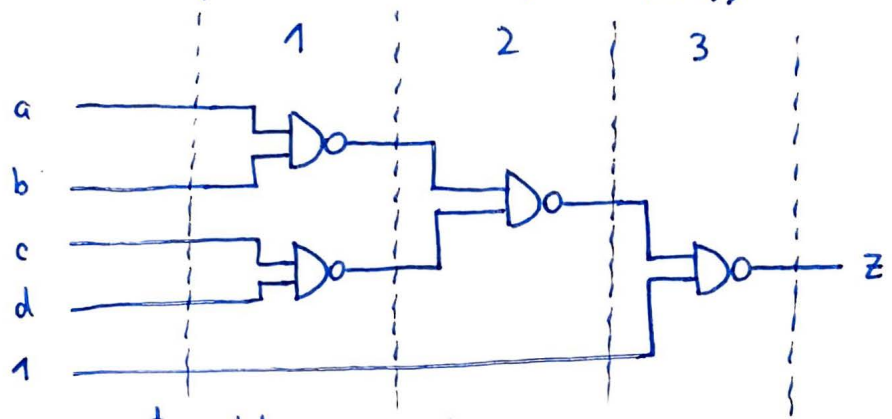
$z = \text{NAND}(a,b) \wedge \text{NAND}(c,d)$

This is equivalent to (using $P \wedge Q = \neg\,\text{NAND}(P,Q)$)

$z = \neg\,\text{NAND}(\text{NAND}(a,b), \text{NAND}(c,d))$

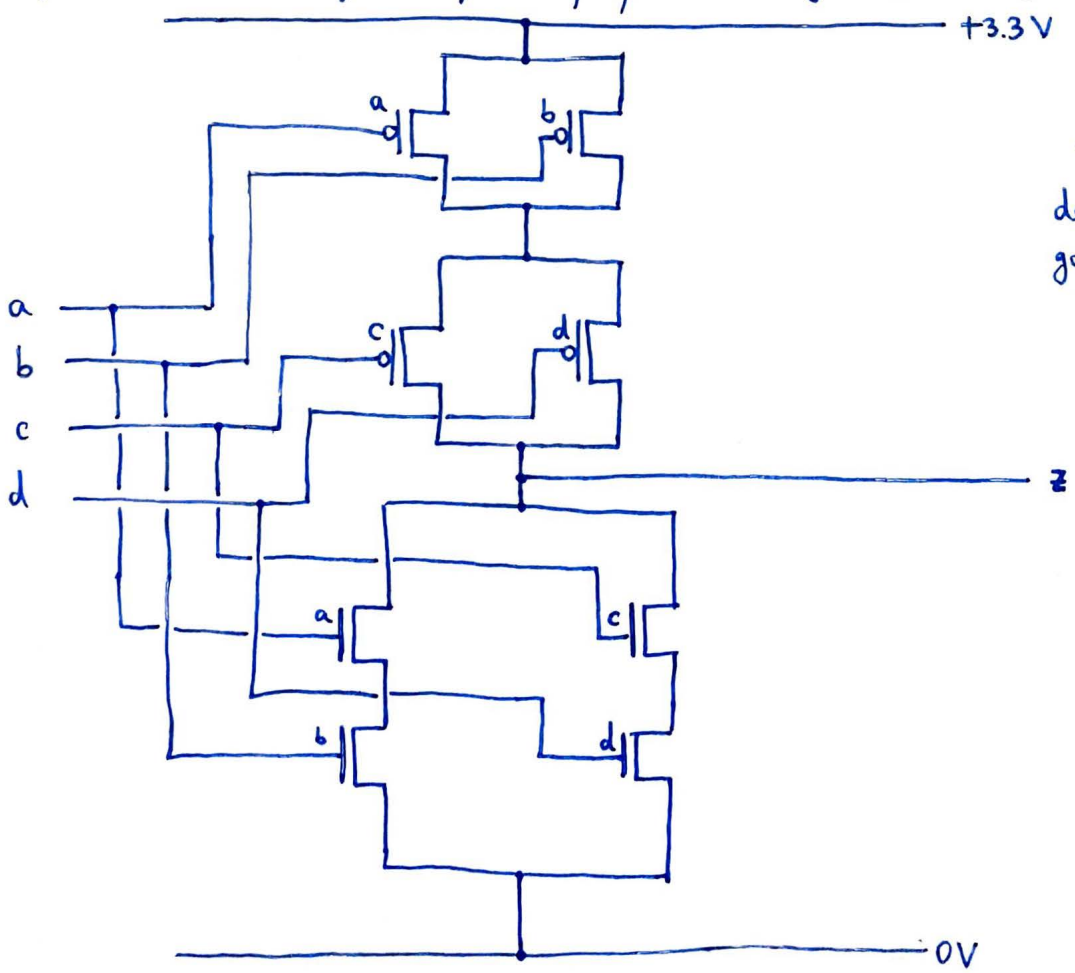
This is equivalent to (using $\neg P = \text{NAND}(P,1)$)

$z = \text{NAND}(1, \text{NAND}(\text{NAND}(a,b), \text{NAND}(c,d)))$



The propagation delay is therefore $3 \cdot 2\,ns = 6\,ns$

(d) Now, we'll design a special-purpose CMOS gate for the function:



This needs 2 propagation delays since the longest path goes to 2 transistors $\Rightarrow$ 4 ns.

4. [2018/1, modified]

If the input at time t is a_t, then the output at time t is $z_t = a_{t-1} \wedge \neg a_{t-2} \wedge a_{t-3} \wedge a_{t-4}$ since we want to recognize the sequence 1101.

The circuit for that is: