

DOCUMENTAÇÃO

Para remover o Hazard, apenas definimos o `stall_s1_s2` sempre para falso, com isso simulamos sua remoção. Por mais que o hazard detecte a situação o pipeline continuará sua execução de forma inalterada.

```
always @(*) begin
    if (memread_s3 == 1'b1 && ((rt == rt_s3) || (rs == rt_s3))) begin
        stall_s1_s2 <= 1'b0; // no stall
    end else
        stall_s1_s2 <= 1'b0; // no stall
    end
```

Para remover o forward também usamos essa mesma técnica. Removemos todas as mudanças que o case fazia e definimos para sempre pegar o valor de `data1_s3` e `data2_s3`, que são os mesmos valores de `data1` e `data2`, com isso, por mais que o forward tenta corrigir o problema, a pipeline se manterá como se estivesse sem essa operação.

Usamos o arquivo “example_addlwsowlbew.txt”.

```
case (forward_a)
    default: fw_data1_s3 = data1_s3;
endcase
```

```
case (forward_b)
    default: fw_data2_s3 = data2_s3;
endcase
```

```
gabriel@User-PC: /mnt/c/Users/User/Documents/GitHub/inf251/MIPSPipeline/2/mips-cpu-master$ iverilog tb.v cpu.v
gabriel@User-PC: /mnt/c/Users/User/Documents/GitHub/inf251/MIPSPipeline/2/mips-cpu-master$ ./a.out
if_pc, if_instr, id_regrs, id_regrt, ex_alua, ex_alub, ex_aluctl, mem_memdata, mem_memread, mem_memwrite, wb_regdat
a, wb_regwrite
VCD info: dumpfile test.vcd opened for output.
PC=00000000 00210820 | |rs= x rt= x rd= x| |A=xxxxxxx B=xxxxxxx| |w=xxxxxxx Ram=xxxxxxx RxWx| |ID=xxxxxxx
b=xxxxxxx j=xxxxxxx| |Opcod=xx Func=xx| |I=xxxxxxx R=xxxxxxx| |D= x alu=xxxxxxx branch0 j0| |R=xx C= 1
PC=00000004 00210820 | |rs= 1 rt= 1 rd= 1| |A=xxxxxxx B=xxxxxxx| |w=xxxxxxx Ram=xxxxxxx RxWx| |ID=xxxxxxx
b=xxxxxxx j=xxxxxxx| |Opcod=00 Func=20| |I=xxxxxxx R=xxxxxxx| |D= x alu=xxxxxxx branch0 j0| |R=xx C= 2
PC=00000008 00210820 | |rs= 1 rt= 1 rd= 1| |A=00000001 B=00000001| |w=xxxxxxx Ram=xxxxxxx R0W0| |ID=xxxxxxx
b=00000000 j=00000000| |Opcod=00 Func=20| |I=00000000 R=00000000| |D= x alu=xxxxxxx branch0 j0| |R=xx C= 3
PC=0000000c 00210820 | |rs= 1 rt= 1 rd= 1| |A=00000001 B=00000001| |w=00000001 Ram=00000000 R0W0| |ID=xxxxxxx
b=00000000 j=00000000| |Opcod=00 Func=20| |I=00000000 R=00000000| |D= 1 alu=00000002 branch0 j0| |R=xx C= 4
PC=00000010 8c010000 | |rs= 1 rt= 1 rd= 1| |A=00000001 B=00000001| |w=00000001 Ram=00000000 R0W0| |ID=00000002
b=00000000 j=00000000| |Opcod=00 Func=20| |I=00000000 R=00000000| |D= 1 alu=00000002 branch0 j0| |R=01 C= 5
PC=00000014 00210820 | |rs= 0 rt= 1 rd= 0| |A=00000002 B=00000002| |w=00000001 Ram=00000000 R0W0| |ID=00000002
b=00000000 j=00000000| |Opcod=23 Func=00| |I=00000000 R=00000000| |D= 1 alu=00000002 branch0 j0| |R=01 C= 6
PC=00000018 ac010000 | |rs= 1 rt= 1 rd= 1| |A=00000000 B=00000000| |w=00000002 Ram=00000004 R0W0| |ID=00000002
b=00000000 j=00000000| |Opcod=00 Func=20| |I=00000000 R=00000000| |D= 1 alu=00000004 branch0 j0| |R=01 C= 7
PC=0000001c 20010001 | |rs= 0 rt= 1 rd= 0| |A=00000002 B=00000002| |w=00000002 Ram=00000000 R1W0| |ID=00000004
b=00000000 j=00000000| |Opcod=2b Func=00| |I=00000000 R=00000000| |D= 1 alu=00000000 branch0 j0| |R=01 C= 8
PC=00000020 01e1102a | |rs= 0 rt= 1 rd= 0| |A=00000000 B=00000000| |w=00000002 Ram=00000004 R0W0| |ID=00000000
b=00000000 j=00000000| |Opcod=08 Func=01| |I=00000000 R=00000000| |D= 1 alu=00000004 branch0 j0| |R=01 C= 9
PC=00000024 00210820 | |rs=15 rt= 1 rd= 2| |A=00000000 B=00000001| |w=00000004 Ram=00000004 R0W1| |ID=00000004
b=00000000 j=00000000| |Opcod=00 Func=2a| |I=00000001 R=00000001| |D= 0 alu=00000000 branch0 j0| |R=01 C=10
PC=00000028 1040fffd | |rs= 1 rt= 1 rd= 1| |A=0000000f B=00000004| |w=00000000 Ram=00000004 R0W0| |ID=00000000
b=00000000 j=00000000| |Opcod=00 Func=20| |I=0000102a R=00000000| |D= 1 alu=00000001 branch0 j0| |R=00 C=11
gabriel@User-PC: /mnt/c/Users/User/Documents/GitHub/inf251/MIPSPipeline/2/mips-cpu-master$
```