UNIVERSIDADE FEDERAL DO PARÁ
INSTITUTO DE TECNOLOGIA
FACULDADE DE ENGENHARIA DA COMPUTAÇÃO E TELECOMUNICAÇÕES

Estudo e Implementação de Técnicas para Sincronismo em Sistemas de Telecomunicações

Gabriel Peixoto de Carvalho

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Trabalho de Conclusão de Curso apresentado para obtenção do grau de Engenheiro em Engenharia da Computação, do Instituto de Tecnologia, da Faculdade de Engenharia da Computação e Telecomunicações.

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Este trabalho foi julgado adequado em __/__/____ para a obtenção do Grau de Engenheiro da Computação, aprovado em sua forma final pela banca examinadora que atribuiu o conceito ____________.

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Viva como se você fosse morrer amanhã. Aprenda como se você fosse viver para sempre.

Mahatma Gandhi

Lista de Siglas

1. ADSL - *Linha de assinante digital assimétrica*

Lista de Símbolos

b	Taxa agregada de bits alcançável para o sistema

Lista de Figuras

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Abstract

Capítulo 1

Introdução

Capítulo 2

Carrier Recovery

Carrier recovery is a processes used in coherent demodulation where the phase and the frequency of the transmitter carrier wave are recovered by the receiver and thus after having such information it is possible to extract the information in the transmitted signal.
Considering that the phase and frequency of the transmitted wave probably will be affected by noise, it is not a straight-forward method, it includes filtering and usually feedback systems to correct the erros in phase or frequency caused by the noise.
This chapter aims in the brief exploration of some techniques used for carrier recovering, such as Phase locked loops, costas loop and others.

2.1 Phase-Locked Loop (PLL)

Phase-locked Loop is a kind of feedback system, which has been extensively used in communications sytems and other applications which require frequency synthesis.
The Phase-Locked Loop is composed by three basic components 2.1:

1. A phase detector (PD).

2. A loop filter.

3. A voltage-controlled oscillator (VCO).

As it can be seen in the figure 2.1 the phase-locked loop is a feedback system whose main goal is to make the output signal the same as the input signal. Basically the phase detector compares the phase of the input signal against the phase of the VCO output, then the PD output is inputed in the loop filter whose output is the voltage that controls the VCO. The output of the phase detector is the phase error between the input signal and the VCO and the output of the loop filter outputs the control voltage to the VCO.

When the loop is locked, theoretically, the output frequency is the same as the input frequency, but to maintain the control voltage necessary to lock it is needed a nonzero output to the phase detector, thus the pll operates with some phase error, but this tends to be small.

Pll makes simple to syntetize frequencies with a pll and do operations of analog modulation and demodulation, these applications willbe briefly discussed later.

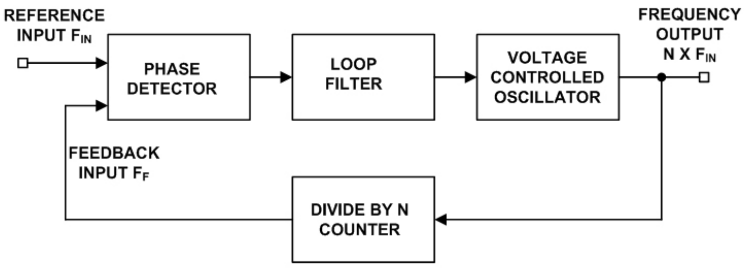

Figura 2.1: Basic PLL scheme

2.1.1 PLL Fundamentals

Considering a basic pll scheme as shown in figure 2.2 we can see that the input signal has a pahse of $\theta_i(t)$ and the VCO output has a phase of $\theta_o(t)$. Assuming that the loop is locked and the phase detector is linear, the ouput of the PD is proportional to the phase difference between its inputs, thus,

$$v_d = K_d(\theta_i - theta_o) \tag{2.1}$$

where k_d is the PD gain factor and its unity is volt/radian.

The v_d is filtered by the loop filter, supressing noise and high frequency signal components, the filter also contributes for the determination of the dynamic performance of the loop. The filter transfer function is given by $F(s)$.

Frequency output of the VCO is determined by the input v_c and since frequency is the derivative of the phase, the operation in the VCO can be described by,

$$L[\frac{d\theta_o(t)}{dt}] = s\theta_o(s) = K_o V_c(s) \tag{2.2}$$

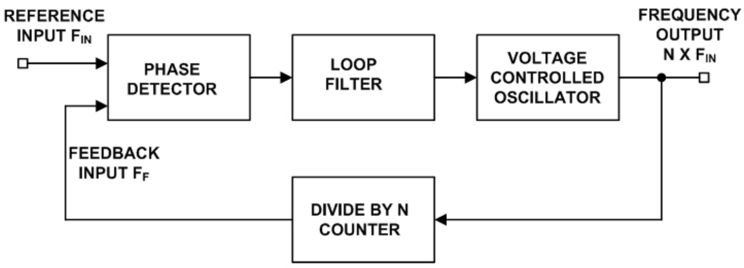

Figura 2.2: PLL

we can see that the output of the VCO is linearly related to the integral of the control voltage.

Using laplace notation it is possible to stablish some basic equations to describe the loop components behavior,

$$V_d(s) = K_d[\theta_i(s) - \theta_o(s)] \tag{2.3}$$

$$V_c(s) = F(s)V_d(s) \tag{2.4}$$

$$\theta_o(s) = \frac{k_o V_c(s)}{s} \tag{2.5}$$

The combination of these equations 2.3, 2.4, 2.5 results in the basic loop equations:

$$H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_o K_d F(s)}{s + K_o K_d F(s)} \tag{2.6}$$

$$\frac{\theta_i(s) - \theta_o(s)}{\theta_i(s)} = \frac{\theta_e(s)}{\theta_i(s)} = \frac{s}{s + K_o K_d F(s)} = 1 - H(s) \tag{2.7}$$

$$V_c(s) = \frac{sK_d F(s)\theta_i(s)}{s + K_o K_d F(s)} = \frac{s\theta_i(s)}{K_o} H(s) \tag{2.8}$$

Where:

- $H(s)$ is the closed-loop transfer function

- θ_e is the phase error

There is indeed another point to explore, regarding loop gain, the open-loop transfer function (open-loop gain) of any PLL is,

$$G(s) = \frac{K_o K_d F(s)}{s} \tag{2.9}$$

thus the closed-loop transfer function can be made in terms of 2.9,

$$H(s) = \frac{G(s)}{1 + G(s)} \tag{2.10}$$

The DC gain can be defined as,

$$K_v = K_o K_d F(0) \tag{2.11}$$

which has dimensions of frequency ($time^-1$). A high K_v value is related to a good performance of the loop. $F(s)$ is a rational function of the loop filter in the form

$$F(s) = \frac{g(s - z_1)(s - Z_2)\dots(s - z_m)}{(s - p_1)(s - p_2)(s - p_3)\dots(s - p_n - 1)} \tag{2.12}$$

For the filter to be realizable m cannot exceed n-1, and if m=n-1 as often occurs in PLL designs, then $g = F(\infty)$.

Expandign $F(s)$ in aprtial fractions it is possible to rewrite the open-loop gain function as

$$G(s) = \frac{K}{s}\left[a_1 + \sum_{i=1}^{n-1} \frac{a_i + 1}{s - p_i}\right] \tag{2.13}$$

where K is the $loopgain$ and a_1 is zero if $m < n - 1$, while $a_1 = 1$ if $m = n - 1$, but K is only "defined"when $a_1 = 1$, thus the most important PLLs are designed for $a_1 = 1$ (equal number of poles and zeroes in the loop filter).

Based on the previous equations which describe the behavior of the components in the phase-locked loop we can classify the pll based on the order of the transfer function associated with the loop. This classification is based upon the nunmber of perfect integrators ($\frac{1}{s}$) present in the transfer function.

- First order loop.

- Second order loop.
- Third and higher order loop.

2.1.1.1 First Order Loop

The first order loop is the simplest implementation of a phase-locked loop, where the loop filter is ommited, thus $F(s) = 1$

$$H(s) = \frac{K_o K_d}{s + K_o K_d} = \frac{K}{s + K} \tag{2.14}$$

Where:

- $K = K_o K_d = K_v$;

In the first-order loop the only parameter avaible to the designer is the loop gain

2.1.1.2 Second Order Loop

In the second order loop the loop filter is used and it is possible to separate it in two major "classes", the loop which use passive filters and the loops whose use active filters. The loops which use passivel filters require high-gain DC amplifier but provides good tracking performance, the closed-loop transfer function for a passive filter is

$$H_1(s) = \frac{K_o K_d (s\tau_2 + 1)/\tau_1}{s^2 + s(1 + K_o K_d \tau_2)/\tau_1 + K_o K_d/\tau_1} \tag{2.15}$$

and for rthe active filter the closed-loop trasnfer function is

$$H_2(s) = \frac{K_o K_d (s\tau_2 + 1)/\tau_1}{s^2 + s(1 + K_o K_d \tau_2)/\tau_1 + K_o K_d/\tau_1} \tag{2.16}$$

witha very large amplifier gain 2.15 and **??** can be rewritten as

$$H_1(s) = \frac{s(2\zeta\omega_n - \omega_n^2/K_o K_d) + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.17}$$

$$H_1(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.18}$$

where ω_n is the natural frequency of the loop and ζ is the damping factor.

The second-order loops are the most prevalent used loop but depending on the application another loop orders are required.

2.1.1.3 Third an Higher Order Loops

2.1.1.4 Analysis Tools

2.1.2 PLL Components

2.1.3 Analogic PLL Tracking

2.1.4 Modulation and Demodulation using PLL

2.1.5 Discrete-time PLL

2.1.6 Design of PLL and DPLL

2.1.7 Costas Loop

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