UNIVERSIDADE FEDERAL DO PARÁ
INSTITUTO DE TECNOLOGIA
FACULDADE DE ENGENHARIA DA COMPUTAÇÃO E TELECOMUNICAÇÕES

An FPGA-Based Radion Frontend for LTE Transmission on Cloud RAN

Gabriel Peixoto de Carvalho

BELÉM - PARÁ

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Trabalho de Conclusão de Curso apresentado para obtenção do grau de Engenheiro em Engenharia da Computação, do Instituto de Tecnologia, da Faculdade de Engenharia da Computação e Telecomunicações.

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Este trabalho foi julgado adequado em __/__/____ para a obtenção do Grau de Engenheiro da Computação, aprovado em sua forma final pela banca examinadora que atribuiu o conceito _____.

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Gabriel Peixoto de Carvalho

Viva como se você fosse morrer amanhã. Aprenda como se você fosse viver para sempre.

Mahatma Gandhi

Lista de Siglas

1. ADSL - *Linha de assinante digital assimétrica*
2. MIMO - *Multiple Input Multiple Output*
3. BBP - *Baseband Processor*
4. RF - *Radio Frequency*
5. LTE - *Long Term Evolution*
6. C-RAN - *Cloud-RAN or Centralized-RAN*
7. RAN - *Radio Access Network*
8. LVDS - *Low Voltage Differential Signalling*
9. FDD - *Frequency Division Duplex*
10. TDD - *Time Division Duplex*
11. AGC - *Automatic Gain Control*
12. PLL - *Phase Locked Loop*
13. BTS - *Base Station*
14. DCXO - *Digital Controlled Crystal Oscillator*
15. LO - *Local Oscillator*
16. BB - *Baseband*
17. ADC - *Analog-to-Digital Converter*
18. DAC - *Digital-to-Analog Converter*

19. RSSI - *Receive Signal Strength Indication*
20. FIR - *Finite Impulse Response*
21. IIR - *Infinite Impulse Response*
22. SNR - *Signal to Noise Rate*
23. FMC - *FPGA Mezzanine Card*
24. LPC - *Low PIn Count*
25. HPC - *High Pin Count*
26. UE - *User Equipment*
27. SMA - *Subminiature Version A*
28. FPGA - *Field Programmable Gate Array*
29. ASIC - *Application Specific Integrated Circuit*
30. SDR - *Software Defined Radio*
31. RAN - *Radio Access Network*
32. RAN - *Radio Access Network*

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b	Taxa agregada de bits alcançável para o sistema

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Abstract

The evolution of mobile services in terms of access technologies and application layers is driving a huge change in mobile communication systems. A recent hot topic in the field is the rise of the cloud computing paradigm, thus the idea known as cloud radio access networks (Cloud-RAN) is growing in the industry. This behavior comes from the potential of cloudification for improvement in the efficiency of resource allocation, manageability and power consumption, aspects inherent of traditional RANs.

Thus, with the emerging of C-RAN, several questions about how to implement and which tools to use come naturally. This work aims to evaluate the potential of a programmable fronthaul radio interface, as known, actual network does not have the adaptative capability needed for the C-RAN. For this work a setup of a radio unit, composed by two fpgas (one acting as the Baseband unit and other as the (digital front-end) of the radio unity) connected through ethernet and two transceivers (analog front-end), one in each FPGA. Within this setup various algorithms can be tested and can be evaluated in LTE scenarios because the transceiver works in LTE and C-RAN .

This work shall focus on the evaluation of the radio interface and perform the tests inherent to it, exploring FPGA adaptability and parallelism with the internal and external communication protocols, and so exploring the advantages of the transceiver used, the fmcomms2 development board (AD9361 chip) from Analog devices, which is a device broadly used in software defined radio hardwares, as known as USRPs (Universal Software Radio Peripheral).

An aspect of the transceiver that is very attractive to the C-RAN paradigm is its configurability and scalability, capable of real-time adjustments in the sampling frequency or operation mode from 2x2 to 4x4 MIMO (Multiple Inputs and Multiple Outputs), this real-time adaptive

characteristic is ideal to C-RAN environment.

The results are generated primarily aiming a fidelity in the transmitted and receiver signals, after these results are conclusive it is possible to proceed to more complex tests and approaches of this setup. Another test made was the analysis of the synchronization between receiver and transceiver using a CIPRI emulator implemented in FPGA logic, which is the standard fronthaul interface, in this test it is possible to observe the advantages of the programmable radio front-end in the system.

Parte I

Introduction

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Introdução

Parte II

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Synchornization

2.1 Carrier Recovery

Carrier recovery is a processes used in coherent demodulation where the phase and the frequency of the transmitter carrier wave are recovered by the receiver and thus after having such information it is possible to extract the information in the transmitted signal.
Considering that the phase and frequency of the transmitted wave probably will be affected by noise, it is not a straight-forward method, it includes filtering and usually feedback systems to correct the erros in phase or frequency caused by the noise.
This chapter aims in the brief exploration of some techniques used for carrier recovering, such as Phase locked loops, costas loop and others.

2.1.1 Costas Loop

Parte III

Implementation

Capítulo 3

FMComms2

3.1 AD9361

The AD9361 is a high performance RF transceiver. Its programmability and adaptability makes it ideal for a wide range of transceiver applications. This device combines a RF front end with a flexible and configurable mixed-signal baseband section and frequency synthesizers, simplified configuration digital interface to a processor. The AD9361 operates from 70 MHz to 6.0GHz range with supported channel bandwidths from 200 KHz to 56 MHz and the AD9361 is a 2 Rx and 2 Tx device packed in a 10mm x10mm, 144 ball chip package ball grid array (CSP_BGA).

3.1.1 General Description

AD9361 is a highly integrated RF frequency transceiver capable of being configured for a wide range of applications, including 3g and 4g frequency applications. AD9361 and AD9364 almost the same hardware and specifications, the difference is that AD9361 is a 2x2 MIMO and AD9364 is a 1x1 [**?**]. The programmability allows the AD9361 to be operated in Frequency Division Duplex (FDD) and Time Division Duplex (TDD) systems, allowing this transceiver to operate in a variety of communication standards. Another interesting feature is the capability of integration with a wide range of BBPs (Baseband Processors) using a single or dual 12-bit parallel data port or a 12-bit LVDS (Low voltage Differential signaling), which uses the FMC connector in the FMCommS2 **??**. AD9361 also provides self-calibration and automatic gain control (AGC) systems to maintain good performance under variable conditions, such as temperature and signal quality. The transceiver has also various modes of test mode with the

Built-in Self Test (BIST) modes which can be used for the designers to debug desgs during prototyping. This configurability and adaptability is very attractive for Software Defined Radio (SDR) and for C-RAN systems, indeed ad9361 is already being used in some Universal Software Radio Peripheral (USRP) from ettus research (National Instruments), this alone is a proof that AD9361 can work in a wide range of systems and standards.

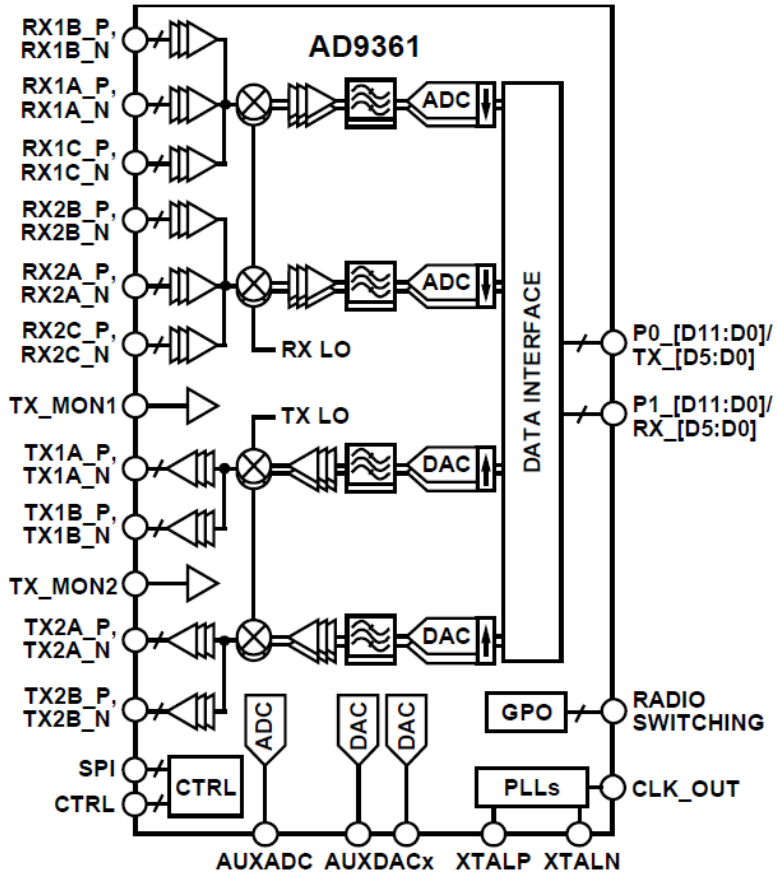

Figura 3.1: AD9361 Functional Block Diagram

3.1.2 Receiver

The receiver section has all the blocks necessary to receive analog RF signals and convert them to digital data which can be used by the BBP. there are two independently controlled channels that share same frequency synthesizer. This characteristic makes possible to the AD9361 to operate in MIMO systems.

Each channel has 3 inputs which can be multiplexed into the signal chain, making possible to use the AD9361 into systems with multiple antenna inputs. The Receiver is a direct

conversion system that contains a Low noise amplifier (LNA) , followed by a matched in-phase and quadrature amplifier, mixers, and band shaping filters that down convert received signals to baseband for digitization. External LNAs can also be interfaced to the AD9361 allowing more flexibility in the design. The receiver signal path passes downconverted signals (I and Q), which are schematically identical to each other, to the baseband (BB) receiver section. The BB section is composed by two programmable low-pass filters, with programmable corner frequency for each filter, 12-bit ADC and four stages of decimating filters, each of the four decimation filters can be bypassed. The gain control is achieved by a preprogrammed gain index map, a lookup table for example, this map distributes gain in order to achieve optimal performance at each level. This optimal behavior can be achieved by enabling AGC, which can run in two modes, fast and slow gain control. This allow for the BBP to make gain adjustments as needed. Each channel also contains independent RSSI measurement capability, DC offset tracking and all other circuitry needed for self-calibration.

The receiver ADC is a 12-bit sigma-delta ($\Sigma - \Delta$) ADC which allows adjustable sample rates. This ADC produces data streams from the received signals and such digitalized signals can be conditioned further by a series of decimation filters and a 128-tap FIR filter with additional decimation settings. The sampling rate of each digital filter is adjustable through changes in the decimation factors to produce the needed data rate.

In short, the Receiver chain has:

- LNA - Low noise Amplifier
- Matched in-phase amplifier;
- Quadrature Amplifier;
- Band Shaping Filters;
- Analog low pass filters;
- 12-bit DAC;
- 4 stages of decimation filters (128-tap FIR filters);
- Automatic gain Control;

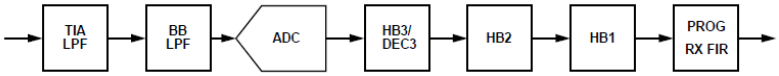

Figura 3.2: Receiver Signal Path

3.1.3 Transmitter

Like the receiver section, the transmitter section contains two identical and independently controller channels, which share the same frequency synthesizer, that provide all digital signal processing, mixed signal and RF blocks necessary to implement a direct conversion system from digital data to RF. The Tx signal path receives from the BBP 12-bit 2s complement I-Q format data in the digital interface and each channel goes through a 128-tap FIR filter with interpolation options, which is fully programmable. Then the signal goes through a series of additional interpolation filters that manipulates the signal with additional filtering and data rate interpolation before reaching the 12-bit DAC, note that all these filtering and interpolation steps can be bypassed if desired. Each 12-bit DAC has an adjustable sampling rate and its analog output passes through to low pass filters to remove any sampling artifacts before going to the RF mixer, these low pass filters corner frequencies can be programmable too. After all these filtering and analog conversion steps, the I and Q signals are recombined and modulated in the carrier frequency, which can be adjusted by changing the synthesizer frequency. These analog combined signals passes through additional analog filters for better band shaping and then it can be transmitted to the output amplifier. Each Transmitting channel provides wide attenuation adjustment range with fine granularity in order to optimize SNR.

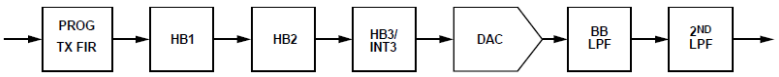

Figura 3.3: Transmitter Signal Path

Identical to the receiver chain, the transmitter chain has also built-in self-calibration circuitry into each transmitting channel providing an automatic real-time adjustment. The transmitter also provides a TX monitor block for each channel, this block monitors the transmission output and routes it back through an unused receiver channel to the BBP for signal monitoring, but these monitoring option is only available in TDD mode operation while the receiver is idle.

In short the transmission chain has:

- 128-tap FIR filters;
- Interpolation Filters;
- 12-bit DAC;
- Analog Low-pass Filters;
- Additional band shaping analog filters;
- Attenuation adjustment;
- self-calibration circuits;
- Tx signal Monitor.

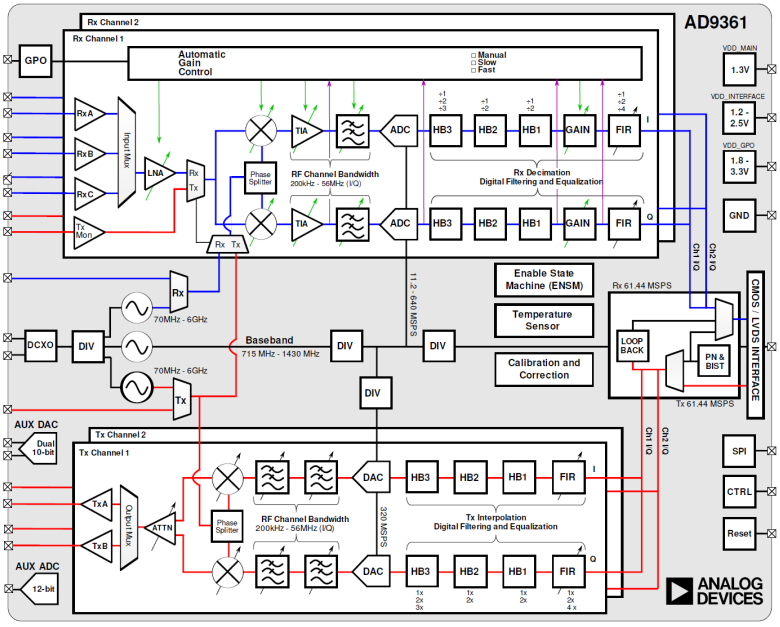

Figura 3.4: AD9361 Block Diagram

3.1.4 Filtering

In both receiver and transmitter there are:

Receiver

- Low pass filter : band shape to reduce adjacent-channel interference.

- Decimation Filter: up convert from the digital baseband rate (64.11MSPS max) to the actual ADC (640MSPS) rate.

Transmitter

- Low pass filter : remove sampling artifacts
- Interpolation Filter : down convert from the digital baseband rate (64.11MSPS max) to the actual DAC (320MSPS) rate.

In both digital and analog implementations these filters have impact the magnitude and the phase in passband, such behavior must be compensated in the system, and this compensation is usually done inside the 128-tap FIR filter. The FIR filter is not only used for low pass filter realization but also to compensate for magnitude and phase impacts created by the analog and digital half band filters in the desired baseband area.

These filters depend in various other systems to work properly, such systems are sample rates, clock, data rates which sets the half band filters, and the desired RF bandwidth, which sets the analog filters. the process of loading a filter and after changing anything in the system will negatively affect the overall baseband performance.

There is a filter too created by analog devices,which designs a low-pass filter and sets the FIR coefficients in order to ensure compensation for magnitude and phase changes in the analog or half band filters.

3.1.5 Clocking

The AD9361 has a series of internal PLL to generate and manipulate clock signals. There are fractional-n PLLs that generate the transmitter and receiver LO frequencies and there are the baseband PLL (BBPLL) used for the data converters, digital filters and I/O ports. All the frequency signals are generated using these PLLs clock outputs.

All the PLLs require a reference clock input and for this there is the digitally controlled oscillator (DXCO) function, which is an in-chip programmable and variable capacitor, such capacitor can tune the crystal frequency variance before entering the system, having a precision of +/- 6 ppm it results in a more accurate reference clock and can be used, if needed, for synchronization purposes. this function can also be used together with the on-chip temperature

sensor to provide temperature compensation depending enviroment in which the chip will be used. For the reference clock there are two options:

External Oscillator

In this option and external clock signal can be connected in the XTALP pin (Leaving the XTALP pin unconnected), this external clock frequency may vary from 10 MHz to 80 MHz. Such type of setup is needed when a wireless basestation (BTS) reference clock is locked to a master clock, and in such systems there is no or less need for clock synchronization.

Dedicated Crystal

In this option a dedicated crystal, with frequency varying from 19 MHz to 50 MHz, is connected in the XTALP and XTALN pins. This setup is usually used in wireless user equipment (UE), which do not need to be locked to a master clock but they do need to adjust periodically the LO frequency in order to maintain a connection with a BTS. The BTS periodically informs the UE of its frequency error relative to the BTS and the BBP can make adjustments to the reference clock and thus adjust the LO frequency if needed.

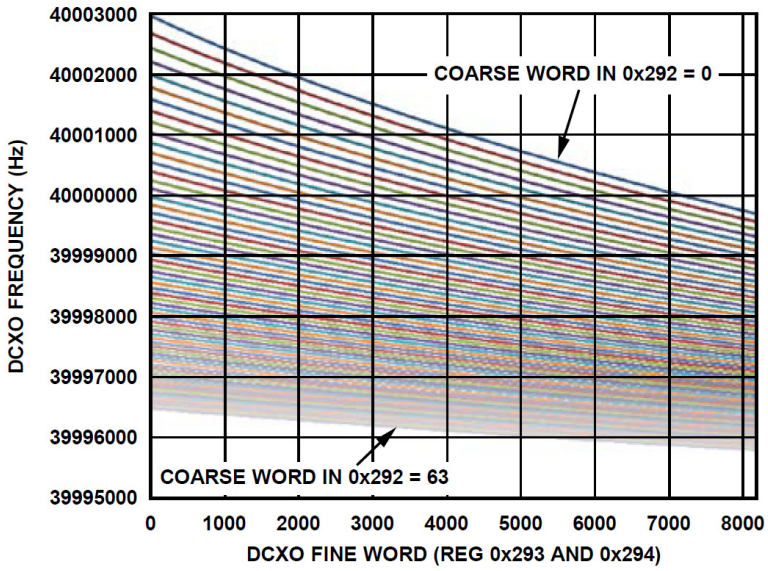

Figura 3.5: DCXO Behavior Graph

3.1.6 Synthesizers

RF PLLs

The AD9361 contains two identical synthesizers to generate the required LO signals for the RF signal path, one for the receiver and one for the transmitter. The PLL synthesizers are fractional-n PLLs with completely integrated VCOs and loop filters, requiring no other external components. In TDD operation mode, the synthesizers turn ON and OFF appropriate for the TX and RX frames, however in FDD TX PLL and RX PLL are activated at the same time.

BB PLL

The AD9361 contains also a baseband PLL synthesizer, which generate all the baseband related clock signals. The BBPLL feeds all the baseband related clock signals to ADC, DAC (Sampling Clock), DATA_CLK signal and all data framing signals. This PLL has a frequency range from 700 Mhz to 1400 Mhz, and can be changed based on system requirements.

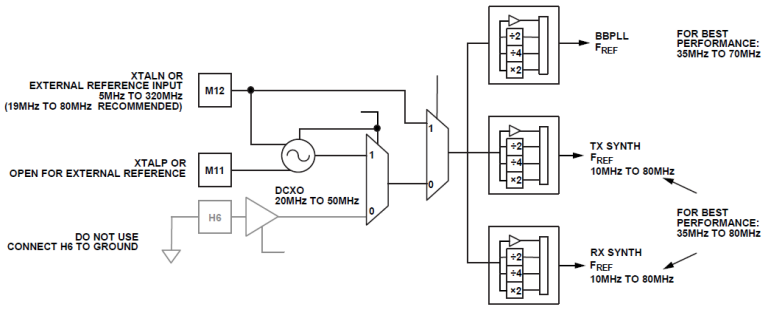

Figura 3.6: AD9361 PLL Reference Block Diagram

3.1.7 Digital Data Interface

The AD9361 uses parallel data ports to transfer data between the device and the BBP. These data ports can be configured either single-ended CMOS format or LVDS format (used in this work). Both formats can be configured in multiple arrangements to adequate the system requirements for data transfer and connections. These arrangements can be of single port data bus, dual port data bus, single data rate, double data rate and other various combinations compatible with the device.

Bus transfers are controlled using hardware handshake signalling, these two ports can be operated in TDD (bidirectional) or FDD (full duplex) where half of the bits are used for transmitting and the other half is used for receiving. The interface can also be configured to use only one of the data ports (usually used in applications that do not require high data rates or samples).
The communication between the BBP processor and the AD9361 rely on some signals to properly work, which are DATA_CLK, FB_CLK and RX_FRAME, its operation is detailed below:

DATA_CLK Signal

RX sends the signal DATA_CLK to the BBP, which can be used when receiving data. DATA_CLK can be used to control data sampling time, which can be single data rate (data is captured on rising clock edge) or double data rate (data is captured on both rising and falling clock edges). This can be applied using single or dual data port.

FB_CLK Signal

The FB_CLK signal must have the same frequency and duty cycle as DATA_CLK and like DATA_CLK it is used as timing reference for the interface. FB_CLK allows source synchronous with rising edge capture for burst control signals and can be used like DATA_CLK for rising edge, single data rate mode or in both edge capture, double data rate mode for transmit signal bursts.

RF_FRAME Signal

The RF_FRAME signal is generated by the device whenever the receiver outputs valid data. RF_FRAME has two modes:

- **Level Mode:** RF_FRAME stays high as long as the data is valid.
- **Pulse Mode:** RF_FRAME pulses with 30

The BBP must provide a TX_FRAME that indicates beginning of a valid data transmission with a rising edge. The TX_FRAME operates similarly as the RF_FRAME, on Level Mode or Pulse Mode.

3.1.8 Enable State Machine

The AD9361 has an Enable State Machine (ENSM) which allows real-time control over the current state of the device. The device can be place in several states like:

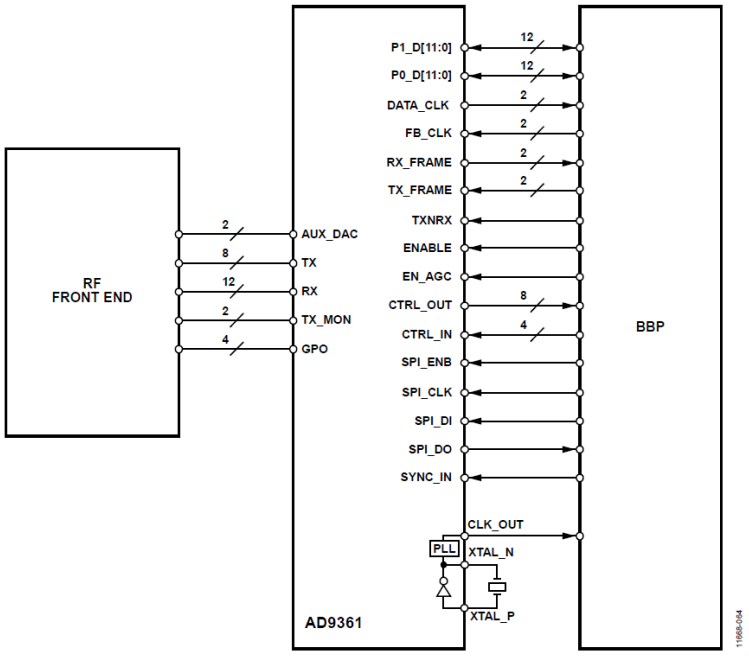

Figura 3.7: AD9361 Digital Data Interface

- **Wait:** Power save, synthesizers disabled.
- **Sleep:** Wait with all clocks and BBPLLs disabled.
- **TX:** TX chain enabled.
- **RX:** RX chain enabled.
- **FDD:**TX and RX chains enabled.
- **Alert:** Synthesizers enabled.

This ENSM can be controlled either by SPI or PIN (GPIO for example), where the SPI control mode is for a non real-time operation and the PIN control mode is for a much faster and real-time control.

SPI Control Mode

In SPI control mode, the BBP writes registers asynchronously by using SPI protocol to access the addresses, and by writing these registers the state machine advances the current state to the next state. SPI communication is considerece asynchronous to the DATA_CLK because the SPI_CLK can be derived from another clock source, where BBP

and the device does not share the same clock source. This control method is recommended when there is no need for a real-time control.

Pin Control Mode

In Pin control mode, there are pins dedicated to activate some states of the ENSM, like ENABLE pin and TXNRX pin, this mode allows a real-time control of the current state. This method is recommended in a system where the BBIC has extra pins to spare with the real-time control outputs, this 2-wire interface can control the state of the device. To advance the current state to the next state of the ENSM, the enable function of the ENABLE pin can be driven by either pulse or level,if the pulse is used the minimum width of the pulse needs to be equal as the FB_CLK cycle. In FDD mode, the ENABLE and TXNRX pins can be remapped to be used as real-time control of the TX and RX data transfers. In this mode ENABLE enables or disables the receive signal and TXNRX enables or disables the transmit signal, using such mode causes the ENSM to be removed from the system for data flow control and is replaced by these pins.

3.1.9 SPI Interface

The AD9361 uses a SPI interface for communication with the BBP. Throught SPI is possible to access all the device registers. The PSI interface can be configured as a 4-wire interface with dedicated transmit and receive pins, duplex, or as 3-wire interface with bidirectional data port. Write commands have a 24-bit format where the first six bits are for setting the bus direction and number of bytes to transfer, the next 10 bits set the address where the data is to be written and the final eight bits are the data to be transferred to the specific register address (MSB to LSB), a LSB-first format is also supported. Read commands follow a similar format, the difference is that the first 16 bits are transferred on the SPI_DI pin and the final eight are read from the AD9361, either using SPI_DO (4-wire interface) or SPI_DI (3-wire interface).

3.1.10 Auxiliary Converters

AUXADC

The AD(361 contains an auxiliary ADC that can be used to monitor some system functions such as temperature or power output, it is a 12-bit converter and has an input range of 0V to 1.25V. The SPI can read the last value latched at the output of the ADC when it is

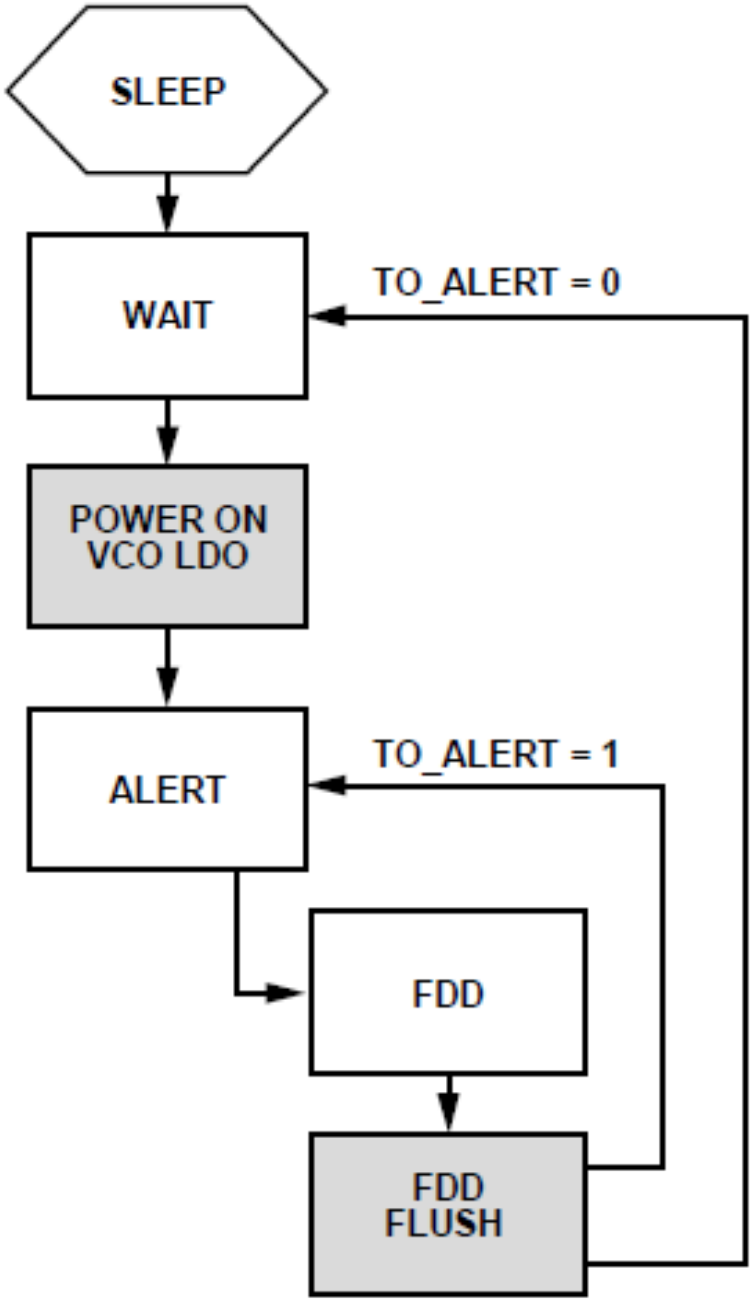

Figura 3.8: FDD Enable State Machine

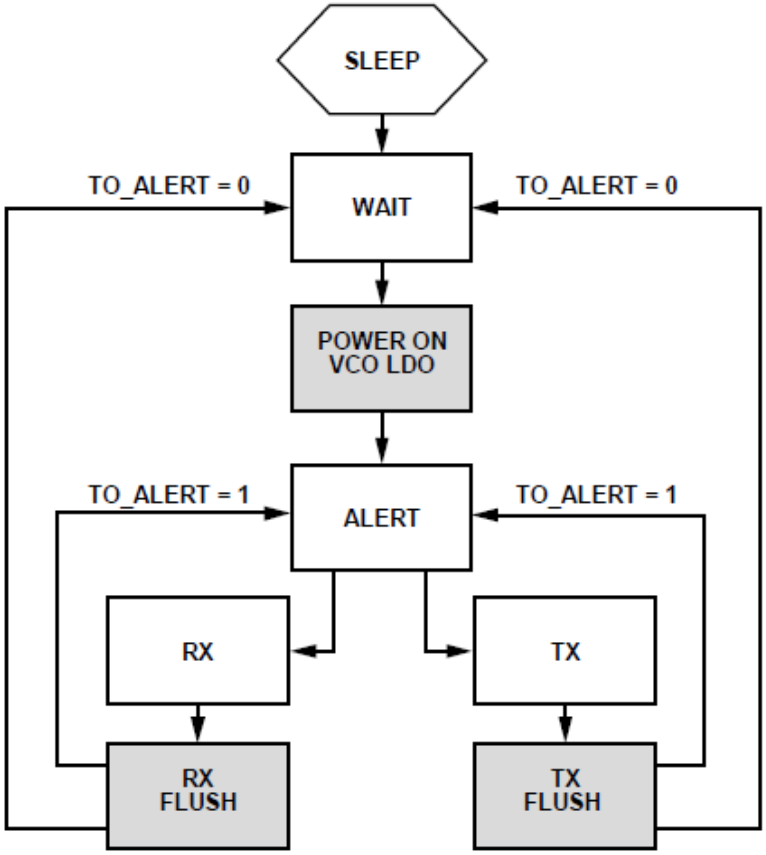

Figura 3.9: TDD Enable State Machine

enabled for use, there is also a multiplexer that permits to select between AUXADC and built-in temperature sensor.

AUXDAC1 and AUXDAC2

The AD(361 also has two identical auxiliary DACs which can be used to provide power amplifier (PA) bias or other system functionality. Both the DACs are 10-bit wide and have an output range of 0.5 V to 0.3V and have a current drive of 10mA. The DACs can be directly controlled by the ENSM.

3.1.11 Applications

3.2 FMCommS2

FMCommS2 is basically evaluation board for the AD9361 that has a FPGA Mezzanine Card (FMC) connector for interfacing with the BBP (Usually FPGA). The FMComms2 has 5 SMA connectors, 2 for Rx, 2 for Tx and one for external reference clock input. The FMComms2 provides a 2x2 RF configuration, extended from the AD9361, and has a narrow tuning range balun, which is performance optimized for 2.4GHz. The FMComms2 is a transceiver intended for use in RF applications such 3G or 4G BTS or SDR. Its programmability and wideband capability make it ideal for broad range of transceiver applications and make it very attractive for the new C-RAN paradigm.

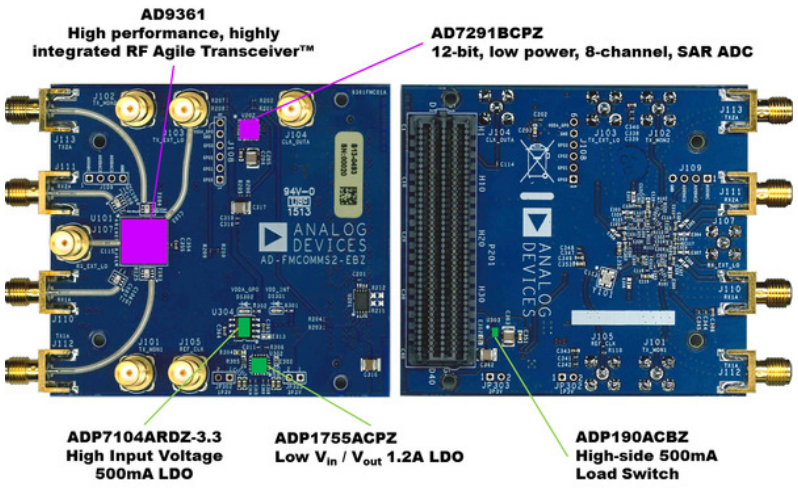

Figura 3.10: FMComms2 and its components

3.2.1 Functional Overview

The Block diagram show that there are 4 main functional partitions - receiver path, transmit path, clocking and power supply. Since the FMComms2 incorporates and extends the basic functionalities of the AD9361, thus the data path is fully integrated into the AD9361.

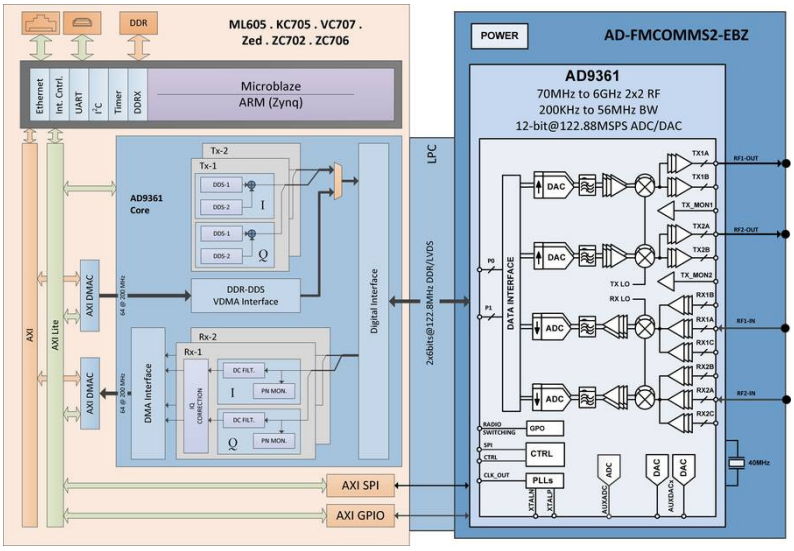

Figura 3.11: FMComms2 and FPGA Block Diagram

Receive

- Support up to 2 direct conversion RF receiver channels.
- Fully integrated frequency synthesizers (including loop filter).
- Data path consists in LNA, Demodulator, LPF, ADC and digital filters.
- *AGC:* quadrature calibration and DC offset calibration.
- *NF:* 2.5 dB at 1Ghz.
- *ADC:* Continuous time sigma-delta ($\Sigma - \Delta$), 640 MSPS.
- *Digital FIlter:* 128 COmplex taps with decimation between 2 and 48.
- *Gain:* 1dB step size, 80 dB analog Range, 30 db digital range (post ADC scaling).
- On-chip sensor for temperature corrected RSSI.

Transmit

- Supports up to 2 direct conversion RF transmit channels.
- Fully integrated frequency synthesizers (including loop filter).
- Data path consists of digital filters, DAC and modulators.
- *Digital FIlter:* 128 complex taps with interpolation between 2 and 48.
- *Gain:* 0.5 dB step size, 86 dB range.
- *ADC:* 340 MSPS.

Clocking

The FMComms2 board has a integrated crystal oscillator of 40 Mhz and has a SMA input for external clock input.

Control/Monitor

The board allows real time control and monitoring via dedicated pins, such pins functionality are programmable. The control and monitor programming configuration is specified in the ad9361 section [**?**].

3.3 Basic Mathematical Background

3.3.1 Complex Modulation

$$I = sin(\omega \times t) \tag{3.1}$$

$$Q = cos(\omega \times t) \tag{3.2}$$

$$cos(\omega \times t) = sin(\frac{\pi}{2} - (\omega \times t)) \tag{3.3}$$

then:

$$I = sin(\omega \times t) \tag{3.4}$$

$$Q = sin(\frac{\pi}{2} - (\omega \times t)) \tag{3.5}$$

These are the two signals coming out of the DAC, two sine waves, phase offset from each other, wich is called IQ.

3.3.2 Basic Modulation Mathematics

Start to modulating signal from a amplitude perspective:

$$LO_I = A_x cos(k) \tag{3.6}$$

$$LO_Q = B_x sin(k) \tag{3.7}$$

We still have the carrier:

$$LO_I = cos(\omega); LO_Q = sin(\omega) \tag{3.8}$$

Will result:

$$LO_I \times I = A_x cos(k) \times sin(\omega) \tag{3.9}$$

$$LO_Q \times I = B_x sin(k) \times cos(\omega) \tag{3.10}$$

That gives the output:

$$x(t) = A_x cos(k) \times sin(\omega) + B_x sin(k) \times cos(\omega) \tag{3.11}$$

This does not match with any trigonometrical identities and it is easier to use Eulerś formula:

$$sin(x) = (\frac{1}{2}e^{-jx} - \frac{1}{2}e^{jx}) \tag{3.12}$$

$$cos(x) = (\frac{1}{2}e^{-jx} + \frac{1}{2}e^{jx}) \tag{3.13}$$

Therefore:

$$x(t) = A_x(\frac{1}{2}e^{-jk} + \frac{1}{2}e^{jk}) \times (\frac{1}{2}e^{-j\omega} - \frac{1}{2}e^{j\omega}) + B_x(\frac{1}{2}e^{-jk} - \frac{1}{2}e^{jk}) \times (\frac{1}{2}e^{-j\omega} + \frac{1}{2}e^{j\omega}) \tag{3.14}$$

$$x(t) = \frac{A}{2}(e^{-jk} + e^{jk}) \times (e^{-j\omega} - e^{j\omega}) + \frac{B}{2}(e^{-jk} - e^{jk}) \times (e^{-j\omega} + e^{j\omega}) \tag{3.15}$$

If we expand we get:

$$x(t) = \frac{1}{2}((Ae^{-jk-j\omega}+Ae^{jk-j\omega}-Ae^{-jk+j\omega}-Ae^{jk+j\omega})+(Be^{-jk-j\omega}-Be^{jk-j\omega}-Be^{-jk+j\omega}+Be^{jk+j\omega})) \tag{3.16}$$

And then:

$$x(t) = \frac{1}{2}((A+B)e^{-jk-j\omega} + (A-B)e^{jk-j\omega} - (A-B)e^{-jk+j\omega} - (A+B)e^{jk+j\omega}) \tag{3.17}$$

It is possible to rearrange as:

$$x(t) = \frac{1}{2} \times ((A+B)(e^{-jk-j\omega} - e^{jk+j\omega}) + (A-B)(e^{jk-j\omega} - e^{-jk+j\omega})) \tag{3.18}$$

And then:

$$x(t) = (\frac{A+B}{2})(sin(k+\omega)) + (\frac{A-B}{2})(sin(k-\omega)) \tag{3.19}$$

If this due to amplitude mismatch, this creates an image on the other side of the local oscillator.

Capítulo 4

FPGA

4.1 ML605 - Virtex6

4.2 VC707 - Virtex7

Capítulo 5

Setup Description

5.1 Overview

5.2 Integration between FPGA and FMComms2

Parte IV

Final Results

Capítulo 6

Results

6.1 Preliminary Tests

6.2 Transmission Tests

Parte V

Conclusion and Future Work

Capítulo 7

Conclusion

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Apêndice A

PLL

Apêndice B

FPGA Design Flow

Apêndice C

PLL