Table 1-47. GPIOA MUX

	Default at Reset Primary I/O Function	Peripheral Selection	Peripheral Selection 2	Peripheral Selection 3
GPAMUX1 Register Bits	**(GPAMUX1 bits = 00)**	**(GPAMUX1 bits = 01)**	**(GPAMUX1 bits = 10)**	**(GPAMUX1 bits = 11)**
1-0	GPIO0	EPWM1A (O)	Reserved[1]	Reserved[1]
3-2	GPIO1	EPWM1B (O)	ECAP6 (I/O)	MFSRB (I/O)[1]
5-4	GPIO2	EPWM2A (O)	Reserved[1]	Reserved[1]
7-6	GPIO3	EPWM2B (O)	ECAP5 (I/O)	MCLKRB (I/O)[1]
9-8	GPIO4	EPWM3A (O)	Reserved[1]	Reserved[1]
11-10	GPIO5	EPWM3B (O)	MFSRA (I/O)	ECAP1 (I/O)
13-12	GPIO6	EPWM4A (O)	EPWMSYNCI (I)	EPWMSYNCO (O)
15-14	GPIO7	EPWM4B (O)	MCLKRA (I/O)	ECAP2 (I/O)
17-16	GPIO8	EPWM5A (O)	CANTXB (O)	$\overline{\text{ADCSOCAO}}$ (O)
19-18	GPIO9	EPWM5B (O)	SCITXDB (O)	ECAP3 (I/O)
21-20	GPIO10	EPWM6A (O)	CANRXB (I)	$\overline{\text{ADCSOCBO}}$ (O)
23-22	GPIO11	EPWM6B (O)	SCIRXDB (I)	ECAP4 (I/O)
25-24	GPIO12	$\overline{\text{TZ1}}$ (I)	CANTXB (O)	MDXB (O)
27-26	GPIO13	$\overline{\text{TZ2}}$ (I)	CANRXB (I)	MDRB (I)
29-28	GPIO14	$\overline{\text{TZ3}}$/$\overline{\text{XHOLD}}$ (I)	SCITXDB (O)	MCLKXB (I/O)
31-30	GPIO15	$\overline{\text{TZ4}}$/$\overline{\text{XHOLDA}}$ (O)	SCIRXDB (I)	MFSXB (I/O)
GPAMUX2 Register Bits	**(GPAMUX2 bits = 00)**	**(GPAMUX2 bits = 01)**	**(GPAMUX2 bits = 10)**	**(GPAMUX2 bits = 11)**
1-0	GPIO16	SPISIMOA (I/O)	CANTXB (O)	$\overline{\text{TZ5}}$ (I)
3-2	GPIO17	SPISOMIA (I/O)	CANRXB (I)	$\overline{\text{TZ6}}$ (I)
5-4	GPIO18	SPICLKA (I/O)	SCITXDB (O)	CANRXA (I)
7-6	GPIO19	$\overline{\text{SPISTEA}}$ (I/O)	SCIRXDB (I)	CANTXA (O)
9-8	GPIO20	EQEP1A (I)	MDXA (O)	CANTXB (O)
11-10	GPIO21	EQEP1B (I)	MDRA (I)	CANRXB (I)
13-12	GPIO22	EQEP1S (I/O)	MCLKXA (I/O)	SCITXDB (O)
15-14	GPIO23	EQEP1I (I/O)	MFSXA (I/O)	SCIRXDB (I)
17-16	GPIO24	ECAP1 (I/O)	EQEP2A (I)	MDXB (O)
19-18	GPIO25	ECAP2 (I/O)	EQEP2B (I)	MDRB (I)
21-20	GPIO26	ECAP3 (I/O)	EQEP2I (I/O)	MCLKXB (I/O)
23-22	GPIO27	ECAP4 (I/O)	EQEP2S (I/O)	MFSXB (I/O)
25-24	GPIO28	SCIRXDA (I)	$\overline{\text{XZCS6}}$ (O)	$\overline{\text{XZCS6}}$ (O)
27-26	GPIO29	SCITXDA (O)	XA19 (O)	XA19 (O)
29-28	GPIO30	CANRXA (I)	XA18 (O)	XA18 (O)
31-30	GPIO31	CANTXA (O)	XA17 (O)	XA17 (O)

(1) The word "Reserved" means that there is no peripheral assigned to this GPxMUX1/2 register setting. Should it be selected, the state of the pin will be undefined and the pin may be driven. This selection is a reserved configuration for future expansion.

Table 1-48. GPIOB MUX

	Default at Reset Primary I/O Function	Peripheral Selection 1	Peripheral Selection 2	Peripheral Selection 3
GPBMUX1 Register Bits	**(GPBMUX1 bits = 00)**	**(GPBMUX1 bits = 01)**	**(GPBMUX1 bits = 10)**	**(GPBMUX1 bits = 11)**
1,0	GPIO32 (I/O)	SDAA (I/OC)	EPWMSYNCI (I)	ADCSOCAO (O)
3,2	GPIO33 (I/O)	SCLA (I/OC)	EPWMSYNCO (O)	ADCSOCBO (O)
5,4	GPIO34 (I/O)	ECAP1 (I/O)	XREADY (I)	XREADY (I)
7,6	GPIO35 (I/O)	SCITXDA (O)	XR/W (O)	XR/W (O)
9,8	GPIO36 (I/O)	SCIRXDA (I)	XZCS0 (O)	XZCS0 (O)
11,10	GPIO37 (I/O)	ECAP2 (I/O)	XZCS7 (O)	XZCS7 (O)
13,12	GPIO38 (I/O)	Reserved	XWE0 (O)	XWE0 (O)
15,14	GPIO39 (I/O)	Reserved	XA16 (O)	XA16 (O)
17,16	GPIO40 (I/O)	Reserved	XA0/XWE1 (O)	XA0/XWE1 (O)
19,18	GPIO41 (I/O)	Reserved	XA1 (O)	XA1 (O)
21,20	GPIO42 (I/O)	Reserved	XA2 (O)	XA2 (O)
23,22	GPIO43 (I/O)	Reserved	XA3 (O)	XA3 (O)
25,24	GPIO44 (I/O)	Reserved	XA4 (O)	XA4 (O)
27,26	GPIO45 (I/O)	Reserved	XA5 (O)	XA5 (O)
29,28	GPIO46 (I/O)	Reserved	XA6 (O)	XA6 (O)
31,30	GPIO47 (I/O)	Reserved	XA7 (O)	XA7 (O)
GPBMUX2 Register Bits	**(GPBMUX2 bits = 00)**	**(GPBMUX2 bits = 01)**	**(GPBMUX2 bits = 10 or 11)**	
1,0	GPIO48 (I/O)	ECAP5 (I/O)	XD31 (I/O)	
3,2	GPIO49 (I/O)	ECAP6 (I/O)	XD30 (I/O)	
5,4	GPIO50 (I/O)	EQEP1A (I)	XD29 (I/O)	
7,6	GPIO51 (I/O)	EQEP1B (I)	XD28 (I/O)	
9,8	GPIO52 (I/O)	EQEP1S (I/O)	XD27 (I/O)	
11,10	GPIO53 (I/O)	EQEP1I (I/O)	XD26 (I/O)	
13,12	GPIO54 (I/O)	SPISIMOA (I/O)	XD25 (I/O)	
15,14	GPIO55 (I/O)	SPISOMIA (I/O)	XD24 (I/O)	
17,16	GPIO56 (I/O)	SPICLKA (I/O)	XD23 (I/O)	
19,18	GPIO57 (I/O)	SPISTEA (I/O)	XD22 (I/O)	
21,20	GPIO58 (I/O)	MCLKRA (I/O)	XD21 (I/O)	
23,22	GPIO59 (I/O)	MFSRA (I/O)	XD20 (I/O)	
25,24	GPIO60 (I/O)	MCLKRB (I/O)	XD19 (I/O)	
27,26	GPIO61 (I/O)	MFSRB (I/O)	XD18 (I/O)	
29,28	GPIO62 (I/O)	SCIRXDC (I)	XD17 (I/O)	
31,30	GPIO63 (I/O)	SCITXDC (O)	XD16 (I/O)	

Table 1-49. GPIOC MUX

	Default at Reset Primary I/O Function	Peripheral Selection 2 or 3
GPCMUX1 Register Bits	**(GPCMUX1 bits = 00 or 01)**	**(GPCMUX1 bits = 10 or 11)**
1,0	GPIO64 (I/O)	XD15 (I/O)
3,2	GPIO65 (I/O)	XD14 (I/O)
5,4	GPIO66 (I/O)	XD13 (I/O)
7,6	GPIO67 (I/O)	XD12 (I/O)
9,8	GPIO68 (I/O)	XD11 (I/O)
11,10	GPIO69 (I/O)	XD10 (I/O)
13,12	GPIO70 (I/O)	XD9 (I/O)
15,14	GPIO71 (I/O)	XD8 (I/O)
17,16	GPIO72 (I/O)	XD7 (I/O)
19,18	GPIO73 (I/O)	XD6 (I/O)
21,20	GPIO74 (I/O)	XD5 (I/O)
23,22	GPIO75 (I/O)	XD4 (I/O)
25,24	GPIO76 (I/O)	XD3 (I/O)
27,26	GPIO77 (I/O)	XD2 (I/O)
29,28	GPIO78 (I/O)	XD1 (I/O)
31,30	GPIO79 (I/O)	XD0 (I/O)
GPCMUX2 Register Bits	**GPCMUX2 bits = 00 or 01**	**GPCMUX2 bits = 10 or 11**
1,0	GPIO80 (I/O)	XA8 (O)
3,2	GPIO81 (I/O)	XA9 (O)
5,4	GPIO82 (I/O)	XA10 (O)
7,6	GPIO83 (I/O)	XA11 (O)
9,8	GPIO84 (I/O)	XA12 (O)
11,10	GPIO85 (I/O)	XA13 (O)
13,12	GPIO86 (I/O)	XA14 (O)
15,14	GPIO87 (I/O)	XA15 (O)
16 – 31	Reserved	Reserved