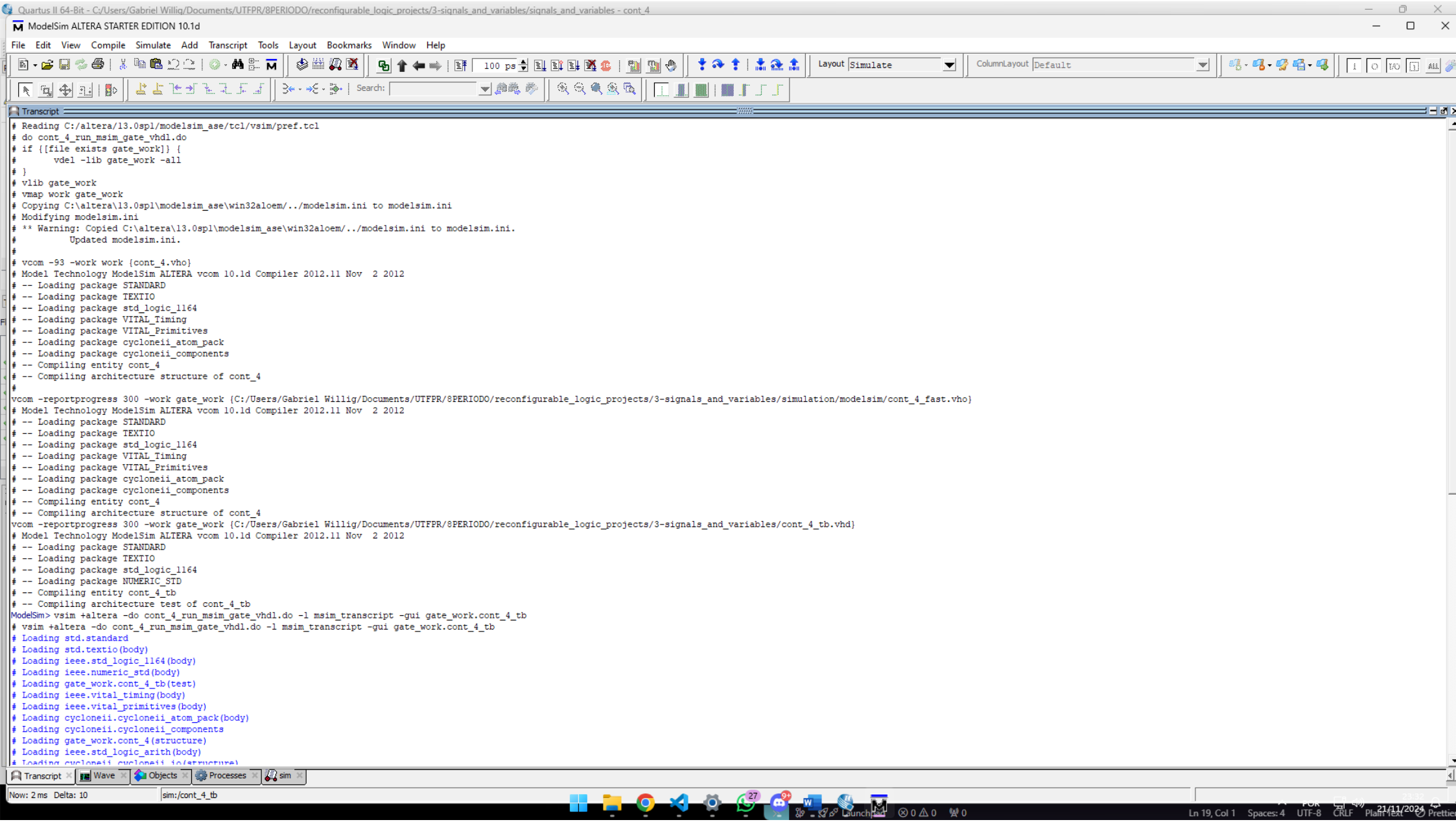
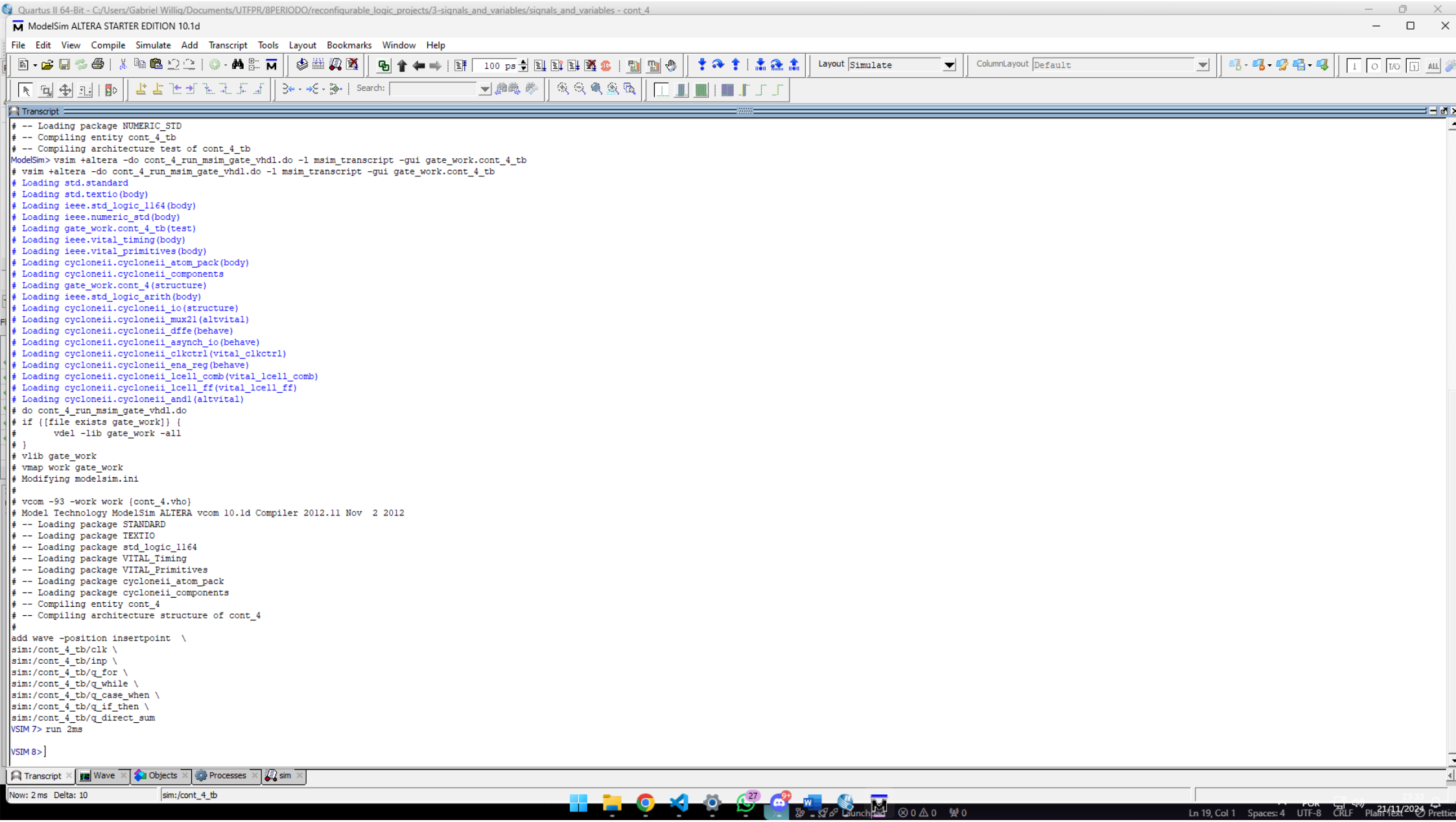
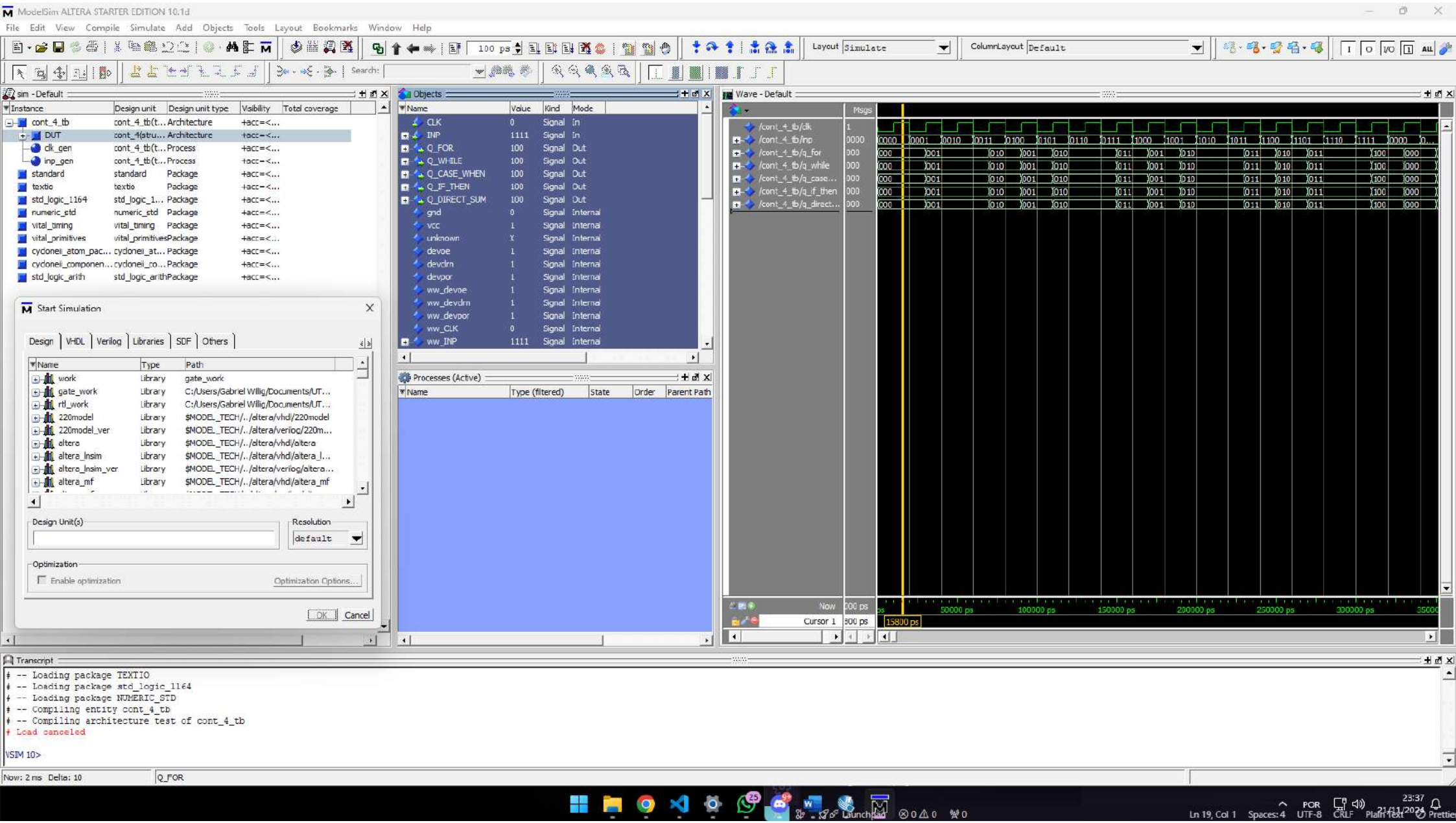

Quartus II 64-Bit - C:/Users/Gabriel Willig/Documents/UTFPR/8PERIODO/reconfigurable_logic_projects/3-signals_and_variables/signals_and_variables - cont_4
ModelSim ALTERA STARTER EDITION 10.1d
File Edit View Compile Simulate Add Transcript Tools Layout Bookmarks Window Help
Transcript
Reading C:/altera/13.0sp1/modelsim_ase/tcl/vsim/pref.tcl
do cont_4_run_msim_gate_vhdl.do
if {[file exists gate_work]} {
vdel -lib gate_work -all
}
vlib gate_work
vmap work gate_work
Copying C:\altera\13.0sp1\modelsim_ase\win32aloem/../modelsim.ini to modelsim.ini
Modifying modelsim.ini
** Warning: Copied C:\altera\13.0sp1\modelsim_ase\win32aloem/../modelsim.ini to modelsim.ini.
Updated modelsim.ini.
#
vcom -93 -work work {cont_4.vho}
Model Technology ModelSim ALTERA vcom 10.1d Compiler 2012.11 Nov 2 2012
-- Loading package STANDARD
-- Loading package TEXTIO
-- Loading package std_logic_1164
-- Loading package VITAL_Timing
-- Loading package VITAL_Primitives
-- Loading package cycloneii_atom_pack
-- Loading package cycloneii_components
-- Compiling entity cont_4
-- Compiling architecture structure of cont_4
#
vcom -reportprogress 300 -work gate_work {C:/Users/Gabriel Willig/Documents/UTFPR/8PERIODO/reconfigurable_logic_projects/3-signals_and_variables/simulation/modelsim/cont_4_fast.vho}
Model Technology ModelSim ALTERA vcom 10.1d Compiler 2012.11 Nov 2 2012
-- Loading package STANDARD
-- Loading package TEXTIO
-- Loading package std_logic_1164
-- Loading package VITAL_Timing
-- Loading package VITAL_Primitives
-- Loading package cycloneii_atom_pack
-- Loading package cycloneii_components
-- Compiling entity cont_4
-- Compiling architecture structure of cont_4
vcom -reportprogress 300 -work gate_work {C:/Users/Gabriel Willig/Documents/UTFPR/8PERIODO/reconfigurable_logic_projects/3-signals_and_variables/cont_4_tb.vhd}
Model Technology ModelSim ALTERA vcom 10.1d Compiler 2012.11 Nov 2 2012
-- Loading package STANDARD
-- Loading package TEXTIO
-- Loading package std_logic_1164
-- Loading package NUMERIC_STD
-- Compiling entity cont_4_tb
-- Compiling architecture test of cont_4_tb
ModelSim> vsim +altera -do cont_4_run_msim_gate_vhdl.do -l msim_transcript -gui gate_work.cont_4_tb
vsim +altera -do cont_4_run_msim_gate_vhdl.do -l msim_transcript -gui gate_work.cont_4_tb
Loading std.standard
Loading std.textio(body)
Loading ieee.std_logic_1164(body)
Loading ieee.numeric_std(body)
Loading gate_work.cont_4_tb(test)
Loading ieee.vital_timing(body)
Loading ieee.vital_primitives(body)
Loading cycloneii.cycloneii_atom_pack(body)
Loading cycloneii.cycloneii_components
Loading gate_work.cont_4(structure)
Loading ieee.std_logic_arith(body)
Transcript Wave Objects Processes sim
Now: 2 ms Delta: 10
sim:/cont_4_tb
Ln 19, Col 1 Spaces: 4 UTF-8 CRLF Plain Text Prettier
21/11/2024


Quartus II 64-Bit - C:/Users/Gabriel Willig/Documents/UTFPR/8PERIODO/reconfigurable_logic_projects/3-signals_and_variables/signals_and_variables - cont_4
ModelSim ALTERA STARTER EDITION 10.1d
File Edit View Compile Simulate Add Transcript Tools Layout Bookmarks Window Help
Transcript
-- Loading package NUMERIC_STD
-- Compiling entity cont_4_tb
-- Compiling architecture test of cont_4_tb
ModelSim> vsim +altera -do cont_4_run_msim_gate_vhdl.do -l msim_transcript -gui gate_work.cont_4_tb
vsim +altera -do cont_4_run_msim_gate_vhdl.do -l msim_transcript -gui gate_work.cont_4_tb
Loading std.standard
Loading std.textio(body)
Loading ieee.std_logic_1164(body)
Loading ieee.numeric_std(body)
Loading gate_work.cont_4_tb(test)
Loading ieee.vital_timing(body)
Loading ieee.vital_primitives(body)
Loading cycloneii.cycloneii_atom_pack(body)
Loading cycloneii.cycloneii_components
Loading gate_work.cont_4(structure)
Loading ieee.std_logic_arith(body)
Loading cycloneii.cycloneii_io(structure)
Loading cycloneii.cycloneii_mux21(altvital)
Loading cycloneii.cycloneii_dffe(behave)
Loading cycloneii.cycloneii_asynch_io(behave)
Loading cycloneii.cycloneii_clkctrl(vital_clkctrl)
Loading cycloneii.cycloneii_ena_reg(behave)
Loading cycloneii.cycloneii_lcell_comb(vital_lcell_comb)
Loading cycloneii.cycloneii_lcell_ff(vital_lcell_ff)
Loading cycloneii.cycloneii_and1(altvital)
do cont_4_run_msim_gate_vhdl.do
if {[file exists gate_work]} {
vdel -lib gate_work -all
}
vlib gate_work
vmap work gate_work
Modifying modelsim.ini
#
vcom -93 -work work {cont_4.vho}
Model Technology ModelSim ALTERA vcom 10.1d Compiler 2012.11 Nov 2 2012
-- Loading package STANDARD
-- Loading package TEXTIO
-- Loading package std_logic_1164
-- Loading package VITAL_Timing
-- Loading package VITAL_Primitives
-- Loading package cycloneii_atom_pack
-- Loading package cycloneii_components
-- Compiling entity cont_4
-- Compiling architecture structure of cont_4
#
add wave -position insertpoint \
sim:/cont_4_tb/clk \
sim:/cont_4_tb/inp \
sim:/cont_4_tb/q_for \
sim:/cont_4_tb/q_while \
sim:/cont_4_tb/q_case_when \
sim:/cont_4_tb/q_if_then \
sim:/cont_4_tb/q_direct_sum
VSIM 7> run 2ms
VSIM 8>
Transcript Wave Objects Processes sim
Now: 2 ms Delta: 10
sim:/cont_4_tb
Ln 19, Col 1 Spaces: 4 UTF-8 CRLF Plain Text Prettier
21/11/2024


ModelSim ALTERA STARTER EDITION 10.1d
File Edit View Compile Simulate Add Objects Tools Layout Bookmarks Window Help
sim - Default
Instance Design unit Design unit type Visibility Total coverage
cont_4_tb cont_4_tb(t... Architecture +acc=<...
DUT cont_4(stru... Architecture +acc=<...
clk_gen cont_4_tb(t... Process +acc=<...
inp_gen cont_4_tb(t... Process +acc=<...
standard standard Package +acc=<...
textio textio Package +acc=<...
std_logic_1164 std_logic_1... Package +acc=<...
numeric_std numeric_std Package +acc=<...
vital_timing vital_timing Package +acc=<...
vital_primitives vital_primitives Package +acc=<...
cycloneii_atom_pac... cycloneii_at... Package +acc=<...
cycloneii_componen... cycloneii_co... Package +acc=<...
std_logic_arith std_logic_arith Package +acc=<...
Start Simulation
Design VHDL Verilog Libraries SDF Others
Name Type Path
work Library gate_work
gate_work Library C:/Users/Gabriel Willig/Documents/UT...
rtl_work Library C:/Users/Gabriel Willig/Documents/UT...
220model Library $MODEL_TECH/../altera/vhdl/220model
220model_ver Library $MODEL_TECH/../altera/verilog/220m...
altera Library $MODEL_TECH/../altera/vhdl/altera
altera_lnsim Library $MODEL_TECH/../altera/vhdl/altera_l...
altera_lnsim_ver Library $MODEL_TECH/../altera/verilog/altera...
altera_mf Library $MODEL_TECH/../altera/vhdl/altera_mf
Design Unit(s)
Resolution
default
Optimization
Enable optimization
Optimization Options...
OK Cancel
Objects
Name Value Kind Mode
CLK 0 Signal In
INP 1111 Signal In
Q_FOR 100 Signal Out
Q_WHILE 100 Signal Out
Q_CASE_WHEN 100 Signal Out
Q_IF_THEN 100 Signal Out
Q_DIRECT_SUM 100 Signal Out
gnd 0 Signal Internal
vcc 1 Signal Internal
unknown X Signal Internal
devoe 1 Signal Internal
devclrn 1 Signal Internal
devpor 1 Signal Internal
ww_devoe 1 Signal Internal
ww_devclrn 1 Signal Internal
ww_devpor 1 Signal Internal
ww_CLK 0 Signal Internal
ww_INP 1111 Signal Internal
Processes (Active)
Name Type (filtered) State Order Parent Path
Wave - Default
Msgs
/cont_4_tb/clk
/cont_4_tb/inp
/cont_4_tb/q_for
/cont_4_tb/q_while
/cont_4_tb/q_case...
/cont_4_tb/q_if_then
/cont_4_tb/q_direct...
Now
Cursor 1
15800 ps
50000 ps
100000 ps
150000 ps
200000 ps
250000 ps
300000 ps
Transcript
-- Loading package TEXTIO
-- Loading package std_logic_1164
-- Loading package NUMERIC_STD
-- Compiling entity cont_4_tb
-- Compiling architecture test of cont_4_tb
Load canceled
VSIM 10>
Now: 2 ms Delta: 10
Q_FOR
Launchpad
Ln 19, Col 1 Spaces: 4 UTF-8 CRLF Plain Text Prettier
23:37
21/11/2024