



M2-BIG DATA

GPGPU - Chapter 6

Exercice 1



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January 12, 2021

Objectives

Improve the grayscale image converter to avoid non-coalesced access

Instructions

Create a second version of your program from exercise 2 in chapter 3 and adjust it to replace the non-coalesced accesses to global memory by coalesced accesses.

Remark : on Turing architecture, a L1 cache is automatically make non-coalesced access as coalesced on memory accesses. This new version will not be more efficient.

Tiger:



Tiger in blackwhite:



Questions

Before coding : In your code, which access is not coalesced in global memory ? (colored image read or gray image write)

The read image is the none coalesced access in global memory and it is up to us to coalesce the access to improve it

La fin.