HOWTO OpenCL with Intel FPGA devices (v1.0)

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Contents

INTRODUCTION

The goal of this document is to provide accurate steps on how to start with OpenCL with Intel FPGA devices. In my experience, the documents provided by the vendors have some missing steps or are not properly explained. I aim at:

- The board DE10-standard from Terasic, but everything can be easily adapted to other boards (from Terasic, I guess).
- Windows 10

I used the following documents to write this document:

- "DE10-Standard OpenCL": Intro, installation, etc.
- "Intel® FPGA SDK for OpenCL™ Pro Edition: Programming Guide"
- "Intel aocl starting guide"

TESTING THE BOARD

The following steps are based on the tutorial provided

1. Documents:
   1.1. "DE10-Standard OpenCL": Intro, installation, etc.
   1.2. "Intel® FPGA SDK for OpenCL™ Pro Edition: Programming Guide"
   1.3. "Intel aocl starting guide"

2. Install UART drivers
   2.1. Install drivers of UART (fdti ft232): http://www.ftdichip.com/Drivers/VCP.htm
   2.2. Run CDEM21228_setup

3. Create a linux image
   3.1. Start with http://www.terasic.com/downloads/cd-rom/de10-standard/Linux/DE10-Standard_LXDE.zip
   3.2. This is not the image recommended in the Terasic's tutorial but it has the advantage of having VGA output, so it is easy to check if the image is properly burnt in the SD-CARD. Plug a keyboard and a mouse and enjoy Ubuntu!
4. Power on the board and plug the USB UART port
   4.1. Open de Device Manager and check the Ports (COM and LPT) to see if the USB serial is there
   4.2. Copy the port number
   4.3. Set up the device for 115200 bauds, 8 bits, no parity, no control flow (these are the default settings of the linux distribution on the FPGA)
5. Create serial profile in Putty (you can use any other terminal, of course) and log in
   5.1. Power off the board (this is important)
   5.2. Create a serial connection profile with Putty selecting the port and 115200 bauds, 8 bits, no parity, no control flow.
   5.3. Open the serial connection
   5.4. Power on the board: the boot messages will be shown in the terminal window
   5.5. Log in as root (no password required)

6. Load the OpenCL kernel driver and setup variables for OpenCL run-time library

```
$ source ./init_opencl.sh
```

7. Run *Hello World* example

```
$ cd terasic/hello_world/
$ ls # to see files in the folder
$ ./host # to launch application
```

8. Launch *vector_add* demo

```
$ cd ../vector_add/
$ ls # to see files in the folder
$ ./host # to launch application
```

INSTALLING THE SDK

1. Documents:
    a. "DE10-Standard OpenCL": Intro, installation, etc.
    b. "Intel® FPGA SDK for OpenCL™ Pro Edition: Programming Guide"
    c. "Intel aocl starting guide"
2. Install Intel FPGA SDK for OpenCL (which includes Quartus Prime Standard (18.0))
    a. http://fpgasoftware.intel.com/opencl/18.0/?edition=standard&download_manager=dlm3
    b. I am installing the "standard edition" since my board makes use of a Cyclone V FPGA.
    c. Quite distressing that you have to download 20GB of files since you are forced to download the OpenCL SDK, Quartus Prime and all device files. A waste of time.
    d. Read the "aocl starting guide"
    e. Unzip and run "setup.bat"
    f. Since I have already installed Quartus I will try to skip that… Well, it seems that it is possible. Select the "Intel FPGA SDK for OpenCL". Despite the fact that Quartus is checked by default (and it is not possible to uncheck), it is detecting that it is already there and it is not installing it (good news). If you don't have Quartus installed, I guess it will install it.
    g. At the end it will ask to install the USB drivers, I chose not to since I had already them installed.

3. Install Intel SOC EDS
    a. http://fpgasoftware.intel.com/soceds/
    b. Install the SOC EDS tool
    c. Do not forget to launch the installation of ARM DS-5
4. Download DE10-Standard_OpenCL_XX.X_BSP (I am using 18.0 ver.)
    a. https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&No=1081&PartNo=4
    b. Look for the IntelFPGA folder and create a folder called "hld/board/terasic" (in my case it was "c:/IntelFPGA/18.0"
    c. Unzip the BSP file in the the root floder of Intel
5. Create an environment variable for OpenCL SDK:
    a. First check if the INTELFPGAOCLSDKROOT and AOCL_BOARD_PACKAGE_ROOT have been already created:
    echo %INTELFPGAOCLSDKROOT%
    echo %AOCL_BOARD_PACKAGE_ROOT%

    b. INTELFPGAOCLSDKROOT=c:\IntelFPGA\18.0\hls
    (in the documentation, it is written *hld*, but in my installation is missing)
    c. AOCL_BOARD_PACKAGE_ROOT=
    c:\IntelFPGA\18.0\hld\board\terasic\de10_standard
    d. Add to the PATH variable the following:
        i. %INTELFPGAOCLSDKROOT%\bin
        ii. %INTELFPGAOCLSDKROOT%\host\windows64\bin
6. Test OpenCL
    a. Open a CMD window

b. Type “aocl ver”
   This should show something similar to “aocl 18.0.0.614 (Intel(R) FPGA SDK for OpenCL(TM), Version 18.0.0 Build 614 Standard Edition, Copyright (C) 2018 Intel Corporation)”
c. The manual indicates to type “aoc -list-boards”

COMPILING OPENCL FOR FPGA DEVICES (INCOMPLETE)

1. Documents:
    a. “DE10-Standard OpenCL”: Intro, installation, etc.
    b. “Intel® FPGA SDK for OpenCL™ Pro Edition: Programming Guide”
    c. “Intel aocl starting guide”
2. Compiling our first example
   Here we are going to compile a test example that comes with the compilation process has two parts:
    - Compilation of OpenCL kernel, which implies generating the FPGA bitstream. This is a long process since it requires the synthesis and P&R tasks
    - Compilation of host program. This is a standard OpenCL compilation, so it should not be long.

    a. Kernel compilation
        i. Type

```
> cd G:\intelFPGA\18.0\hld\board\terasic\de10_standard\test\boardtest
```

or

```
> cd %AOCL_BOARD_PACKAGE_ROOT%\test\boardtest”
```

        ii. Type

```
> aoc boardtest.cl  -o bin\boardtest.aocx  -board=de10_standard_sharedonly
  -v -report
```

This process may take half an hour. The compiler outputs:

```
c:\intelFPGA\18.0\hld\board\terasic\de10_standard\test\boardtest>aoc
boardtest.cl  -o bin\boardtest.aocx  -board=de10_standard_sharedonly -v -
report

aoc: Environment checks are completed successfully.

aoc: Cached files in C:\Users\gacaf\AppData\Local\aocl may be used to reduce
compilation time

You are now compiling the full flow!!

aoc: Selected target board de10_standard_sharedonly

aoc: Running OpenCL parser....

c:/intelFPGA/18.0/hld/board/terasic/de10_standard/test/boardtest/boardtest.cl:
78:20: warning: declaring kernel argument with no 'restrict' may lead to low
kernel performance

    __global uint *dst,

                  ^

c:/intelFPGA/18.0/hld/board/terasic/de10_standard/test/boardtest/boardtest.cl:
79:26: warning: declaring kernel argument with no 'restrict' may lead to low
kernel performance

    __global const uint *index,

                         ^

2 warnings generated.
```

```
aoc: OpenCL parser completed successfully.
aoc: Optimizing and doing static analysis of code...
aoc: Linking with IP library ...
Checking if memory usage is larger than 100%

!===========================================================================
! The report below may be inaccurate. A more comprehensive
! resource usage report can be found at boardtest/reports/report.html
!===========================================================================

+--------------------------------------------------------------------+
; Estimated Resource Usage Summary                                  ;
+---------------------------------------+----------------------------+
; Resource                              + Usage                      ;
+---------------------------------------+----------------------------+
; Logic utilization                     ;   38%                      ;
; ALUTs                                 ;   22%                      ;
; Dedicated logic registers             ;   18%                      ;
; Memory blocks                         ;   32%                      ;
; DSP blocks                            ;    0%                      ;
+---------------------------------------+----------------------------;
aoc: First stage compilation completed successfully.
Compiling for FPGA. This process may take a long time, please be patient.
aoc: Hardware generation completed successfully.
```

b. Compiling host program

i. Launch the Embedded Command shell

```
> cd C:\IntelFGPA\18.0\embedded
> Embedded_Command_Shell.bat
```

The prompt will turn green.

ii. Type

```
> cd
/cygdrive/G/intelFPGA/18.0/hld/board/terasic/de10_
standard/test/boardtest/
> ls
```

(This is to check the test files. The host program files are in folder “host”)

```
> make
```

(This is to build the host executable)

I stop here. The next step is to scopy the files into the FPGA board and execute. Coming soon…