GATE Exercises on Digital Design

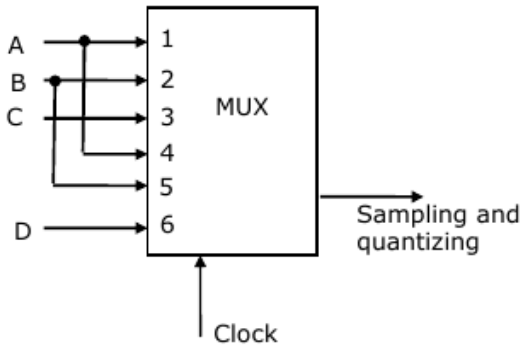


Fig. 2

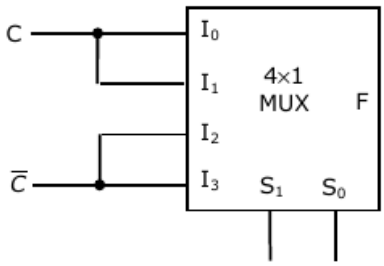


Fig. 3

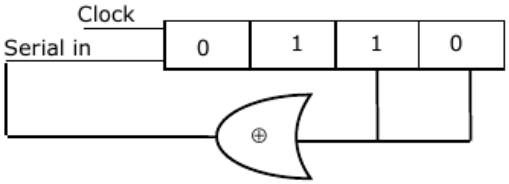


Fig. 4

***Abstract*—This problem set has questions related to combinational and sequential circuits taken from GATE papers over the last twenty years. Teachers can use the problem set for courses tutorials.**

1) Convert an $S-R$ FLIP-FLOP into a T FLIP FLOP.
2) A sequential multiplexer is connected as shown in Fig. 2. Each time the multiplexer receives the clock, it switches to the next channel(From 6 it goes to 1). If the input signals are
   (a) $A = 5\cos 2\pi(4 \times 10^3 t)$
   (b) $B = 2\cos 2\pi(3.8 \times 10^3 t)$
   (c) $C = 6\cos 2\pi(2.2 \times 10^3 t)$
   (d) $D = 4\cos 2\pi(1.7 \times 10^3 t)$

   the minimum clock frequency should be _____ KHz.
3) The logic realized by the circuit shown in Fig. 3 is :
   (a) $F = A.C$
   (b) $F = A + C$
   (c) $F = B.C$
   (d) $F = B + C$
4) The initial contents of the 4−bit serial-in-parallel-out, right-shift, Shift Register shown in Fig. 4 , is 0 1 1 0. After three clock pulses are applied, the contents of the Shift Register will be
   (a) 0 0 0 0
   (b) 0 1 0 1
   (c) 1 0 1 0
   (d) 1 1 1 1
5) A new clocked $X-Y$ flip flop is defined with two inputs, X and Y is addition to the clock input. The flip flop functions as follows:
   If $XY = 00$, the flip flop changes stage with each clock pulse
   If $XY = 01$, the flip flop state Q becomes

1 with the next clock pulse
If $XY = 10$, the flip flop state Q becomes 0 with the next clock pulse
If $XY = 11$, the change of state occurs with the clock pulse

(a) Write the Truth table for the $X-Y$ flip flop
(b) Write the Excitation table for the $X-Y$ flip flop
(c) It is desired to convert a $J-K$ flip flop into the $X-Y$ flip flop by adding some external gates, if necessary. Draw a circuit to show how you will implement in $X-Y$ flip flop using a $J-K$ flip flop.

6) 2's complement representation of a 16-bit number (one sign bit and 15 magnitude bits) is FFFI. Its magnitude in decimal representation is
   (a) 0
   (b) 1
   (c) $32,767$
   (d) $65,535$
7) Signals A, B, C, D and $\bar{D}$ are available. Using a single 8 to 1 multiplexer and no other gate, implement the Boolean function $f(A,B,C,D) = B.C + A.B.\bar{D} + \bar{A}.\bar{C}.D$
8) A clocked sequential circuit has three states, A, B and C and one input X. As long as the input X is 0, the circuit alternates between the states A and B. If the input X becomes 1 (either in state A or in state B),the circuit goes to state C and remains in state C as long as X continues to be 1. The circuit returns to state A if the input becomes 0 once again and from then on repeats its behaviour.Assume that the state assignments are $A = 00$, $B = 01$ and $C = 10$.
   (a) Draw the state diagram of the circuit
   (b) Give the state table for the circuit
   (c) Draw the circuit using D flip flops
9) Match each of the items A,B and C with an appropriate item on the right.

(a) A shift register can be used	(1) for code conversion
(b) A multiplexer can be used	(2) to generate memory chip select
(c) A decoder can be used	(3) for parallel-to-serial conversion
	(4) as a many-to-one switch
	(5) for analog-to-digital conversion

10) A 2 bit binary multiplier can be implemented using
   (a) 2 inputs ANDs only
   (b) 2 input XORs and 4 input AND gates only
   (c) Two 2 inputs NORs and one XNOR gate
   (d) XOR gates and shift registers
11) A signed integer has been stored in a byte using the 2's complement format. We wish to store the same integer in a 16 bit word. We should
   (a) copy the original byte to the less significant byte of the word and fill the more significant with zeros
   (b) copy the original byte to the more significant byte of the word and fill the less significant byte with zeros
   (c) copy the original byte to the less significant byte of the word and make each fit of the more significant byte equal to the most significant bit of the original byte
   (d) copy the original byte to the less significant byte as well as the more significant byte of the word
12) In a $J-K$ flip-flop we have $J = Q$ and $K = 1$. Assuming the flip flop was initially cleared and then clocked for 6 pulses, the

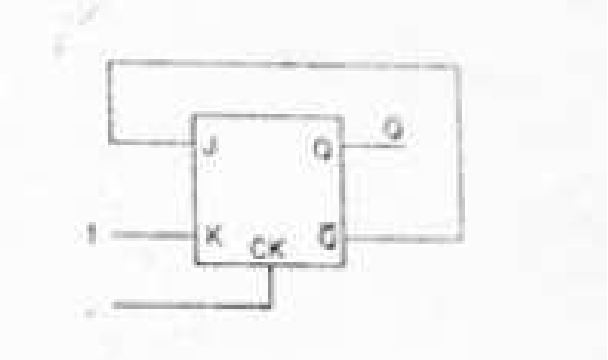


Fig. 12

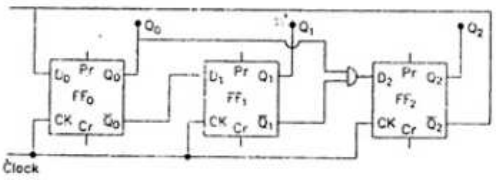


Fig. 13

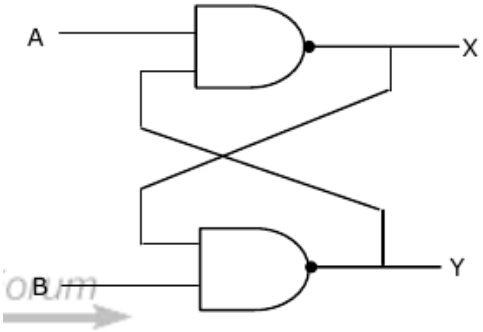


Fig. 14

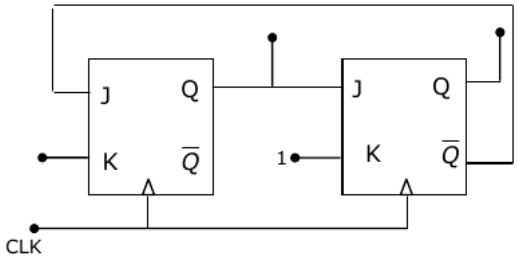


Fig. 17

sequence at the Q output will be

(a) 010000
(b) 011001
(c) 010010
(d) 010101

13) A sequence generator is shown in the Fig. 13 is The counter status (Q_0, Q_1, Q_2) is initialised to 010 using preset/clear inputs. The clock has a period of 50 ns and transitions take place at the rising clock edge.
   (a) Give the sequence generate at Q_0 till it repeats.
   (b) What is the repetition rate of the generated sequence?

14) In Fig. 14, $A = 1$ and $B = 1$, the input B is now replaced by a sequence 101010.... the outputs x and y will be
   (a) fixed at 0 and 1, respectively
   (b) x = 1010.... while y = 0101....
   (c) x = 1010.... and y = 0101....
   (d) fixed at 1 and 0, respectively

15) An equivalent 2's complement representation of the 2's complement number 1101 is
   (a) 110100
   (b) 001101
   (c) 110111
   (d) 111101

16) Two 2's complement number having sign bits x and y are added and the sign bit of the result is z. Then, the occurrence of overflow is indicated by the Boolean function
   (a) $x\ y\ z$
   (b) $\overline{x}\ \overline{y}\ \overline{z}$
   (c) $\overline{x}\ \overline{y}\ z\ +\ x\ y\ \overline{z}$
   (d) $xy\ +\ yz\ +\ zx$

17) Fig. 17, shows a $mod - K$ counter, here K is equal to
   (a) 1
   (b) 2
   (c) 3

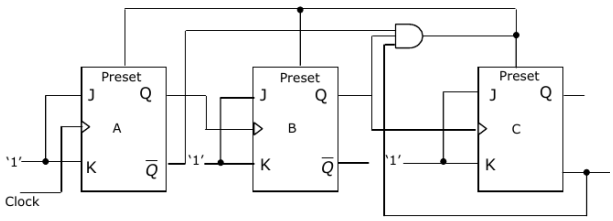


Fig. 19

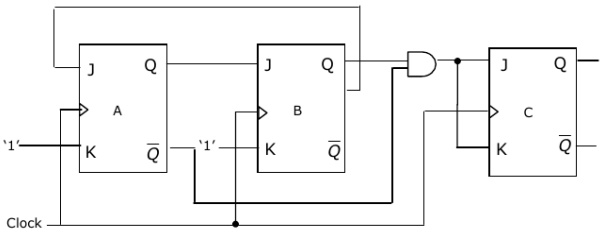


Fig. 20

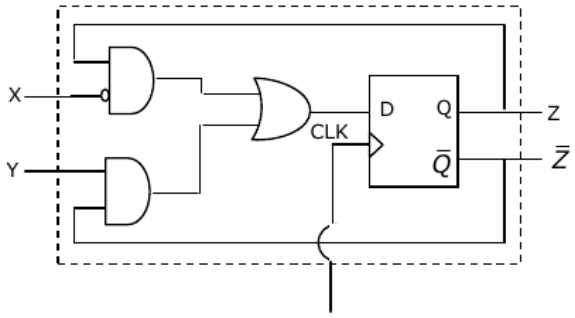


Fig. 21

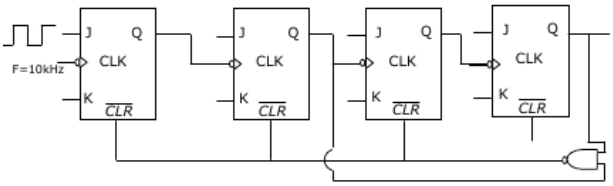


Fig. 22

(d) 4

18) For a binary half-sub-tractor having two inputs A and B, the correct set of logical expressions for the outputs D (=A minus B) and X(=borrow) are
   (a) $D = A\overline{B} + \overline{A}B, X = \overline{A}B$
   (b) $D = \overline{A}\overline{B} + A\overline{B} + A\overline{B}, X = A\overline{B}$
   (c) $D = \overline{A}B + A\overline{B}, X = \overline{A}B$
   (d) $D = AB + \overline{A}\overline{B}, X = A\overline{B}$
19) The ripple counter shown in Fig. 19 works as a
   (a) mod - 3 up counter
   (b) mod - 5 up counter
   (c) mod - 3 down counter
   (d) mod - 5 down counter
20) The circuit diagram of a synchronous counter is shown in Fig. 20. Determine the sequence of states of the counter assuming that the initial state is $'000'$. Give your answer in a tabulor form showing the present state $Q_{A(n)}, Q_{B(n)}, Q_{C(n)}, J-K$ inputs (J_A, K_A, J_B, J_C, K) and the next state $Q_{A(n+1)}, Q_{B(n+1)}, Q_{C(n+1)}$. From the table, determine the modulus of the counter.
21) A sequential circuit using D flip flop and logic gates is shown in Fig. 21,where X and Y are the inputs and Z is the output. The circuit is
   (a) $S-R$ Flip-Flop with inputs $X = R$ and $Y = S$
   (b) $S-R$ Flip-Flop with inputs $X = S$ and $Y = R$
   (c) $J-K$ Flip-Flop with inputs $X = J$ and $Y = K$
   (d) $J-K$ Flip-Flop with inputs $X = K$ and $Y = J$
22) In Fig. 22, the J and K inputs of all the four Flip-Flops are made high. The frequency of the signal at output Y is
   (a) 0.833 KHz
   (b) 1.0 KHz
   (c) 0.91 KHz
   (d) 0.77 KHz
23) A one-bit full adder is to be implemented using 8-to-1 multiplexers(MUX).
   (a) Write the truth table for sum (S) and carry to the next stage (C_N) in terms of the two bits(A, B) and carry from the previous stage (C_p).The truth table

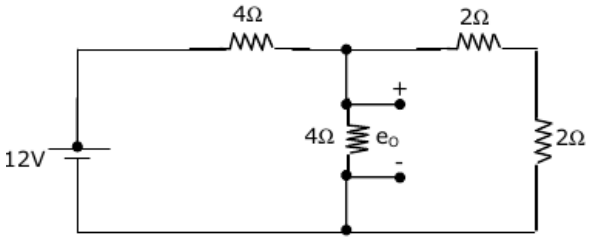


Fig. 24

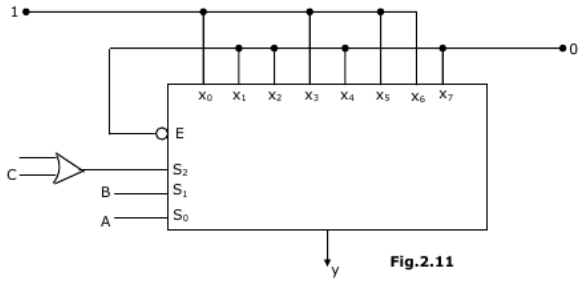


Fig. 25

should be in the ascending order of (A, B, C_p),i.e(000, 001, 010, ...etc.).

(b) Implement S and C_N using 8-to-1 multiplexers.

24) The voltage e_0 in Fig. 24 is
   (a) $2V$
   (b) $\frac{4}{3}V$
   (c) $4V$
   (d) $8V$

25) In the TTL circuit in Fig. 25, S_2 to S_0 are select lines and X_7 and X_0 are input lines. S_0 and X_0 are LSBs. The output Y is
   (a) indeterminate
   (b) $\overline{A \oplus B}$
   (c) $\overline{A} \oplus \overline{B}$
   (d) $\overline{C}.\overline{(A \oplus B)} + C.(A \oplus B)$

26) The digital block in Fig. 26 is realized using two positive edge triggered D-flip-flops. Assume that for $t < t_0$, $Q_1 = Q_2 = 0$.The circuit in the digital block is given by:
   (a) Figure (a)

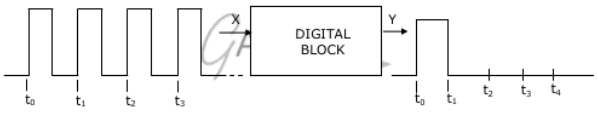


Fig. 26

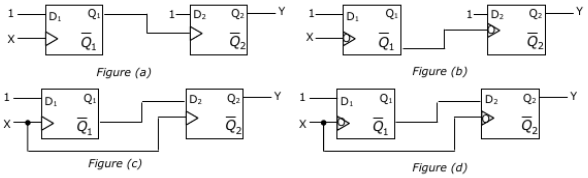


Fig. 26

   (b) Figure (b)
   (c) Figure (c)
   (d) Figure (d)

27) In Fig. 27, the output of the oscillator, V_1 has $10V$ peak amplitude with zero DC value. The transfer characteristic of the Schmitt inverter is also shown in Fig. Assume that the JK flip-flop is resent at time $t = 0$.
   (a) What is the period and duty cycle of the waveform V_2?
   (b) What is the period and duty cycle of the waveform V_3?
   (c) Sketch V_1, V_2 *and* V_3 for the duration $0 \le t \le 6\mu s$. Clearly indicate the exact timings when the waveforms V_2 and V_3 make high-to-low and low-to-high transitions.

28) In the network of Fig. 28, the maximum

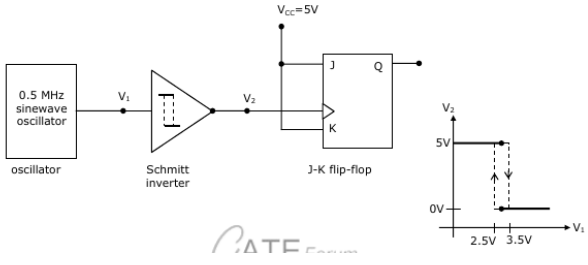


Fig. 27

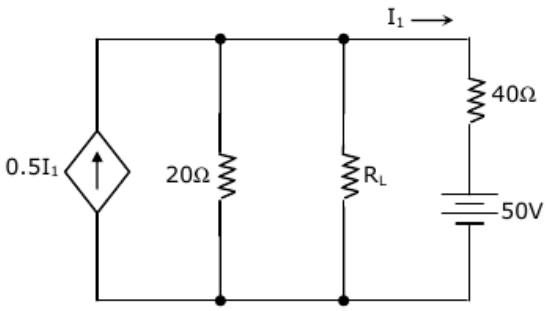


Fig. 28

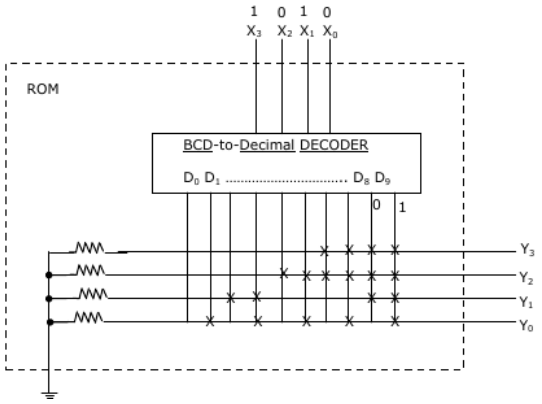


Fig. 29

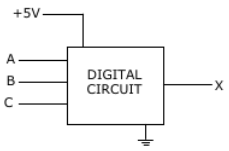
power is delivered to R_L if its value is

(a) 16Ω
(b) $\frac{40}{3}$Ω
(c) 60Ω
(d) 20Ω

29) If the input X_3, X_2, X_1, X_0 to the ROM in Fig. 29 are $8-4-2-1$ BCD numbers, then the outputs Y_3, Y_2, Y_1, Y_0 are

(a) gray code numbers
(b) $2-4-2-1$ BCD numbers
(c) excess 3 code numbers
(d) none of the above

30) The inputs to a digital circuit shown in Fig. 30 are the external signals A, B and C.
($\overline{A}, \overline{B}$ and $\overline{C}$ are not available). The $+5V$ power supply (logic 1) and the ground (logic 0) are also available. The output



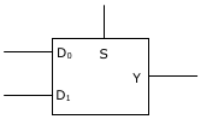


Table 9

S	Y
0	D_0
1	D_1

Fig. 30

of the circuit is $X = \overline{A}B + \overline{A}\ \overline{B}\ \overline{C}$.

(a) Write down the output function in its canonical SOP and POS forms.
(b) Implement the circuit using only two $2:1$ multiplexers shown in figure (b),where S is the data-select line D_0 and D_1 are the input data lines and Y is the output lines. The function table for the multiplexer is given in table 9.

31) It is required to design a binary mod-5 synchronous counter using AB flip-flops such that the output Q_2, Q_1, Q_0 changes as $000 \rightarrow 001 \rightarrow 010$..... and so on. The excitation table for the AB flip-flop is given in table.

(a) Write down the state table for the mod-5 counter.
(b) Obtain simplified SOP expressions for the inputs A_2, B_2, A_1, B_1, A_0 and B_0 in terms of Q_2, Q_1, Q_0 and their complements.
(c) Hence, complete the circuit diagram for the mod-5 counter given in Fig. 31 using minimum number of 2-input NAND-gate only.

32) Without any additional circuitry, an $8:1$ MUX can be used to obtain

(a) some but not all Boolean functions of 3 variables
(b) all function of 3 variables but none of 4 variables
(c) all functions of 3 variables and some but not all of 4 variables
(d) all functions of 4 variables

33) A 0 to 6 counter consists of 3 flip flops and a combination circuit of 2 input gate(s).

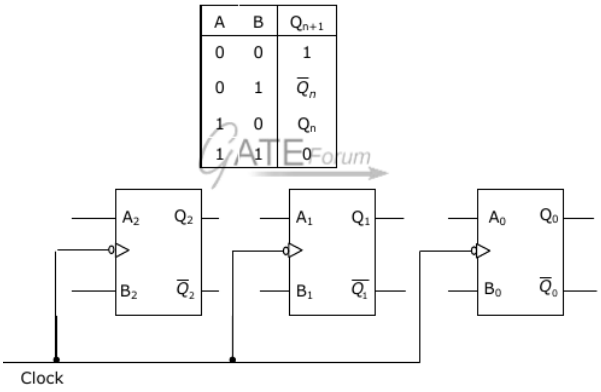


Fig. 31

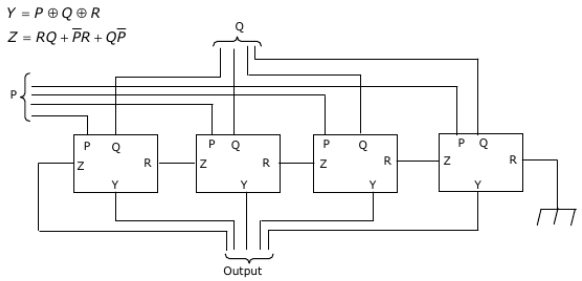


Fig. 34

The combination circuit consists of

(a) one AND gate
(b) one OR gate
(c) one AND gate and one OR gate
(d) two AND gates

34) The circuit shown in Fig. 34 has 4 boxes each described by inputs P, Q, R and outputs Y, Z with
The circuit acts as a
(a) 4 bit adder giving $P + Q$
(b) 4 bit subtractor-giving $P - Q$
(c) 4 bit subtractor-giving $Q - P$
(d) 4 bit adder giving $P + Q + R$

35) A 4 bit ripple counter and a 4 bit synchronous counter are made using flip-flops having a propagation delay of 10 ns each. If the worst case delay in the ripple counter and the synchronous counter be R and S respectively, then

Group 1	Group 2
P. Shift register	1. Frequency division
Q. Counter	2. Addressing in memory chips
R. Decoder	3. Serial to parallel data conversion

Fig. 38

(a) $R = 10\ ns, S = 40\ ns$
(b) $R = 40\ ns, S = 10\ ns$
(c) $R = 10\ ns, S = 30\ ns$
(d) $R = 30\ ns, S = 10\ ns$

36) A master slave flip-flop has the characteristic that
(a) change in the input immediately reflected in the output
(b) change in the output occurs when the state of the master is affected
(c) change in the output occurs when the state of the slave is affected
(d) both the master and the slave states are affected at the same time

37) The range of signed decimal numbers that can be represented by 6-bite 1's complement number is
(a) -31 to $+31$
(b) -63 to $+64$
(c) -64 to $+63$
(d) -32 to $+31$

38) Choose the correct one from among the alternatives A, B, C, D after matching an item from Group 1 with the most appropriate item in Group 2.
(a) $P - 3$ $Q - 2$ $R - 1$
(b) $P - 3$ $Q - 1$ $R - 2$
(c) $P - 2$ $Q - 1$ $R - 3$
(d) $P - 1$ $Q - 2$ $R - 2$

39) The minimum number of 2 to 1 multiplexers required to realize a 4 to 1 multiplexer is
(a) 1
(b) 2
(c) 3
(d) 4

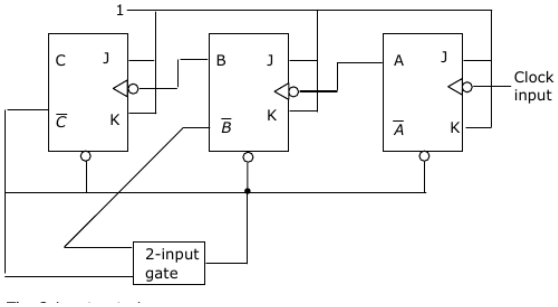


Fig. 41

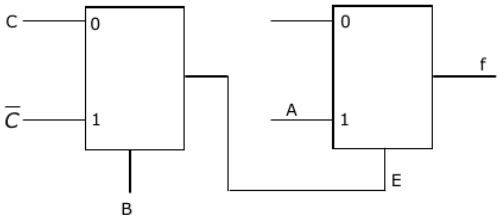


Fig. 42

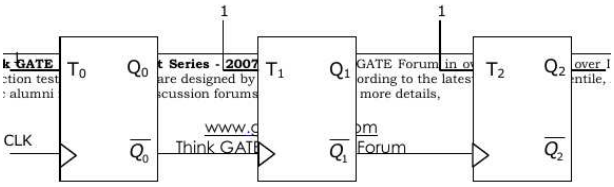


Fig. 44

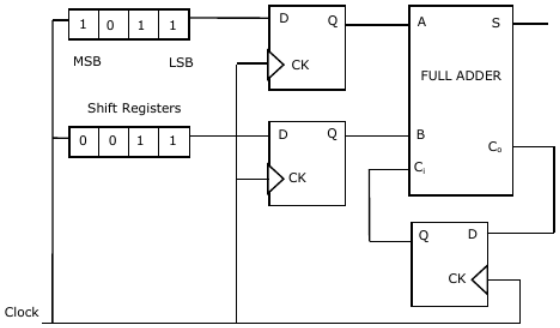


Fig. 45

40) 11001, 1001 and 111001 correspond to the 2's complement representation of which one of the following sets of number?
(a) 25, 9 and 57 respectively
(b) −6, −6 and −6 respectively
(c) −7, −7 and −7 respectively
(d) −25, −9 and −57 respectively

41) In the modulo-6 ripple counter shown in Fig. 41, the output of the 2-input gate is used to clear the $J-K$ flip-flops.
The 2-input gate is
(a) a NAND gate
(b) a NOR gate
(c) an OR gate
(d) an AND gate

42) The Boolean function f implemented in Fig. 42 using two input multiplexers is
(a) $A\overline{B}C + AB\overline{C}$
(b) $ABC + A\overline{B}\,\overline{C}$
(c) $\overline{A}BC + \overline{A}\,\overline{B}\,\overline{C}$
(d) $\overline{A}\,\overline{B}C + \overline{A}B\overline{C}$

43) The present output Q_n of an edge triggered JK flip-flop is logic 0. If $J = 1$, then Q_{n+1}
(a) cannot be determined
(b) will be logic 0
(c) will be logic 1
(d) will race around

44) Fig. 44 shows a ripple counter using positive edge triggered flip-flops. If the present state of counter is $Q_2Q_1Q_0 = 011$, then its next state ($Q_2Q_1Q_0$) will be
(a) 010
(b) 100
(c) 111
(d) 101

45) For the circuit shown in Fig. 45 below, two 4-bit parallel-in serial-out shift registers loaded with the data shown are used to feed the data to a full adder. Initially, all the flip-flops are in clear state. After applying two clock pulses, the outputs of the full-adder should be
(a) $S = 0$ $C_0 = 0$
(b) $S = 0$ $C_0 = 1$
(c) $S = 1$ $C_0 = 0$
(d) $S = 1$ $C_0 = 1$

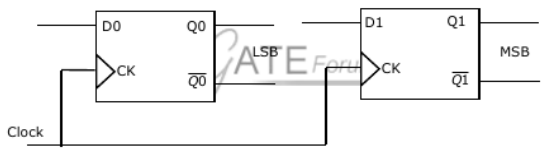


Fig. 46

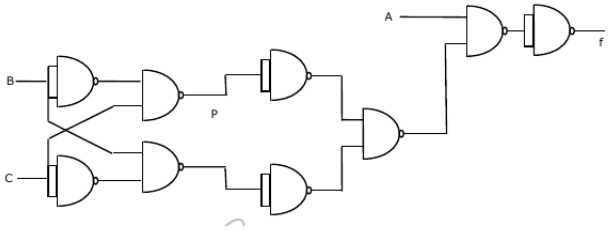


Fig. 47

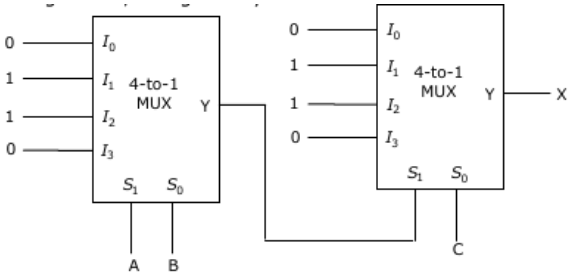


Fig. 49

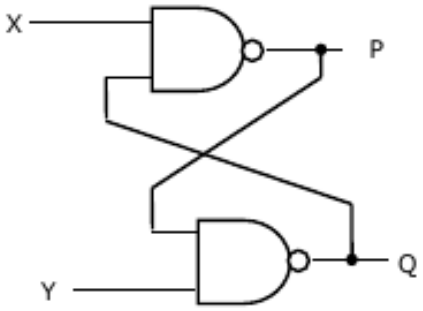


Fig. 50

46) Two D-flip-flops, as shown below in Fig. 46, are to be connected as a synchronous counter that goes through the following Q_1Q_0 sequence
$00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00 \rightarrow$ .....
The inputs D_0 and D_1 respectively should be connected as
(a) $\overline{Q_1}$ and Q_0
(b) $\overline{Q_0}$ and Q_1
(c) $\overline{Q_1}Q_0$ and $\overline{Q_1}Q_0$
(d) $\overline{Q_1}\ \overline{Q_0}$ and Q_1Q_0

47) The point P in the following Fig. 47 is stuck-at-1. The output f will be
(a) $\overline{A\overline{BC}}$
(b) $\overline{A}$
(c) $A\overline{BC}$
(d) A

48) X = 01110 and Y = 11001 are two 5-bit binary numbers represented in two's complement format. The sum of X and Y represented in two's complement format using 6 bits is :
(a) 100111
(b) 001000
(c) 000111
(d) 101001

49) In the following circuit in Fig. 49, X is given by
(a) $X = A\overline{B}\,\overline{C} + \overline{A}B\overline{C} + \overline{A}\,\overline{B}C + ABC$
(b) $X = \overline{A}BC + A\overline{B}C + AB\overline{C} + \overline{A}\,\overline{B}\,\overline{C}$
(c) $X = AB + BC + AC$
(d) $X = \overline{A}\,\overline{B} + \overline{B}\,\overline{C} + \overline{A}\,\overline{C}$

50) The following binary values were applied to the X and Y inputs of the NAND latch shown in the Fig. 50 in the sequence indicated below:
$X = 0, Y = 1;\ X = 0, Y = 0;\ X = 1, Y = 1;$
The corresponding stable P,Q outputs will be :
(a) $P = 1,\ Q = 0;\ P = 1,\ Q = 0;\ P = 1,\ Q = 0$ or $P = 0,\ Q = 1$
(b) $P = 1,\ Q = 0;\ P = 0,\ Q = 1;$ or $P = 0,\ Q = 1$ $P = 0,\ Q = 1$
(c) $P = 1,\ Q = 0;\ P = 1,\ Q = 1;\ P = 1,\ Q = 0$ or $P = 0,\ Q = 1$
(d) $P = 1,\ Q = 0;\ P = 1,\ Q = 1;\ P = 1,\ Q = 1$

51) For the circuit shown, the counter state

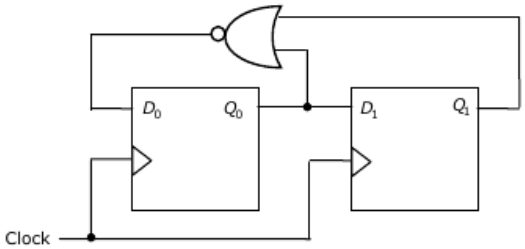


Fig. 51

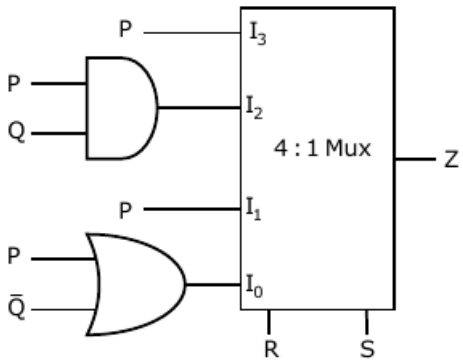


Fig. 53

$(Q_1 Q_0)$ follows the sequence

(a) 00, 01, 10, 11, 00...
(b) 00, 01, 10, 00, 01...
(c) 00, 01, 11, 00, 01...
(d) 00, 10, 11, 00, 10...

52) The two numbers represented in signed 2's complement form are P = 11101101 and Q = 11100110. If Q is subtracted from P, the value obtained in signed 2's complement form is

(a) 100000111
(b) 00000111
(c) 11111001
(d) 111111001

53) For the circuit shown in Fig. 53, 32 $I_0 - I_3$ are inputs to the 4 : 1 multiplexer R(MSB) and S are control bits
The output Z can be represented by

(a) $PQ + P\overline{Q}S + \overline{Q}\ \overline{R}\ \overline{S}$
(b) $P\overline{Q} + PQ\overline{R} + \overline{P}\ \overline{Q}\ \overline{S}$

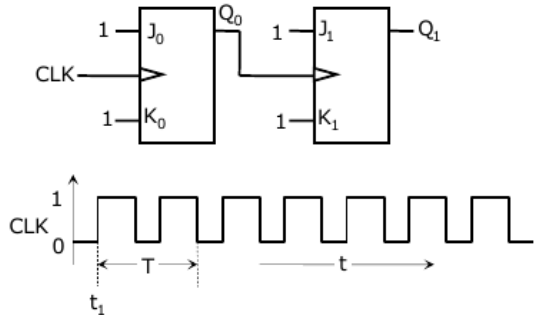


Fig. 54

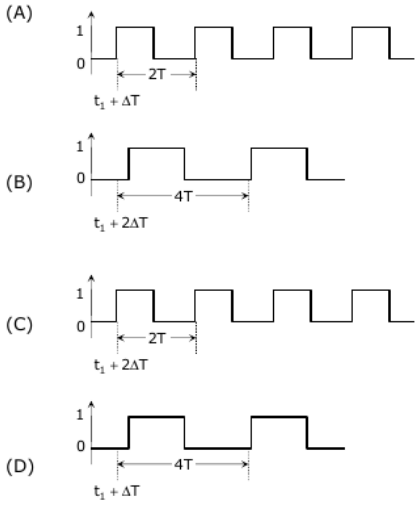


Fig. 54

(c) $P\overline{Q}\ \overline{R} + \overline{P}QR + PQRS + \overline{Q}\ \overline{R}\ \overline{S}$
(d) $PQ\overline{R} + PQR\overline{S} + P\overline{Q}\ \overline{R}S + \overline{Q}\ \overline{R}\ \overline{S}$

54) For each of the positive edge-triggered $J - K$ flip flop used in the following Fig. 54,the propagation delay is $\triangle T$
Which of the following waveforms in Fig. 54 correctly represents the output at Q_1 ?

55) For the circuit shown in the Fig. 55, D has a transition from 0 to 1 after CLK changes from 1 to 0. Assume gate delays to be negligible
Which of the following statements is true?

(a) Q goes to 1 at the CLK transition and stays at 1
(b) Q goes to 0 at the CLK transition and stays at 0

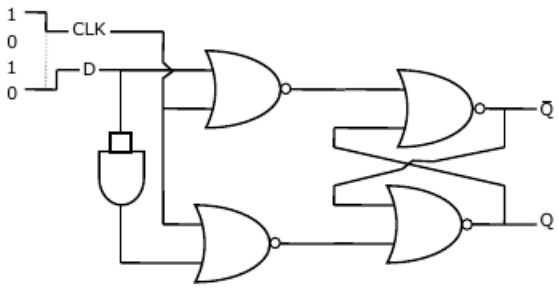


Fig. 55

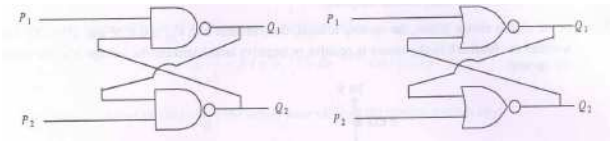


Fig. 58

(c) Q goes to 1 at the CLK transition and goes at 0 when D goes to 1
(d) Q goes to 0 at the CLK transition and goes to 1 when D goes to 1

56) The stable reading of the LED display is
(a) 06
(b) 07
(c) 12
(d) 13

57) What are the minimum number of 2-to-1 multiplexers required to generate a 2-input AND gate and a 2-input Ex-OR gate?
(a) 1 and 2
(b) 1 and 3
(c) 1 and 1
(d) 2 and 2

58) Refer to the NAND and NOR latches shown in the Fig. 58. The inputs (P_1, P_2) for both the latches are first made $(0, 1)$ and then, after a few seconds, made $(1, 1)$. The corresponding stable outputs (Q_1, Q_2) are
(a) NAND: first $(0, 1)$ then $(0, 1)$ NOR: first $(1, 0)$ then $(0, 0)$
(b) NAND: first $(1, 0)$ then $(1, 0)$ NOR: first $(1, 0)$ then $(1, 0)$

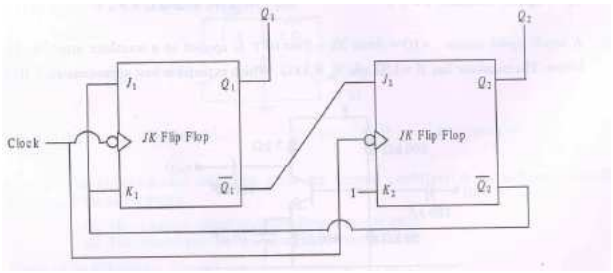


Fig. 59

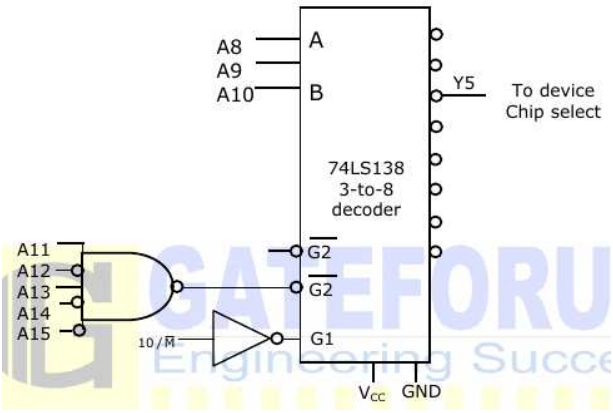


Fig. 60

(c) NAND: first $(1, 0)$ then $(1, 0)$ NOR: first $(1, 0)$ then $(0, 0)$
(d) NAND: first $(1, 0)$ then $(1, 1)$ NOR: first $(0, 1)$ then $(0, 1)$

59) What are the counting states $(Q_1 Q_2)$ for the counter shown in the Fig. 59 below?
(a) 11, 10, 00, 11, 10...
(b) 01, 10, 11, 00, 01...
(c) 00, 11, 01, 10, 00...
(d) 01, 10, 00, 01, 10...

60) In the circuit shown, the device connected to $Y5$ can have address in the range
(a) $2000 - 20FF$
(b) $2D00 - 2DFF$
(c) $2E00 - 2EFF$
(d) $FD00 - FDFF$

61) Assuming that flip-flops are in reset condition initially, the count sequence observed at Q_A in the circuit shown is

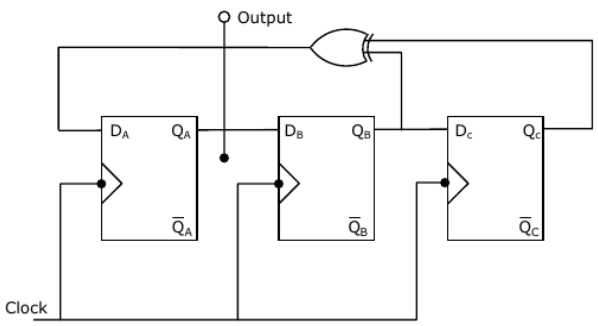


Fig. 61

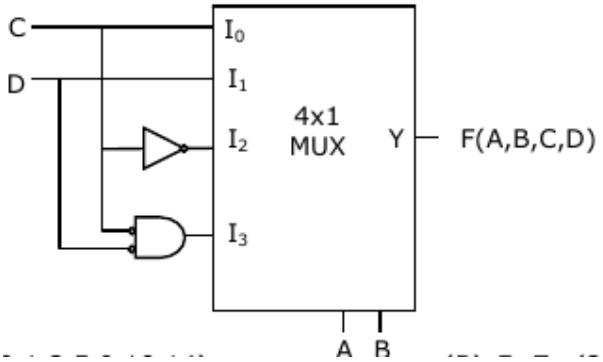


Fig. 62

(a) 0010111...
(b) 0001011...
(c) 0101111...
(d) 0110100...

62) The Boolean function realized by the logic circuit shown is
(a) $F = \Sigma m(0, 1, 3, 5, 9, 10, 14)$
(b) $F = \Sigma m(2, 3, 5, 7, 8, 12, 13)$
(c) $F = \Sigma m(1, 2, 4, 5, 11, 14, 15)$
(d) $F = \Sigma m(2, 3, 5, 7, 8, 9, 12)$

63) When the output Y in the circuit below is $'1'$, it implies that data has
(a) changed from 0 to 1
(b) changed from 1 to 0
(c) changed in either direction
(d) not changed

64) The logic function implemented by the circuit below is (ground implies logic 0)

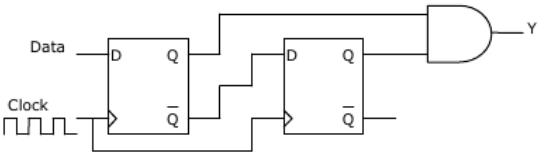


Fig. 63

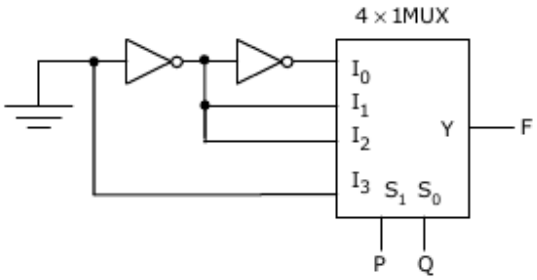


Fig. 64

(a) $F = AND(P, Q)$
(b) $F = OR(P, Q)$
(c) $F = XNOR(P, Q)$
(d) $F = XOR(P, Q)$

65) The output of a 3-stage Johnson (twisted ring) counter is fed to a digital-to-analog (D/A) converter as shown in Fig. 65 below. Assume all the states of the counter to be unset initially. The waveform which represents the D/A converter output V_0 is

66) Two D flip-flops are connected as a synchronous counter that goes through the

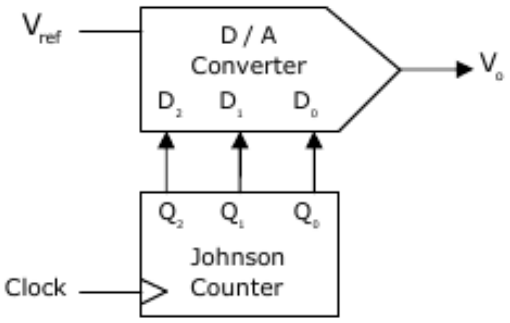


Fig. 65

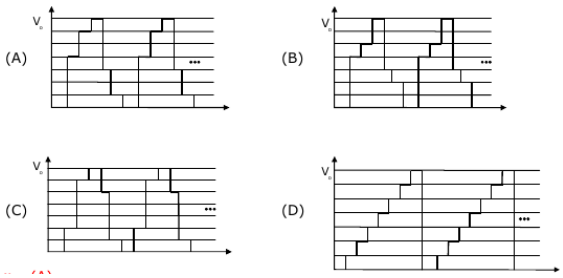


Fig. 65

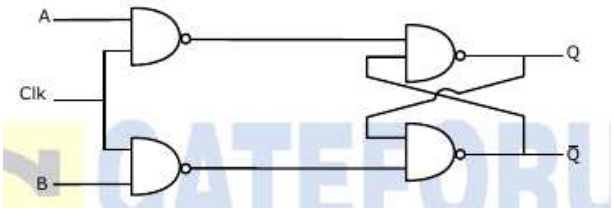


Fig. 68

following Q_BQ_A sequence $00 \rightarrow 11 \rightarrow 01 \rightarrow 10 \rightarrow 00 \rightarrow ...$
The combination to the inputs D_A and D_B are

(a) $D_A = \overline{Q_B}; D_B = \overline{Q_A}$
(b) $D_A = \overline{Q_A}; D_B = \overline{Q_B}$
(c) $D_A = (Q_A\overline{Q_B} + \overline{Q_A}Q_B); D_B = \overline{Q_A}$
(d) $D_A = (Q_AQ_B + \overline{Q_A}\overline{Q_B}); D_B = \overline{Q_B}$

67) The output Y of a 2-bit comparator is logic 1 whenever the 2-bit input A is greater than the 2-bit input B. The number of combinations for which the output is logic 1, is

(a) 4
(b) 6
(c) 8
(d) 10

68) Consider the given circuit in Fig. 68. In this circuit, the race around

(a) does not occur
(b) occurs when $CLK = 0$
(c) occur when $CLK = 1$ and $A = B = 1$
(d) occurs when $CLK = 1$ and $A = B = 0$

69) The state transition diagram for the logic

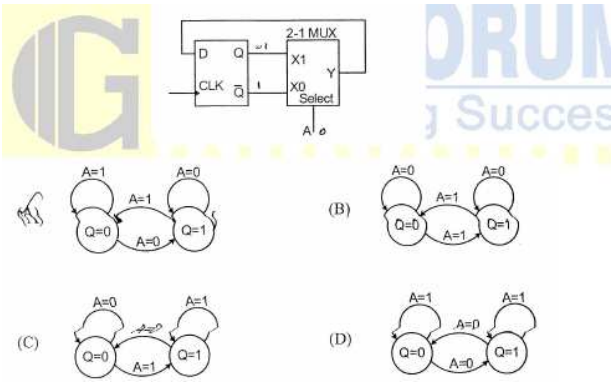


Fig. 69

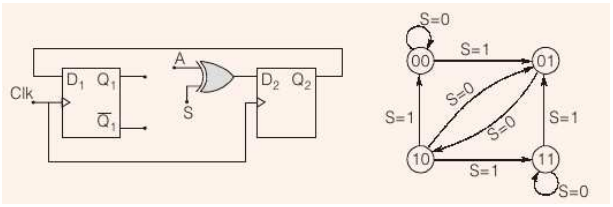


Fig. 70

circuit shown in Fig. 69 is

70) In the given circuit in Fig. 70, if A is connected to Q_1, the operation of the circuit is according to the state diagram. If XOR is replaced with XNOR, then to get the same operation of the circuit which of the following changes has to be done

(a) A should be connected to $\overline{Q_1}$
(b) A should be connected to Q_2
(c) A should be connected of Q_1 and S is replaced $\overline{S}$ to $\overline{Q_1}$
(d) A should be connected to $\overline{Q_1}$ by S is replaced by $\overline{S}$

71) The input frequency for the given counters $1MHz$, the output frequency observes at Q_4 is _____

72) For the circuit given, if the clock frequency is 1 kHz, then the frequency of output at Q_3 is Hz _____

73) Consider the multiplexer based logic ckt. in Fig. 73 Find the boolean function = ?

(a) $f = w\overline{S_1}\ \overline{S_2}$

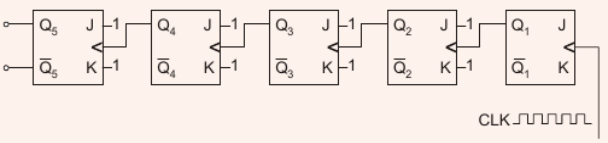


Fig. 71

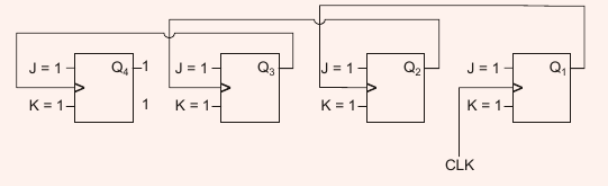


Fig. 72

(b) $f = wS_1 + wS_2 + S_1S_2$
(c) $f = \overline{w} + S_1 + S_2$
(d) $w \oplus S_1 \oplus S_2$

74) Current option is
(a) JK flip-flop
(b) SR flip-flop
(c) D flip-flop
(d) Master-slave arrangement

75) Find the output
y = _____
(a) $w'x'y + wx'y$
(b) $wxy + wx'y'$
(c) $w'x'y' + xw'y + xyw$
(d) none

76) Assume that all the digital gates in the circuit shown in the Fig. 76 are ideal, the

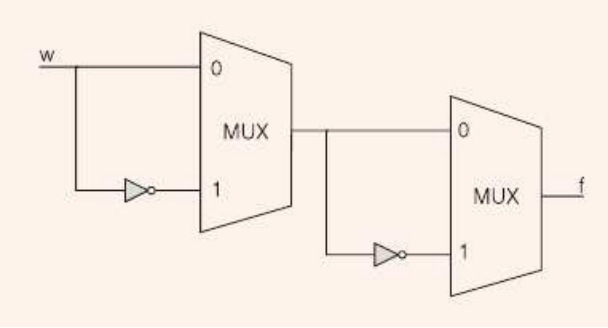


Fig. 73

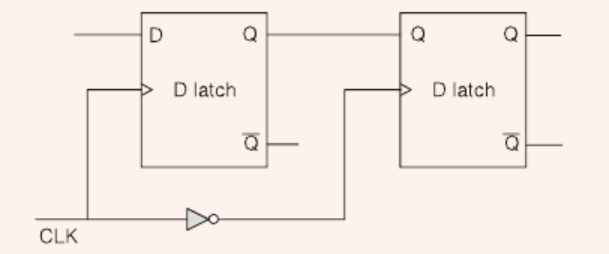


Fig. 74

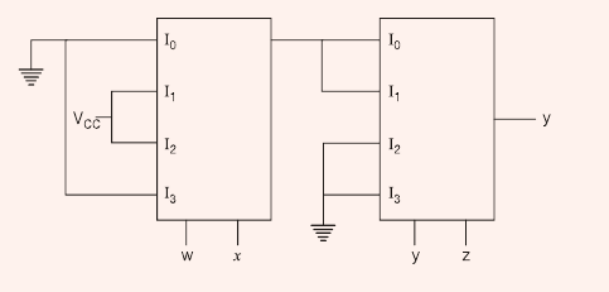


Fig. 75

resistor $R = 10\ k\Omega$ and the supply voltage is $5V$. The D flip-flops D_1, D_2, D_3, D_4, and D_5 are initialized with logic values $0, 1, 0, 1$ and 0, respectively. The clock has a 30% duty cycle.
The average power dissipated (in mW) in the resistor R is _____

77) The 4 : 1 multiplexer in Fig. 77 is to be used for generating the output carry of a full adder. A and B are the bits to be added while C_{in} is the input carry and C_{out} is the output carry. A and B are to be used as the select bits with A being the more significant select bit.
Which one of the following statements

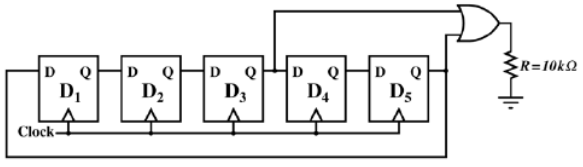


Fig. 76

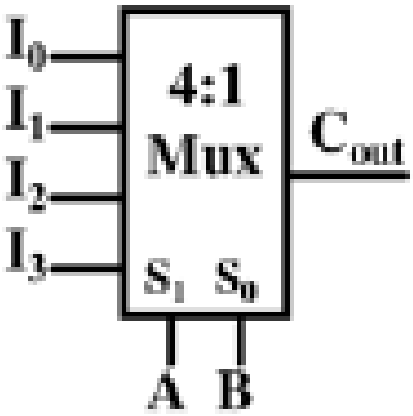


Fig. 77

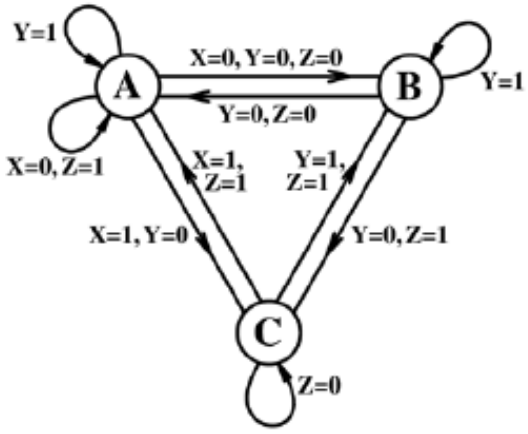


Fig. 78

correctly describes the choice of signals to be connected to the inputs I_0, I_1, I_2 and I_3 so that the output is C_{out} ?

(a) $I_0 = 0, I_1 = C_{in}, I_2 = C_{in}$ and $I_3 = 1$
(b) $I_0 = 1, I_1 = C_{in}, I_2 = C_{in}$ and $I_3 = 1$
(c) $I_0 = C_{in}, I_1 = 0, I_2 = 1$ and $I_3 = C_{in}$
(d) $I_0 = 0, I_1 = C_{in}, I_2 = 1$ and $I_3 = C_{in}$

78) The state transition diagram for a finite state machine with states A, B and C, and binary inputs X, Y and Z, is shown in Fig. 78.
Which one of the following statements is correct?

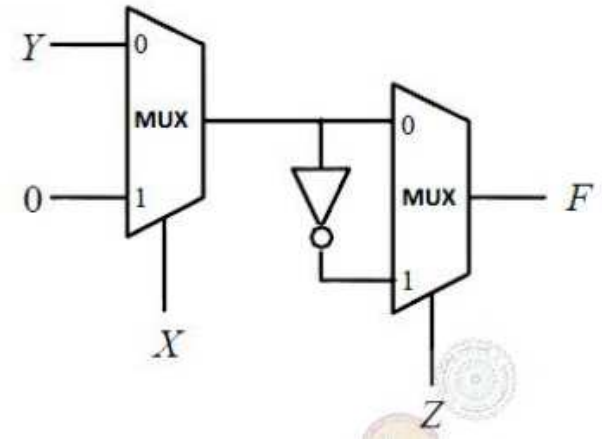


Fig. 79

(a) Transitions from State A are ambiguously defined.
(b) Transitions from State B are ambiguously defined.
(c) Transitions from State C are ambiguously defined.
(d) All of the state transitions are defined unambiguously.

79) Consider the circuit shown in the Fig. 79. The Boolean expression F implemented by the circuit is

(a) $\overline{X}\ \overline{Y}\ \overline{Z} + X\ Y + \overline{Y}\ Z$
(b) $\overline{X}\ Y\ \overline{Z} + X\ Z + \overline{Y}\ Z$
(c) $\overline{X}\ Y\ \overline{Z} + X\ Y + \overline{Y}\ Z$
(d) $\overline{X}\ \overline{Y}\ \overline{Z} + X\ Z + \overline{Y}\ Z$

80) The state diagram of a finite state machine (FSM) designed to detect an overlapping sequence of three bits is shown in the Fig. 80. The FSM has an input 'In' and an 'Out'. The initial state of the FSM is S_0. If the input sequence is 10101101001101, starting with the left-most bit, then the number of times 'Out' will be 1 is

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81) In Fig. 81, Figure I shows a 4-bit ripple carry adder realized using full adders and Figure II shows the circuit of a full-adder(FA). The propagation delay of the

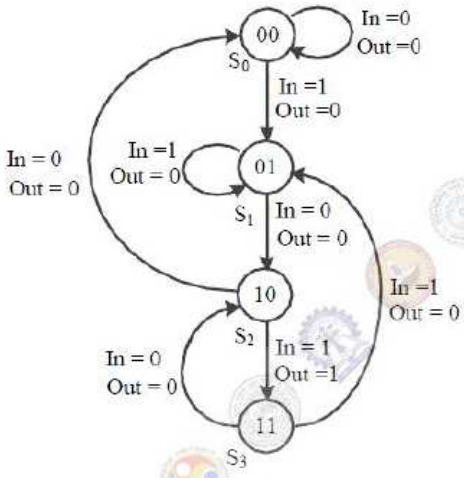

Fig. 80

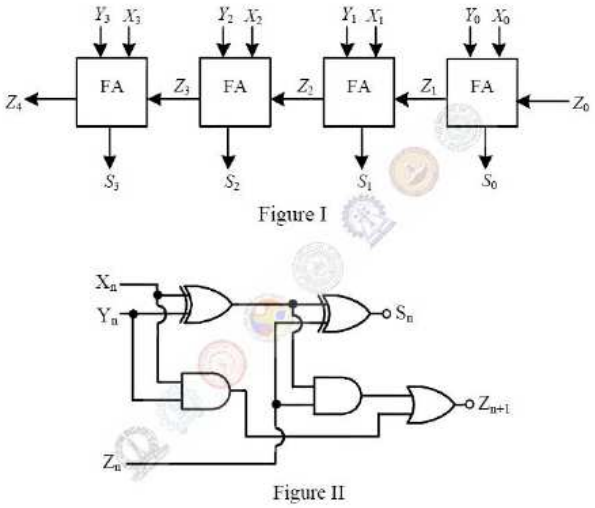

Fig. 81

XOR, AND and OR gates in Figure II are 20 ns, 15 ns and 10 ns,respectively. Assume all the inputs to the 4-bit adder are initially reset to 0.

At t = 0,the inputs to the 4-bit adder are changed to $X_3X_2X_1X_0$ = 1100, $Y_3Y_2Y_1Y_0$ = 0100 and Z_0 = 1. The output of the ripple carry adder will be stable at $t(in\ ns)$ =

82) A four-variable Boolean function is realized using 4×1 multiplexers as shown in

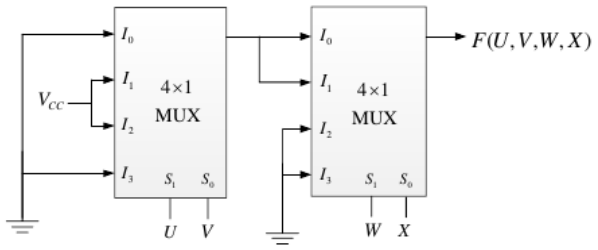

Fig. 82

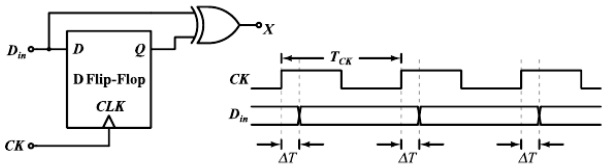

Fig. 83

the Fig. 82.

The minimized expression for $F(U, V, W, X)$ is

(a) $(UV + \overline{U}\ \overline{V})\overline{W}$

(b) $(UV + \overline{U}\ \overline{V})(\overline{W}\ \overline{X} + \overline{W}X)$

(c) $(U\overline{V} + \overline{U}V)\overline{W}$

(d) $(U\overline{V} + \overline{U}V)(\overline{W}\ \overline{X} + \overline{W}X)$

83) In the circuit shown below, a positive edge-triggered D Flip-Flop is used for sampling input data D_{in} using clock CK. The XOR gate outputs 3.3 volts for logic HIGH and 0 volts for logic LOW levels.The data bit and clock periods are equal and the value of $\Delta T/T_{CK}$ = 0.15, where the parameters ΔT and T_{CK} are shown in the Fig. 83. Assume that the Flip-Flop and the XOR gate are ideal.

If the probability of input data bit (D_{in}) transition in each clock period is 0.3, the average value (in volts, accurate to two decimal places) of the voltage at node X, is _____