Digital Calculator

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Contents

***Abstract*—This manual shows how to design a 4-bit calculator using the principles of digital design.**

1 Combinational Logic

1.1 Display Decoder

Table 1.1 is the truth table for the display decoder in Fig. 1.1.

Problem 1.1. Use K-maps to obtain the minimized expressions for a, b, c, d, e, f, g in terms of A, B, C, D with and without don't care conditions.

1.2 Adder

Problem 1.2. Find the logic for the outputs in Table 1.2.

1.3 Adder

Problem 1.3. Find the logic for the outputs in Table 1.3.

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D	C	B	A	a	b	c	d	e	f	g	Decimal
0	0	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	0
0	0	0	1	**1**	**0**	**0**	**1**	**1**	**1**	**1**	1
0	0	1	0	**0**	**0**	**1**	**0**	**0**	**1**	**0**	2
0	0	1	1	**0**	**0**	**0**	**0**	**1**	**1**	**0**	3
0	1	0	0	**1**	**0**	**0**	**1**	**1**	**0**	**0**	4
0	1	0	1	**0**	**1**	**0**	**0**	**1**	**0**	**0**	5
0	1	1	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	6
0	1	1	1	**0**	**0**	**0**	**1**	**1**	**1**	**1**	7
1	0	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	8
1	0	0	1	**0**	**0**	**0**	**1**	**1**	**0**	**0**	9

TABLE 1.1: Truth table for display decoder.

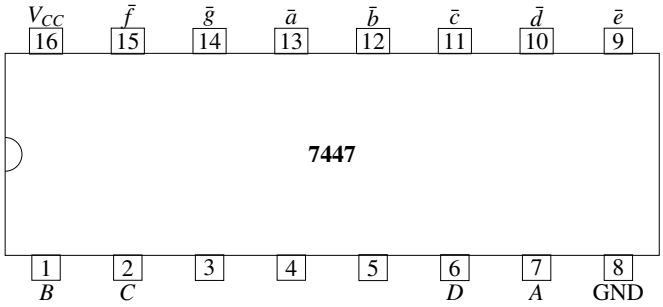

Fig. 1.1: The display decoder

1.4 MUX

Problem 1.4. Obtain the logic for the outputs in Table 1.4. **d** are the don't care conditions.

1.5 Comparator

Problem 1.5. Obtain the logic for the outputs in Table 1.5.

Input			Output	
a	**b**	$\mathbf{c_{in}}$	**s**	$\mathbf{c_{out}}$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

TABLE 1.2: The full adder

Input			Output	
a	**b**	$\mathbf{c_{in}}$	**s**	$\mathbf{c_{out}}$
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

TABLE 1.3: The full subtractor

Input			Output
I_0	I_1	**S**	**Y**
0	d	0	0
1	d	0	1
d	0	1	0
d	1	1	1

TABLE 1.4: Multiplexer

Input		Output
a	**b**	**Y**
0	0	0
0	1	1
1	0	0
1	1	0

TABLE 1.5: Comparator

2 Sequential Logic

2.1 D Flip Flop

Problem 2.1. The following cirucit in Fig. 2.1 is known as an S-R latch has two outputs Q and QN. The inputs are R and S.

1) Generate the i/o function table for this circuit
2) Can you think of any application for this circuit?

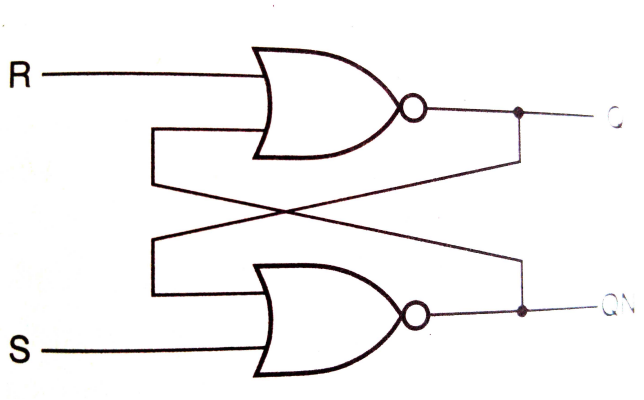

Fig. 2.1: S-R Latch

Problem 2.2. This problem depends on the previous problem.

1) Design an S-R latch with an enable.
2) Write the function table for this circuit.
3) Can you think of any problems that you may encounter with the S-R latch with an enable?
4) Now let $R = \bar{S}$. Comment.

Problem 2.3. The circuit in Fig. 2.3 comprises of two D-latches in cascade. C is the enable for the latch. The two waveforms shown below in 2.3 are the D input to the first latch and a periodic waveform CLK. (I know that it doesn't look like one).

1) Sketch the output (Q of second latch) waveform.
2) What is the most striking feature of the circuit?

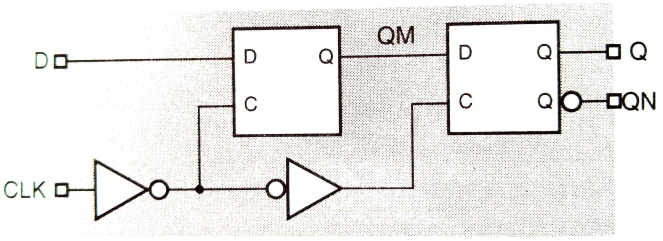

Fig. 2.3: The D-Flip Flop

2.2 Multiplier

Problem 2.4. Find 1011×1101 in binary and verify the result with their decimal equivalents.

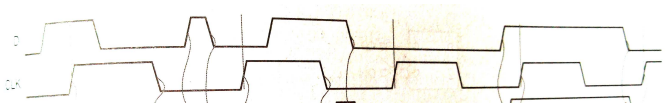

Fig. 2.3: Waveforms

2.3 Exercises

Use an arduino along with seven segment displays and shift registers for the following.

Problem 2.5. Verify all combinational logic in this manual on hardware.

Problem 2.6. Implement a 4 - bit adder.

Problem 2.7. Implement a 4 - bit subtractor.

Problem 2.8. Implement a 4 - bit multiplier.