GATE Exercises on ATMEGA328P

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***Abstract*—This problem set has questions taken from GATE papers over the last twenty years suitably modified for the ATMEGA328P microcontroller, present in the Arduino Uno. Teachers can use the problem set for course tutorials and labs.**

1) The clock frequency of an 8085 microprocessor is 5 MHz.If time required to execute an instruction is 1.4 μ s,then number of T states needed for executing the instruction is
   a) 1
   b) 6
   c) 7
   d) 8
2) The following five instructions were executed on 8085 microprocessor.

```
MVI A,33H
MVI B,78H
ADD B
CMA
ANI 32H
```

   The Accumulator value immediately after the execution of the fifth instruction is
   a) 00H
   b) 10H
   c) 11H
   d) 32H
3) In an 8085 system, a PUSH operation requires more clock cycles than a POP operation. Which one of the following options is the correct reason for this?
   a) For POP, the data transceivers remain in the same direction as for instruction fetch (memory to processor), whereas for PUSH their direction has to be reversed.
   b) Memory write operations are slower than memory read operations in an 8085 based system.
   c) The stack pointer needs to be pre-decremented before writing registers in a PUSH, whereas a POP operation uses the address already in the stack pointer.
   d) Order of registers has to be interchanged for a PUSH operation, whereas POP uses their natural order.
4) In an 8085 microprocessor, the shift registers which store the result of an addition and the overflow bit are, respectively
   a) B and F
   b) A and F
   c) H and F
   d) A and C
5) For 8085 microprocessor, following code executed

```
MVI A,05H
MVI B,05H
PTR:ADD B
DCR B
JNZ PTR
ADI 03H
HLT
```

   At the end of program,accumulator contains
   a) 17H
   b) 20H
   c) 23H
   d) 05H
6) An 8085 assembly language program is given below. Assume that the carry flag is initially unset.The content of the accumulator after the execution of the program is

```
MVI A,07H
RLC
MOV B,A
RLC
RLC
ADD B
```

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a) 8CH
b) 46H
c) 23H
d) 15H

7) In an microprocessor, the service routine for a certain interrupt starts from a fixed location of memory which cannot be externally set ,but the interrupt can be delayed or rejected .such interrupt is
   a) non-maskable and non-vectored
   b) maskable and non-vectored
   c) non-maskable and vectored
   d) maskable and vectored
8) The number of memory cycles required to execute the following 8085 instructions.
   I. LDA 3000H
   II. LXI D, FOF 1H
   would be
   a) 2 for I and 2 for II
   b) 4 for I and 3 for II
   c) 3 for I and 3 for II
   d) 3 for I and 4 for II
9) The 8255 Programmable Peripheral Interface is used as described below.
   I. An A/D converter is interfaced to a microprocessor through an 8255. the conversion is initiated by a signal from the 8255 on Port C. A signal on Port C causes data to be strobed into Port A.
   II. Two computers exchange data using a pair of 8255s. Port A works as a bidirectional data port supported by appropriate handshaking signals.
   would be
   The appropriate modes of operation of the 8255 for I and II would be
   a) Mode 0 for I and Mode 1 for II
   b) Mode 1 for I and Mode 0 for II
   c) Mode 2 for I and Mode 0 for II
   d) Mode 2 for I and Mode 1 for II
10) Consider the sequence of 8085 instructions given below.

```
LXI H, 9258
MOV A, M
CMA
MOV M, A
```

   Which one of the following is performed by this sequence?
   a) contents of location 9258 are moved to the accumulator
   b) contents of location 9258 are compared with the contents of the accumulator
   c) contents of location 9258 are complemented and stored in location 9258
   d) contents of location 5892 are complemented and stored in location 5892
11) In an 8085 microprocessor, the instruction CMP B has been executed while the content of the accumulator is less than that of register B. As a result?
   a) Carry flag will be set but Zero flag will be reset
   b) Carry flag will be reset but Zero flag will be set
   c) Both Carry flag and Zero flag will be reset
   d) Both Carry flag and Zero flag will be set
12) The number of hardware interrupts (which require an external signal to interrupt) present in an 8085 microprocessor are
   a) 1
   b) 5
   c) 4
   d) 13
13) In the 8085 microprocessor, the RST6 instruction transfers the program execution to the following location
   a) 30 H
   b) 24 H
   c) 48 H
   d) 60 H
14) An 8085 executes the following instructions.

```
2710 LXI H, 30A0H
2713 DAD H
2714 PCHL
```

   All addresses and constants are in Hex. Let PC be the contents of the program counter and HL be the contents of the HL register pair just after executing PCHL. Which of the following statements is correct?
   a) PC=2715H HL=30A0H
   b) PC=30A0H HL=2715H
   c) PC=6140H HL=6140H
   d) PC=6140H HL=2715H
15) For a microprocessor system using I/O mapped

I/O the following statement(s) is NOT true

a) Memory space available is greater.
b) Not all data transfer instruction are available.
c) I/O and Memory address spaces are distinct.
d) I/O address space is greater.

16) In an 8085 microprocessor system,the RST instruction will cause an interrupt
a) Only if an interrupt service routine is not being executed.
b) Only if a bit in the interrupt mask is made 0.
c) Only if interrupts have been enabled by an EI instruction.
d) None of the above.

17) A snapshot of the address, data and control buses of an 8085 microprocessor executing program is given below:

Address	2020*H*
Data	24*H*
$\overline{M}$	*Logichigh*
$\overline{RD}$	*Logichigh*
$\overline{WR}$	*LogicLow*

The assembly language instruction being executed is

a) IN 24H
b) OUT 24H
c) IN 20H
d) OUT 20H

18) An 8Kx8 bit RAM is interfaced to an 8085 microprocessor. In a fully decoded scheme, if the address of the last memory location of this RAM is 4FFFH, the address of the first memory location of the RAM will be
a) 1000H
b) 2000H
c) 3000H
d) 4000H

19) The following is an assembly language program for 8085 microprocessors

Address	*Instructioncode*	*Mnemonic*
1000*H*	3*E*06	*MVIA*, 06*H*
1002*H*	*C*670	*ADI*70*H*
1004*H*	320710	*STA*1007*H*
1007*H*	*AF*	*XRAA*
1008*H*	76	*HLT*

When this program halts, the accumulator contains
a) 00H
b) 06H
c) 70H
d) 76H

20) A part of a program written for an 8085 microprocessor is shown below. When the program execution reaches LOOP2, the value of register C will be

```
SUB A
MOV C, A
LOOP1: INR A
DAA
JC LOOP2
JNC LOOP1
LOOP2: NOP
```

a) 63H
b) 64H
c) 99H
d) 100H

21) A 2k8 bit RAM is interfaced to an 8-bit microprocessor. If the address of the first memory location in the RAM is 0800H, the address of the last memory location will be
a) 1000H
b) 0FFFH
c) 4800H
d) 47FFH

22) Find the correct match among the following pair in the context of an 8085 microprocessor :

(*a*)*DAA*	(*e*)*Programcontrolinstruction*
(*b*)*LXI*	(*f*)*DatamovementInstruction*
(*c*)*RST*	(*g*)*Interruptinstruction*
(*d*)*JMP*	(*h*)*Arithmeticinstruction*

a) a-e, b-f, c-g, d-h
b) a-h, b-g, c-f, d-e
c) a-h, b-f, c-g, d-e
d) a-f, b-h, c-g, d-e

23) The subroutine SBX given below is executed by an 8085 processor. The value in the accumulator immediately after the execution of the subroutine will be:

```
SBX : MVI A,99H
ADI 11H
MOV C,A
RET
```

a) 00H
b) 11H
c) 99H
d) AAH

24) In an 8085 processor, the main program calls the subroutine SUB1 given below. When the program returns to the main program after executing SUB1, the value in the accumulator is

Address	*OpcodeMnemonics*
2000	3*E*00
2002	*CD*0520
2005	3*C*
2006	*C*9

```
SUB1:MVI A,00H
CALL SUB2
SUB2:INR A
RET
```

a) 00
b) 01
c) 03
d) 04

25) Consider a system consisting of a microprocessor, memory, and peripheral devices connected by a common bus. During DMA data transfer, the microprocessor
a) only read from the bus.
b) only write to the bus.
c) both read from and writes to the bus.
d) neither read from nor writes to the bus.

26) A memory mapped I/O device has an address of 00F0H. Which of the following 8085 instructions outputs the content of the accumulat or to the I/O device?
a) LXI H, 00F0H , MOV M, A
b) LXI H, 00F0H , OUT F0H
c) LXI H, 00F0H, OUT M
d) LXI H, 00F0H , MOV A, M

27) An 8085 assembly language program is given as follows. The execution time of each instruction is given against the instruction in terms of T-state.

Instruction	$T-states$
$MVIB, 0AH$	$7T$
$LOOP: MVIC, 05H$	$7T$
$DCRC$	$4T$
$DCRB$	$4T$
$JNZLOOP$	$10T/7T$

The execution time of the program in terms of T states is
a) 247 T
b) 254 T
c) 250 T
d) 257 T

28) The time period of a square wave in the audio frequency range is measured using an 8085 microprocessor by feeding the square wave to one of the four interrupts, namely, RST 7.5, RST 6.5, RST 5.5, or INT. The algorithm used starts a timer at the beginning of a time period, stops the timer at the beginning of the next time period and reads the timer values for time measurement. Which of the following interrupts should be selected for this application?
a) INTR
b) RST 6.5
c) RST 5.5
d) RST 7.5

29) In an 8085 microprocessor, which one of the following is the correct sequence of the machine cycles for the execution of the DCR M instruction?
a) op-code fetch.
b) op-code fetch, memory read, memory write.
c) op-code fetch memory read.
d) op-code fetch memory write, memory write.

30) In an 8085 microprocessor the value of the stack pointer (SP) is 2010H and that of DE register pair is 1234H before the following code is executed. The value of the DE register pair after the following code is executed is

```
LXI H, 0000H
PUSH H
PUSH H
POP B
DAD SP
XCHG
```

a) 200EH
b) 2010H
c) 200CH
d) 1232H

31) The vectored address corresponding to the software interrupt command RST7 in 8085 microprocessor is
a) 0017H

b) 0038H
c) 0700H
d) 0027H

32) The following 8085 instructions are executed sequentially.

```
PROG: XRA A
      MOV L, A
      MOV H, L
      INX H
      DAD H
```

After execution, the content of HL register pair is

a) 0000H
b) 0001H
c) 0002H
d) 0101H

33) In an 8085 system containing 8KB of ROM and 8KB of RAM , the ROM is selected when A 15 is 0 and the RAM is selected when A15 is 1. A13 and A14 are unused. The CPU executes the following program

```
MVI A,00H
STA 8080H
DCR A
STA C080H
RET
```

The content of memory location 8080 H after the execution of the RETURN instruction is

a) FFH
b) FEH
c) 00H
d) 01H

34) In an INTEL 8085 microprocessor the ADDRESS-DATA bus and the DATA bus are

a) Non multiplexed
b) Duplicated
c) Multiplexed
d) Same as CONTROL bus

35) A minimal microcomputer system is constructed using INTEL 8085 microprocessor, an 8156 RAM and an 8355 ROM. The chip enable CE of 8156 and chip enable CE of 8355 are connected to the address line. A12 of 8085. The address of port A of the 8156 chip is

a) 21H
b) 11H
c) 12H
d) 20H

36) In a microprocessor with 16 address and 12 data lines, the maximum number of opcodes is

a) 2^6
b) 2^{12}
c) 2^8
d) 2^{16}

37) An m-bit microprocessor has an m-bit

a) flag register
b) data register
c) instruction register
d) program counter

38) In 8085 microprocessor, CY flag may be set by the instruction

a) SUB
b) CMA
c) INX
d) ANA

39) Microprocessor 8085 regains control of the bus

a) immediately after HOLD goes low.
b) immediately after HOLD goes high.
c) after half-clock cycle after HLDA goes low.
d) after half-clock cycle after HLDA goes high.

40) If the following program is executed in a microprocessor, the number of instruction cycles it will take from START TO HALT is

```
START MVI A, 14 H
SHIFT RLC
JNZ SHIFT
HALT
```

a) 4
b) 8
c) 13
d) 16

41) Which one of the following is not a vectored interrupt?

a) TRAP
b) RST7.5
c) INTR
d) RST3

42) The following program is written for an 8085 microprocessor to add two bytes located at memory addresses 1FFE and 1FFF

```
LXI H, 1FFE
```

```
MOV B, M
INR L
MOV A, M
ADD B
INR L
MOV M, A
XOR A
```

On completion of the execution of the program, the result of addition is found

a) in the register A
b) at the memory address 1000
c) at the memory address 1F00
d) at the memory address 2000

43) In an 8085 microprocessor ,the following program executed

Address	*Instructioncode*
2000*H*	*XRAA*
2001*H*	*MVIB*, 04*H*
2003*H*	*MVIA*, 03*H*
2005*H*	*RAR*
2006*H*	*DCRB*
2007*H*	*JNZ*2005
200*AH*	*HLT*

At the end of program ,register A contains

a) 60H
b) 30H
c) 06H
d) 03H

44) In an 8085 microprocessor, the contents of the Accumulator, after the following instructions are executed will become

```
XRA A
MVIB F0H
SUB B
```

a) 01H
b) F0H
c) 10H
d) 0FH

45) An input device is interfaced with Intel 8085A microprocessor as memory mapped I/O. The address of the device is 2500H. In order to input data from the device to accumulator, the sequence of instructions will be

a) LXI H, 2500H ;MOV A, M
b) LHLD 2500H;MOV A, M
c) LXI H, 2500H ;MOV M, A
d) LHLD 2500H;MOV M, A

46) The contents (in Hexadecimal) of some of the memory locations in an 8085A based system are given below

Address	*Contents*
....	....
26*FE*	00
26*FF*	01
2700	02
2701	03
2702	04
....	....

The contents of stack pointer (SP), Program counter(PC) and (H, L) are 2700H, 2100H and 0000H respectively. When the following sequence of instructions are executed,

```
2100 H: DAD SP
2101 H: PCHL
```

the contents of (SP) and (PC) at the end of execution will be

a) (PC) = 2102H, (SP) = 2700H
b) (PC) = 2800H, (SP) = 26 FE H
c) (PC) = 2700H, (SP) = 2700H
d) (PC) = 2A02H, (SP)= 2702H

47) Which one of the following statements regarding the INT (interrupt) and the BRQ (bit request) pins in a CPU is true?

a) The BRQ pin is sampled after every instruction cycle, but the INT is sampled after every machine cycle.
b) Both INT and BRQ are sampled after every machine cycle.
c) The INT pin is sampled after every instruction cycle, but the BRQ is sampled after every machine cycle.
d) Both INT and BRQ are sampled after every instruction cycle.

48) If the operating frequency of 8086 microprocessor is 10MHz and ,if for the given instruction ,the machine cycle consist of 4 T states ,what will be the time taken by

the machine cycle to complete execution of same instruction when three waits states are inserted ?

a) 0.4μs
b) 0.7μs
c) 70μs
d) 7μs

49) consider the following loop

```
   MOV CX, 8000H
L1:DEC CX
   JNX L1
```

The processor is running at 14.7456/3 MHz and DEC CX require two clock cycles and JNZ requires 16 clock cycles .The total time taken is nearly

a) 0.01s
b) 0.12s
c) 3.66s
d) 4.19s

50) An Addressing mode in which the location of the data is obtained within the mnemonics,is known as
a) Immediately addressing mode.
b) Implied addressing mode.
c) Register addressing mode.
d) Direct addressing mode.

51) In microprocessor, WAIT states are used to
a) Make the processor WAIT during a DMA operation.
b) Make the processor WAIT during an Interrupt operation .
c) Make the processor WAIT during a Power shut Down.
d) Direct addressing mode.