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Abstract—This manual shows how to manage clocks in arm using STM32F103C8T6.

1 COMPONENTS

Component	Value	Quantity
Breadboard		1
Resistor	220 Ω	1
STM32F103C8T6		1
Seven Segment Display	Common Anode	1
Jumper Wires		20

TABLE 1.0: Components

Problem 1.1. List all available clocks in the STM32F103C8T6 blue pill.

Solution: See Table 1.1.

Clock	Location	Type	Frequency
HSI	Internal	RC	8Mhz
LSI	Internal	RC	32.768 kHz
HSE	External	Crystal	8Mhz

TABLE 1.1: STM32F103C8T6 Clock Types

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Problem 1.2. Make connections as shown in Table 1.2.

STM32	Seven Segment Display
3.3V	COM (through resistor)
PA1	DOT

TABLE 1.2: Pin Connections

1.1 HSE

Problem 1.3. Execute the following program

```
https://github.com/gadepall/
STM32F103C8T6/blob/master/
examples/clocks/
hse_systick_blink.c
```

Problem 1.4. Explain the following instruction

```
RCC->CR =0x00010000 ;
```

Solution: Fig. 1.4 shows the RCC->CR register. The above instruction enables the HSE crystal, which is 8 MHz for the STM32F103C8T6.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						PLL RDY	PLLON	Reserved				CSS ON	HSE BYP	HSE RDY	HSE ON
						r	rw					rw	rw	r	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSICAL[7:0]								HSITRIM[4:0]				Res.	HSI RDY	HSION	
r	r	r	r	r	r	r	r	rw	rw	rw	rw		r	rw	

Fig. 1.4: RCC Clock Control Register (RCC->CR)

Problem 1.5. Explain the following instruction

```
RCC->CFGR =0x00000001 ;
```

Solution: Fig. 1.5 shows the RCC->CFGR register. The above instruction makes the HSE as the system clock through SW = 01.

Problem 1.6. Verify that HSE is the system clock by checking that SWS = 01.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					MCO[2:0]			Res.	USB PRE	PLLMUL[3:0]				PLL XTPRE	PLL SRC
					rw	rw	rw		rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCPRE[1:0]		PPRE2[2:0]			PPRE1[2:0]			HPRE[3:0]			SWS[1:0]		SW[1:0]		
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	r	r	rw	rw

Fig. 1.5: RCC clock Configuration Register (RCC->CFGR)

2 PLL

Problem 2.1. Make the PLL as the system clock.

Solution:

```
RCC->CFGR =0x00000010;
```

Problem 2.2. Choose the PLL input as HSE.

```
RCC->CFGR =0x00010010;
```

Problem 2.3. Enable PLL

Solution:

```
RCC->CR =0x01010000;
```

Problem 2.4. Execute the following code.

```
https://github.com/gadepall/
STM32F103C8T6/blob/master/
examples/clocks/
pll_systick_blink.c
```

Problem 2.5. Make the PLL output = 24 MHz.