Research Proposal

1 Proposal Summary

A. Project title : Simulation and performance evaluation of Equalizer and Synchronization algorithms for Narrow band Modem

B. Nodal Institution : Indian Institute of Technology Hyderabad

C. Funding Agency : Bharat Electronics Limited

D. Principal Investigator : Dr. GVV Sharma
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E. Total Estimated Cost : ₹. 8,07,120/- (inclusive of GST@18%)

F. Duration : 3 months

G. Details of Budget :

S.No	Head	Cost (₹)
1	Man power	520000
2	Hardware/Software	
3	Contingency	
4	Consumables	
5	Travel	50000
6	**Total**	570000
7	Institute overhead cost (20% of project cost)	114000
8	Gross Total	684000
9	State GST (9% of overall cost)	61560
10	Central GST (9% of overall cost)	61560
11	**Grand Total**	**807120**

2 Specifications

To develop a robust equalizer with time/frequency synchronization at the receiver to sustain fading effects of V/UHF channel as per the specifications in Table I

Parameter	Value
Hardware	ARTIX-7 A200T FPGA based baseband card (Available at CRL)
MODEM	8PSK-TCM (Implemented in CRL)
Modem Rate	555Kbps (CRL)
SNR	7.6 db at 1e5 (simulations done in CRL)
Channel (V/UHF)	30Mhz - 512Mhz
Bandwidth	250khz
Bit Duration	2.7us
Throughput	100kbps (Throughput at application Layer)
Ramp up time	116 us (Junk symbols will be sent)
Propagation Delay	100 us (Junk symbols will be sent)
Training sequence	421.2us(provided time for training sequence)
Frame Slot	2 ms
Frame SOM	8 bytes
Payload	32 bytes (692 us)

TABLE I

3 List of Tasks and Deliverables

1) Simulation of suitable Preamble detection algorithm.
2) Simulation of suitable channel estimation and equalization algorithms for mitigating Rayleigh fading channel effects.
3) Simulation of suitable timing and frequency algorithms for narrow band waveform (coherent TCM-8PSK). Convergence of timing, frequency and equalization algorithms in limited preamble symbols provided (19.5 bytes which is equal to 156 bits or 78 symbols for BEL TCM 8PSK modulation) and efficient utilization of hardware resources (required all these algorithms shall take max 40% of FPGA resources).
4) Performance evaluation and Simulation of equalizer and synchronization algorithms should to be done in fixed point with BEL Modem.
5) MATLAB codes delivered to CRL should be hardware implementable and consider FPGA resources restrictions. Matrix inversions in MATLAB code should not be there.

4 Milestones and Payment

Relevant milestones and corresponding payment details are available in Table II.

5 Technology Overview

Preamble detection can be done using a special kind of correlation as in [1]. A symbol detection technique in the presence of time offsets is available in [2]. A correlation based technique for frequency offset estimation is provided in [3]. A DFSE based equalization technique based on the Viterbi algorithm is provided in [4]. A constant modulus decision directed algorithm is proposed in [5]. A channel impulse response based sparse equalization and synchronization technique is given in [6]. Blind equalization techniques are listed in [7].

Milestone	Deliverable	Time	Payment (₹)	Remarks
1	Basic Simulation for Preamble Detection	15 days	80712	10% of Overall Cost
2	Basic Simulation for Equalizer, Time and Frequency Synchronization	45 days	322848	40% of Overall cost
3	Hardware compatible MATLAB implementation	90 days	403560	Final Payment
	Total		**807120**	

TABLE II: Milestones 1 and 2 will be limited to proof of concept and finalizing suitable algorithms. Hardware compatibility will be guaranteed only in Milestone 3. Timelines applicable from the date of approval of the project.

All the above techniques will be analyzed before before finalizing the algorithms for preamble detection, synchronization and equalization.

References

[1] H. Miyashiro, E. Boutillon, C. Roland, J. Vilca, and D. Díaz, "Improved Multiplierless Architecture for Header Detection in DVB-S2 Standard," in *2016 IEEE International Workshop on Signal Processing Systems (SiPS)*, Oct 2016, pp. 248–253. [Online]. Available: https://doi.org/10.1109/SiPS.2016.51

[2] F. Gardner, "A BPSK/QPSK Timing-Error Detector for Sampled Receivers," *IEEE Transactions on Communications*, vol. 34, no. 5, pp. 423–429, May 1986. [Online]. Available: https://doi.org/10.1109/TCOM.1986.1096561

[3] M. Luise and R. Reggiannini, "Carrier frequency recovery in all-digital modems for burst-mode transmissions," *IEEE Transactions on Communications*, vol. 43, no. 2/3/4, pp. 1169–1178, Feb 1995. [Online]. Available: https://doi.org/10.1109/26.380149

[4] B. W. Peterson, D. R. Stephens, and W. H. Tranter, "DFSE equalization of dual-h CPM over UHF MILSATCOM channels," in *MILCOM 2002. Proceedings*.

[5] V. Anis, C. Delaosa, L. H. Crockett, and S. Weiss, "Energy-efficient implementation of a wideband transceiver system with per-band equalisation and synchronisation," in *2018 IEEE Wireless Communications and Networking Conference (WCNC)*, April 2018, pp. 1–6.

[6] J. Baek and J. Seo, "Improved CIR-Based Receiver Design for DVB-T2 System in Large Delay Spread Channels: Synchronization and Equalization," *IEEE Transactions on Broadcasting*, vol. 57, no. 1, pp. 103–113, March 2011.

[7] Chee-Siong Lee, S. Vlahoyiannatos, and L. Hanzo, "Satellite based turbo-coded, blind-equalized 4-QAM and 16-QAM digital video broadcasting," *IEEE Transactions on Broadcasting*, vol. 46, no. 1, pp. 23–33, March 2000.