

Robust equalizer with time/frequency synchronization at the receiver to sustain fading effects of V/UHF channel

G V V Sharma*

CONTENTS

1	Specifications	1
1.1	Specifications	1
1.2	Sequence of Steps	1
1.3	Technology Overview	1
2	Frame Synchronization	2
2.1	Frame Synchronization : Global Summation of SOF/PLSC Detectors	2
2.1.1	Global Threshold Calculation	2
2.2	Plots	3
	References	3

Abstract—This book provides an introduction to optimization based on the NCERT textbooks from Class 6-12. Links to sample Python codes are available in the text.

Download python codes using

```
svn co https://github.com/gadepall/school/trunk/ncert/optimization/codes
```

Parameter	Value
Hardware	ARTIX-7 A200T FPGA based baseband card
MODEM	8PSK-TCM
Modem Rate	555Kbps
SNR	7.6 db at 1e5
Channel (V/UHF)	30Mhz - 512Mhz
Bandwidth	250khz
Bit Duration	2.7us
Throughput	100kbps (Throughput at application Layer)
Ramp up time	116 us (Junk symbols will be sent)
Propagation Delay	100 us (Junk symbols will be sent)
Training sequence	421.2us(provided time for training sequence)
Frame Slot	2 ms
Frame SOM	8 bytes
Payload	32 bytes (692 us)

TABLE 0

1 SPECIFICATIONS

1.1 Specifications

To develop a robust equalizer with time/frequency synchronization at the receiver to sustain fading effects of V/UHF channel as per the specifications in Table 0

*The author is with the Department of Electrical Engineering, Indian Institute of Technology, Hyderabad 502285 India e-mail: gadepall@iith.ac.in. All content in this manual is released under GNU GPL. Free and open source.

1.2 Sequence of Steps

- 1) Simulation of suitable Preamble detection algorithm.
- 2) Simulation of suitable channel estimation and equalization algorithms for mitigating Rayleigh fading channel effects.
- 3) Simulation of suitable timing and frequency algorithms for narrow band waveform (coherent TCM-8PSK). Convergence of timing, frequency and equalization algorithms in limited preamble symbols provided (19.5 bytes which is equal to 156 bits or 78 symbols for TCM 8PSK modulation) and efficient uti-

lization of hardware resources (required all these algorithms shall take max 40% of FPGA resources).

- 4) Performance evaluation and Simulation of equalizer and synchronization algorithms should to be done in fixed point.
- 5) MATLAB codes should be hardware implementable and consider FPGA resources restrictions. Matrix inversions in MATLAB code should not be there.

1.3 Technology Overview

Preamble detection can be done using a special kind of correlation as in [1]. A symbol detection technique in the presence of time offsets is available in [2]. A correlation based technique for frequency offset estimation is provided in [3]. A DFSE based equalization technique based on the Viterbi algorithm is provided in [4]. A constant modulus decision directed algorithm is proposed in [5]. A channel impulse response based sparse equalization and synchronization technique is given in [6]. Blind equalization techniques are listed in [7].

All the above techniques will be analyzed before before finalizing the algorithms for preamble detection, synchronization and equalization.

2 FRAME SYNCHRONIZATION

2.1 Frame Synchronization : Global Summation of SOF/PLSC Detectors

Fig. 5 shows the Frame Structure for the communication system. Corresponding details are available

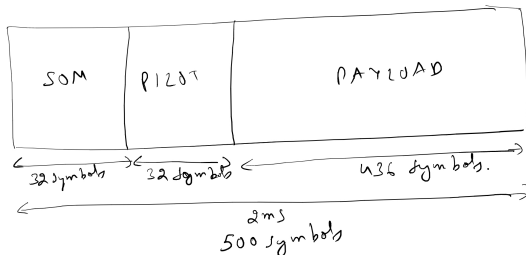


Fig. 5: Frame Structure

in Table 5 Let the frequency offset be Δf and phase

Head	Size (Bits)	Duration (us)
SOM	32	128
PILOT	32	128
PAYLOAD	436	1744
Total	500	2000

TABLE 5

offset be $\Delta\phi$. Then,

$$Y_k = X_k e^{j(2\pi\Delta f k M + \phi_k)} + V_k, \quad k = 1, \dots, N \quad (2.1.1)$$

assuming that no pilot symbols are transmitted. Let the phase information be θ_k , and defined as

$$e^{\theta(k)} = \frac{Y_k}{|Y_k|} \quad (2.1.2)$$

At the receiver, the header information is available in the form of

$$g_i(l) = x_s(l)x_s(l-i), \quad l = 0, \dots, SOF - 1 \quad (2.1.3)$$

$$h_i(l) = x_p(l)x_p(l-i), \quad l = 0, \dots, PLSC - 1 \quad (2.1.4)$$

where x_s are the mapped SOF symbols, x_p are the scrambled PLSC symbols, both modulated using 8-PSK for $i = 1, 2, 4, 8, 16, 32$. The SOM is chosen as a 64-bit length such that SOF and PLS each are of 32-bit length.

A special kind of correlation is performed to obtain

$$m_i(k) = \sum_{l=0}^{PLSC-1} e^{j(\theta(k-l) - \theta(k-l-i))} h_i(l), \quad (2.1.5)$$

$$n_i(k) = \sum_{l=0}^{SOF-1} e^{j(\theta(k-l) - \theta(k-l-i))} g_i(l), \quad (2.1.6)$$

$$k = 1, \dots, N \quad (2.1.7)$$

Compute

$$p_i(k) = \begin{cases} \max(|n_i(k - PLSC) + m_i(k)|, \\ |n_i(k - PLSC) - m_i(k)|) & k > PLSC \end{cases} \quad (2.1.8)$$

GLOBAL variable $G_{R,T}(k)$ [1] defined as,

$$G_{R,T}(k) = \sum_{i \geq 1} p_i(k), \quad i = 1, 2, 4, 8, 16, 32 \quad (2.1.9)$$

At the receiver, let us consider we have sent two types of transmission. One is PLHEADER+DATA

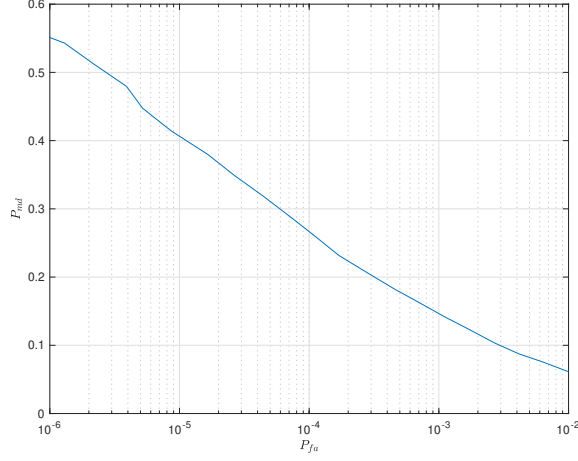


Fig. 5: Frame Synchronization Receiver Operating Characteristics (ROC)

(Y_{k1}) and another is only DATA (Y_{k2}) and the GLOBAL variables for (Y_{k1}) and (Y_{k2}) from (2.1.9) are $G1_{R,T}(k)$, $G2_{R,T}(k)$ respectively.

2.1.1 Global Threshold Calculation: The Global Threshold variable is defined as

$$T = \max(\max(G1_{R,T}(k)), \max(G2_{R,T}(k))) \quad (2.1.10)$$

The probability of false detection of plheader when only DATA frame (Y_{k2}) has been sent is defined as

$$P_{FA} = \frac{\sum \frac{\text{sign}(|Y_{k2}-T|)+1}{2}}{N} \quad (2.1.11)$$

The probability of missed detection of plheader when PLHEADER+DATA (Y_{k1}) has been sent is defined as

$$P_{MD} = \frac{\sum \frac{\text{sign}(T-|Y_{k1}|)+1}{2}}{N + PLSC + SOF} \quad (2.1.12)$$

2.2 Plots

Fig.5 shows the ROC curve (P_{FA} vs P_{MD}) at the receiver for frame synchronization at $\frac{E_b}{N_0} = -2$ dB and with a frequency offset of 250 KHz.

REFERENCES

[1] H. Miyashiro, E. Boutillon, C. Roland, J. Vilca, and D. Díaz, "Improved Multiplierless Architecture for Header Detection in DVB-S2 Standard," in *2016 IEEE International Workshop on Signal Processing Systems (SiPS)*, Oct 2016, pp. 248–253. [Online]. Available: <https://doi.org/10.1109/SiPS.2016.51>

[2] F. Gardner, "A BPSK/QPSK Timing-Error Detector for Sampled Receivers," *IEEE Transactions on Communications*, vol. 34, no. 5, pp. 423–429, May 1986. [Online]. Available: <https://doi.org/10.1109/TCOM.1986.1096561>

[3] M. Luise and R. Reggiannini, "Carrier frequency recovery in all-digital modems for burst-mode transmissions," *IEEE Transactions on Communications*, vol. 43, no. 2/3/4, pp. 1169–1178, Feb 1995. [Online]. Available: <https://doi.org/10.1109/26.380149>

[4] B. W. Peterson, D. R. Stephens, and W. H. Tranter, "DFSE equalization of dual-h CPM over UHF MILSATCOM channels," in *MILCOM 2002. Proceedings*.

[5] V. Anis, C. Delaosa, L. H. Crockett, and S. Weiss, "Energy-efficient implementation of a wideband transceiver system with per-band equalisation and synchronisation," in *2018 IEEE Wireless Communications and Networking Conference (WCNC)*, April 2018, pp. 1–6.

[6] J. Baek and J. Seo, "Improved CIR-Based Receiver Design for DVB-T2 System in Large Delay Spread Channels: Synchronization and Equalization," *IEEE Transactions on Broadcasting*, vol. 57, no. 1, pp. 103–113, March 2011.

[7] Chee-Siong Lee, S. Vlahoyiannatos, and L. Hanzo, "Satellite based turbo-coded, blind-equalized 4-QAM and 16-QAM digital video broadcasting," *IEEE Transactions on Broadcasting*, vol. 46, no. 1, pp. 23–33, March 2000.