# Simplified LLR calculation for DVB-S2 LDPC decoder

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***Abstract*—The computation of the Log-Likelihood Ratio (LLR) at the channel output may impose great demand of memory and hardware area, especially for high-order modulations. This paper introduces a new approach for the approximation of the LLR in AWGN channels based on the splitting of the original constellation into smaller sectors. Each new sector has a less complex configuration in which it is possible to take into account only two symbols besides the received one. The proposed solution is applied for the 8-PSK and 16-APSK constellations adopted in the Digital Video for Satellite Second Generation standard (DVB-S2).**

***Index Terms*—Log-likelihood ratio (LLR), LDPC Codes, DVB-S2, Soft Demapper, Modulation and Coding, Communication Theory**

## I. Introduction

Low Density Parity Check (LDPC) codes provide excellent bit error rates in Additive White Gaussian Noise (AWGN) channels [1]. Nowadays design techniques for LDPC generation enable the construction of codes which approach the Shannon's capacity [7] to within hundredths of a decibel. However, the channel codes such as LDPC require a soft demapper [2] for the calculation of a soft metric for each bit from the constellation. Log-likelihood ratios (LLRs) have been shown to be very efficient metrics for soft decoding of many powerful codes such as turbo codes [8] and LDPC codes [1]. The LLRs offer practical advantages such as numerical stability (low dynamic range) and simplification of many decoding algorithms. They are defined as the logarithmic ratio between the probability of the bit to be 0, $b_j = 0$, and the probability of the bit to be 1, $b_j = 1$, from a given received symbol, $r$, i.e,

$$\mathrm{LLR}(b_j) = \ln\left(\frac{P(b_j = 0 \mid r)}{P(b_j = 1 \mid r)}\right) \tag{1}$$

The exact calculation of the LLR for an $M$-ary modulation over AWGN is defined as

$$\mathrm{LLR}(b_j) = \ln\left(\frac{\sum_{i\in\{\mathcal{A}_{b_j=0}\}} V_i}{\sum_{i\in\{\mathcal{A}_{b_j=1}\}} V_i}\right) \tag{2}$$

where $\mathcal{A}$ is the alphabet of symbols, $\mathcal{A}_{b_j=x}$ is the set of symbols which presents the $j$-th bit equal to 0 or 1 and $V_i$ is the Gaussian probability density function of the received symbol, which in this case is given by

$$V_i = \frac{1}{\sqrt{2\pi\sigma^2}} e^{\frac{-|r-s_i|^2}{2\sigma^2}} \quad i = 0, 1 \cdots M \tag{3}$$

In Equation (3), $\sigma^2$ is the variance per dimension, $r$ is the received symbol and $s_i$ is the $i$-th symbol from the constellation.

Equations (2) and (3) require a high computational cost and hardware complexity given by the large amount of square roots, exponential and logarithm operations in addition to the memory requirements, mainly observed in high order modulations. In this sense, the Max-Log approach [6] brings a significant reduction in the amount of operations through the elimination of the exponentials and logarithms computations. In this method, the LLR calculations rely on the Jacobian Logarithm [6] identity, which is approximated by

$$\ln(e^{x_1} + e^{x_2}) \approx \max(x_1, x_2) \tag{4}$$

In this paper, we present an alternative approximation [4] to the computation of the LLR. This approximation is tailor-made for the constellations used in the DVB-S2 [3]. Our main concern consists of avoiding the square root operations and the comparisons such as those required in Max-Log by the Euclidean distance calculation and the max function operation, respectively. This paper is organized as follows: Section II starts with an analysis of Max-Log approach over 8-PSK and then introduces the proposed approximation, the involved assumptions and the final LLRs expressions. Section III will expand this approximation for APSK modulation by taking as example 16-APSK constellation. The numerical results are illustrated in Section IV. Section V discusses all the results and draws the conclusions of this work.

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## II. 8-PSK LLR Approximation

From the Max-Log approximation it is possible to achieve a substantial reduction in the amount of operations on the soft demapper. In the context of the 8-PSK constellation, the LLRs can be approximated as

$$\begin{aligned}\mathrm{LLR}(b_2) &\approx \max(D_0, D_1, D_2, D_3) - \\ &\quad - \max(D_4, D_5, D_6, D_7) \\ \mathrm{LLR}(b_1) &\approx \max(D_0, D_1, D_4, D_5) - \\ &\quad - \max(D_2, D_3, D_6, D_7) \\ \mathrm{LLR}(b_0) &\approx \max(D_0, D_2, D_4, D_6) - \\ &\quad - \max(D_1, D_3, D_5, D_7)\end{aligned}$$

where

$$D_i = -\frac{|r - s_i|^2}{2\sigma^2} \quad i = 0, 1 \cdots 7 \tag{5}$$

$b_2$ is the Most Significant Bit (MSB) and $b_0$ is the Least Significant Bit (LSB).

On the other hand, the proposed simplification stems from the observation that $\max\{D_1, \cdots, D_{M/2}\}$ is always obtained from the symbol $s_i$ (associated with $D_i$) that is closest to the received symbol $r$. Proceeding from this point, one may approximate the LLR by designing decision areas for each bit, neglecting the probability that the noise corrupts the symbol such that it reaches another sector outside the original one. Thus, each sector will contain only two symbols from which the LLRs of a corresponding bit will be approximated. The sector to be employed in this approach is that in which $r$ resides. We remark that the simplification introduced by Max-Log approach uses all the constellation symbols for the LLR calculations. Nonetheless, aiming to reduce the number of operations and its complexity, the proposed method splits the constellation into smaller regions of decision such that the number of symbols to be considered are reduced to only two of them.

In order to obtain appropriate decision areas, a rotation $\phi = -\pi/8$ on the original 8-PSK constellation is proposed. This transformation will lead to convenient bounds (one sector per quadrant). These sectors might be defined by simply joining two neighboring symbols, one of them containing the corresponding bit equal to 1 and the second one containing the same bit equal to 0. After this rotation and the junction of symbols in pairs, contemplating the restriction mentioned before, the LLR for bit $b_2$ is approximated by

$$\mathrm{LLR}(b_2) \approx \begin{cases} D_0 - D_4; & I > 0,\ Q > 0 \\ D_1 - D_5; & I > 0,\ Q < 0 \\ D_2 - D_6; & I < 0,\ Q > 0 \\ D_3 - D_7; & I < 0,\ Q < 0 \end{cases} \tag{6}$$

where $I$ (in-phase) is the real value of the received symbol, $r$, and $Q$ (quadrature) is the imaginary value of this symbol. The constellation sections are depicted in Figure 1.

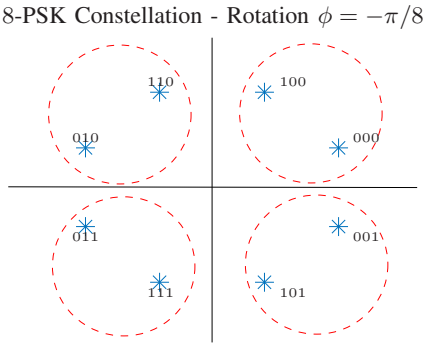


Figure 1: Decision areas for bit $b_3$.

The sectors splitting for the bit $b_1$ is even simpler due to a geometrical feature of this constellation. The symbols in which $b_1 = 0$ and those in which $b_1 = 1$ are symmetrically located with respect to the vertical axis, $Q$. Figure 2 shows the symbol partitions for which this approximation is based. The LLR for bit $b_1$ is approximatef by Equation (7).

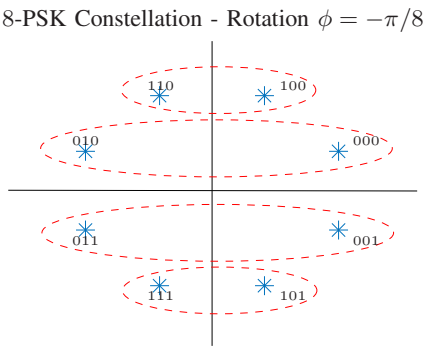


Figure 2: Decision areas for bit $b_1$

$$\mathrm{LLR}(b_1) \approx \begin{cases} D_4 - D_6; & Q > 0,\ |Q| > |I| \\ D_0 - D_2; & Q > 0,\ |I| > |Q| \\ D_1 - D_3; & Q < 0,\ |I| > |Q| \\ D_5 - D_7; & Q < 0,\ |Q| > |I| \end{cases} \tag{7}$$

Similarly, the symbols in which $b_0 = 0$ and those in which $b_0 = 1$ are symmetrically located with respect to the horizontal axis, $I$. Figure 3 depicts the symbol partitions for which this approximation is established. The LLR approximation for this bit is given by Equation (8).

$$\mathrm{LLR}(b_0) \approx \begin{cases} D_2 - D_3; & I < 0,\ |I| > |Q| \\ D_6 - D_7; & I < 0,\ |Q| > |I| \\ D_4 - D_5; & I > 0,\ |Q| > |I| \\ D_0 - D_1; & I > 0,\ |I| > |Q| \end{cases} \tag{8}$$

Deriving the proposed expressions, a general representation for the LLR expression in each sector is given by

$$\mathrm{LLR}(b_j) \approx \frac{1}{\sigma^2}\left[I(I_{sx} - I_{sy}) + Q(Q_{sx} - Q_{sy})\right] \tag{9}$$

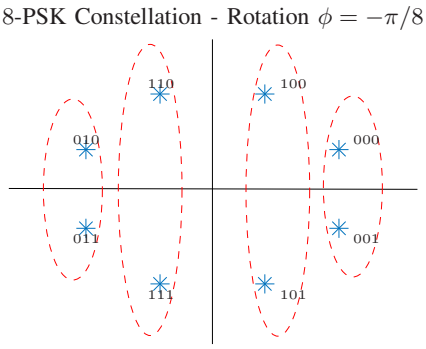


Figure 3: Decision areas for bit $b_0$ (Right - LSB)

where $s_x = I_{sx} + jQ_{sx}$ and $s_y = I_{sy} + jQ_{sy}$ are, respectively, the symbol inside the sector for which $b_j = 0$ and the symbol inside the sector for which $b_j = 1$.

The constants $\mu_i = (I_{sx} - I_{sy})$ and $\mu_q = (Q_{sx} - Q_{sy})$ can be easily calculated and stored in memories, by taking the hardware context. Table I shows the obtained values, $\mu_i$ and $\mu_q$ for 8-PSK in DVB-S2 constellation.

| LLR | $\mu_i$ | $\mu_q$ | Bound |
|---|---|---|---|
| $b_2$ | 0.5412 | $-0.5412$ | $I > 0, Q > 0$ |
| | 0.5412 | 0.5412 | $I > 0, Q < 0$ |
| | $-0.5412$ | $-0.5412$ | $I < 0, Q > 0$ |
| | $-0.5412$ | 0.5412 | $I < 0, Q < 0$ |
| $b_1$ | 0.7654 | 0 | $Q > 0, \|Q\| > \|I\|$ |
| | 1.8478 | 0 | $Q > 0, \|I\| > \|Q\|$ |
| | 1.8478 | 0 | $Q < 0, \|I\| > \|Q\|$ |
| | 0.7654 | 0 | $Q < 0, \|Q\| > \|I\|$ |
| $b_0$ | 0 | 0.7654 | $I < 0, \|I\| > \|Q\|$ |
| | 0 | 1.8478 | $I < 0, \|Q\| > \|I\|$ |
| | 0 | 1.8478 | $I > 0, \|Q\| > \|I\|$ |
| | 0 | 0.7654 | $I > 0, \|I\| > \|Q\|$ |

Table I: Table of constants for LLR in 8-PSK constellation.

## III. 16-APSK LLR Approximation

This section extends the proposed method for APSK modulations by using 16-APSK as an illustrative case. In addition to the PSK remarks, 16-APSK scenario counts on a particular aspect: the symmetry of the constellation and the possibility of mapping all the symbols to the first quadrant. This aspect is highly useful in order to reduce the number of sectors to be considered. As opposed to the 8-PSK constellation, 16-APSK does not need to be rotated.

The main difference between the two cases is that, in the PSK modulation, all the symbols in the constellation have the same energy. Hence, for any sector where the two symbols reside (one of them containing a bit set on 0 and, the second one containing the bit set on 1) the LLRs are approximated by

$$\text{LLR} \approx -\frac{\left[(I - D_{sx}^{(I)})^2 + (Q - D_{sx}^{(Q)})^2\right]}{2\sigma^2} + \\ + \frac{\left[(I - D_{sy}^{(I)})^2 + (Q - D_{sy}^{(Q)})^2\right]}{2\sigma^2} \quad (10)$$

The terms $-({D_{sx}^{(I)}}^2 + {D_{sx}^{(Q)}}^2) + ({D_{sy}^{(I)}}^2 + {D_{sy}^{(Q)}}^2)$, as well as $-(I^2+Q^2)+(I^2+Q^2)$ from the Equation (10) cancel each other such that all the quadratic terms in the LLR equation are removed. The same is not true for the 16-APSK constellation since the symbols $s_x$ and $s_y$ might not have the same energy level.

To overcome handicaps brought by the additional feature of this constellation (the amplitude variation) and the resulting loss of performance, we suggest to establish *Equivalent Received Symbols* that we will refer to as ERS from now on. A general ERS, $r_i$, is obtained by scaling the original constellation symbol such that $r_i = G_i r$. The scale factor $G_i$ is given by

$$G_i = \frac{R_i}{|r|}$$

where $R_i$ corresponds to the radius of the ring $i$ from constellation and $r$ corresponds to the radius of the original received symbol. Similarly as in 8-PSK, we will refer to $I_i$ and $Q_i$ as the real and imaginary parts, respectively, of the ERS $r_i$.

Particularly, in 16-APSK one defines, for each bit of the symbols, a set of areas where the LLRs are obtained based again on two symbols only. An illustrative scheme of the adopted regions in the context of bit $b_3$ (Left-MSB) is shown in the Figure 4. One remarks that, specially for this bit, the whole symbols from the constellation may be remapped to the first quadrant since there is symmetry between the horizontal and vertical axes.

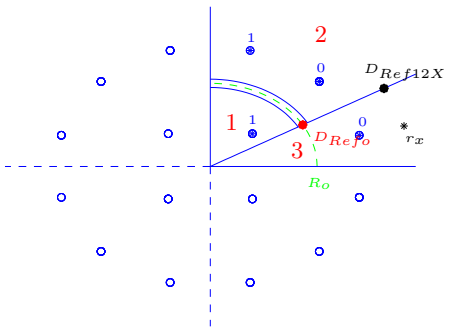


Figure 4: Decision areas for bit $b_3$.

**Region 1:** Bounds: $|r| < R_O,\ \pi/6 \leq \theta \leq \pi/2$

$$\begin{aligned}\text{LLR}(b_3) &\approx -\frac{|r_2 - D_0|^2}{2\sigma^2} + \frac{|r_1 - D_{12}|^2}{2\sigma^2} \\ &= \frac{(R_1^2 - R_2^2) + I_2 D_0^{(I)} + Q_2 D_0^{(Q)}}{\sigma^2} - \\ &\quad - \frac{I_1 D_{12}^{(I)} + Q_1 D_{12}^{(Q)}}{\sigma^2}\end{aligned}$$

As we can see in the calculation above, the final LLR is obtained by multiplying the real and imaginary parts of the received symbol by two constant values. As well as in the 8-PSK scenario, all these constants can be stored in memories structures, which makes the calculation much less complex.

**Region 2:** Bounds: $|r| \geq R_O,\ \pi/6 \leq \theta \leq \pi/2$

$$\begin{aligned}\text{LLR}(b_3) &\approx -\frac{|r_2 - D_0|^2}{2\sigma^2} + \frac{|r_2 - D_8|^2}{2\sigma^2} \\ &= \frac{I_2\left(D_0^{(I)} - D_8^{(I)}\right)}{\sigma^2} + \\ &\quad + \frac{Q_2\left(D_0^{(Q)} - D_8^{(Q)}\right)}{\sigma^2}\end{aligned}$$

As in the sector 1, the approximation for the sector 2 may be obtained by simply storing a set of constants.

**Region 3:** Bounds: $0 < \theta \leq \pi/6$

This sector would present a significant increase in the bit errors given the boundaries limitations. Inside this sector, the closest symbol in which the bit $b_3$ has the value 1 may not have the same radius neither the same phase than all the possible received symbols inside this sector. The same occurs for the associated symbols in which bit $b_3$ is 0. To overcome this limitation, the addition of a constant reference point, $D_{RefO}$ and an ERS $D_{Ref12X}$ is proposed as depicted in Figure 4.

$$D_{RefO} = \begin{bmatrix} R_O \cos(\pi/6) \\ R_O \sin(\pi/6) \end{bmatrix} \tag{11}$$

and

$$D_{Ref12X} = \begin{bmatrix} |r| \cos(\pi/6) \\ |r| \sin(\pi/6) \end{bmatrix} \tag{12}$$

The approximate expression for the LLR is calculated as

$$\begin{aligned}\text{LLR}(b_3) &\approx -\frac{|r_O - D_{RefO}|^2}{2\sigma^2} + \frac{|r - D_{Ref12X}|^2}{2\sigma^2} \\ &= \frac{(|r|^2 - R_O^2) + I_O D_{RefO}^{(I)} + Q_O D_{RefO}^{(Q)}}{\sigma^2} - \\ &\quad - \frac{I D_{Ref12X}^{(I)} + Q D_{Ref12X}^{(Q)}}{\sigma^2}\end{aligned}$$

Similar remarks can be made for the corresponding sectors of the bit $b_2$. However, the angles in the vectors $D_{RefO}$ and $D_{Ref12X}$ are set to $\pi/3$. The new bounds for each sector are depicted in Figure 5.

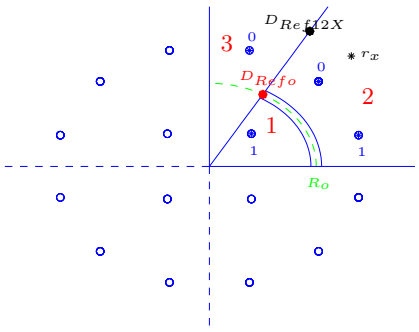


Figure 5: Decision areas for bit $b_2$.

**Region 1:** Bounds: $|r| < R_O,\ 0 \leq \theta \leq \pi/3$

$$\begin{aligned}\text{LLR}(b_2) &\approx -\frac{|r_2 - D_0|^2}{2\sigma^2} + \frac{|r_1 - D_{12}|^2}{2\sigma^2} \\ &= \frac{(R_1^2 - R_2^2) + I_2 D_0^{(I)} + Q_2 D_0^{(Q)}}{\sigma^2} - \\ &\quad - \frac{I_1 D_{12}^{(I)} + Q_1 D_{12}^{(Q)}}{\sigma^2}\end{aligned}$$

**Region 2:** Bounds: $|r| \geq R_O,\ 0 \leq \theta \leq \pi/3$

$$\begin{aligned}\text{LLR}(b_2) &\approx -\frac{|r_2 - D_0|^2}{2\sigma^2} + \frac{|r_2 - D_4|^2}{2\sigma^2} \\ &= \frac{\left[I_2\left(D_0^{(I)} - D_4^{(I)}\right) + Q_2\left(D_0^{(Q)} - D_4^{(Q)}\right)\right]}{\sigma^2}\end{aligned}$$

**Region 3:** Bounds: $\pi/3 < \theta \leq \pi/2$

$$\begin{aligned}\text{LLR}(b_2) &\approx -\frac{|r_O - D_{RefO}|^2}{2\sigma^2} + \frac{|r - D_{Ref12X}|^2}{2\sigma^2} \\ &= \frac{(|r|^2 - R_O^2) + I_O D_{RefO}^{(I)} + Q_O D_{RefO}^{(Q)}}{\sigma^2} - \\ &\quad - \frac{I D_{Ref12X}^{(I)} + Q D_{Ref12X}^{(Q)}}{\sigma^2}\end{aligned}$$

Log-Likelihood Ratios for the two less significant bits from 16-APSK are obtained in a similar way to the bit $b_1$ and bit $b_0$ from 8-PSK. The approximated LLR is obtained based in the closest symbol $X$ for which the bit has the value 0 and the closest symbol $Y$ for which the bit has the value 1. Fortunately for the bit $b_1$, the symbols $X$ and $Y$ are symmetric with respect to the vertical axis, as illustrated in Figure 6. Hence, the LLR for bit $b_1$ is given by

$$\begin{aligned}\text{LLR}(b_1) &\approx -\frac{|r - D_X|^2}{2\sigma^2} + \frac{|r - D_Y|^2}{2\sigma^2} \\ &= \frac{2I D_0^{(I)}}{2\sigma^2}\end{aligned}$$

To avoid many regions of decision, the LLR can be approximated by eliminating the constant factor such that

$$\text{LLR}(b_1) \approx \frac{I}{2\sigma^2} \tag{13}$$

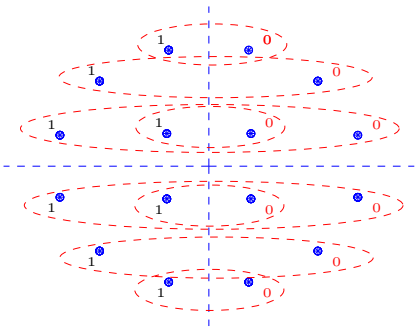

Figure 6: Configuration of the bit $b_1$ in 16-APSK constellation.

The same procedure can be applied for the bit $b_0$ (LSB). But in this case, the symmetry occurs with respect to the horizontal axis, as depicted in Figure 7. Hence, the LLR obtained, in this case, is

$$\mathrm{LLR}(b_0) \approx \frac{Q}{2\sigma^2} \tag{14}$$

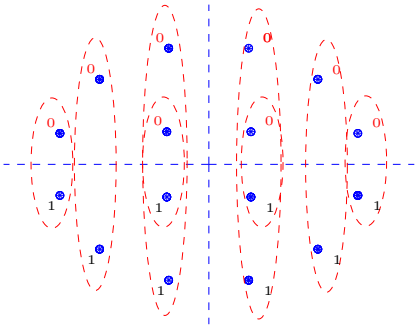

Figure 7: Configuration of the bit $b_0$ in 16-APSK constellation.

## IV. Results

The performance of the soft demapper was first evaluated independently and then by concatenating the obtained LLRs and the LDPC decoder. We performed the simulations on AWGN channel. Figure 8 shows the bit error rate obtained in the output of demapper.

In the concatenated simulation, the algorithm for the LDPC decoding is the Min-Sum [9]. Bit error rate was estimated for short frame transmission (16200 bits) from DVB-S2, code rate $R = 3/5$ for 8-PSK and $R = 2/3$ for 16-APSK. The obtained results are depicted in Figure 9.

These simulations confirm that the proposed LLR calculation has a low degradation of performance compared to the Max-Log simplification. In addition, the method provides a significant reduction in hardware and software

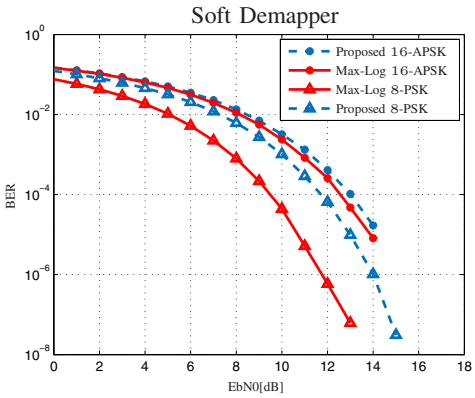


Figure 8: BER performance of the Soft Demappers.

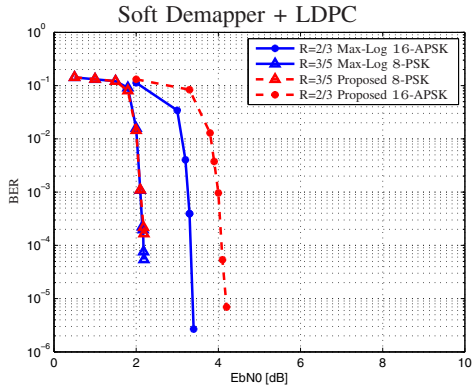


Figure 9: BER Performance 8-PSK and 16-APSK in the output of LDPC decoder.

complexity since the LLRs are essentially obtained by the multiplication of the real and imaginary part of the received symbol by a set of constants previously stored in a memory.

From Tables II and III it can be noted that the computational complexity for calculating one soft-bit value through Max-Log approach increases when the modulation order $M$ raises. The proposed soft demapper has a low-complexity compared to the other approximation method since the number of additions, multiplications e comparisons is much smaller.

| | Proposed 8-PSK | Max-Log 8-PSK |
|---|---|---|
| Additions | $1 \longrightarrow M/2-3$ | $25 \longrightarrow (3M+1)$ |
| Multiplications | $2 \longrightarrow M/2-2$ | $16 \longrightarrow (2M)$ |
| Comparisons | $4 \longrightarrow (M/2)$ | $6 \longrightarrow (M-2)$ |

Table II: Computational complexity for computing the soft information on the $i$-th bit in 8-PSK constellation.

The loss of performance in 16-APSK can not be totally justified by the proposed constellation's splitting since the results from the isolated soft demapper are much less affected than the results from LDPC decoder. A possible reason for

| | Proposed 16-APSK | Max-Log 16-APSK |
|---|---|---|
| Additions | $7 \longrightarrow M/2-1$ | $49 \longrightarrow (3M+1)$ |
| Multiplications | $16 \longrightarrow M$ | $32 \longrightarrow (2M)$ |
| Comparisons | $8 \longrightarrow (M/2)$ | $14 \longrightarrow (M-2)$ |

Table III: Computational complexity for computing the soft information on the $i$-th bit in 16-APSK constellation.

this could be the lack of scaling factors for adjustments in the calculated LLRs levels making them unsuitable or numerically unstable for the LDPC decoding algorithm. This hypothesis is well illustrated by Figure 10 in which one remarks that the LLR levels are quite similar in both methods if one takes a range of radius smaller than the bound $R_O$.

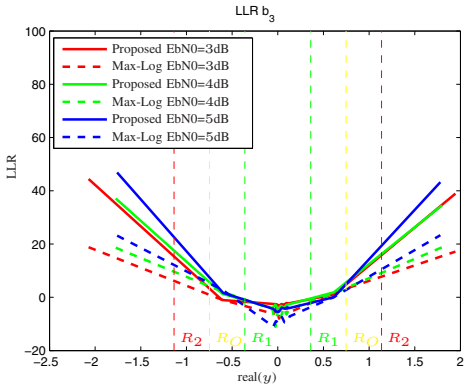


Figure 10: Comparison between the levels of LLR($b_3$) from Max-Log and from the proposed 16-APSK method.

On the other hand one notes that the LLR levels from both methods diverge from each other if one takes a range of values from the real part of a received symbol, $I$, that is larger than the bound $R_O$. This might suggest the need of scaling in the LLR equations from the proposed sectors.

## V. Conclusion

Results reveal a good performance for the approximation introduced in the 8-PSK. A degradation nearly 0.5dB with respect to the Max-Log approach is noted for the proposed LLR calculation in 16-APSK. The theoretical analysis and the simulation results indicate that the proposed soft demapper presents low complexity and a satisfactory performance especially for 8-PSK. In terms of computational complexity, this method requires much less operations of multiplication and addition for computing a given LLR. The number of comparisons is also reduced.

Directions for future work include the investigation of the scaling factors in the LLR equations and the generalization of this method for APSK systems by exploiting applications at higher order modulations in DVB-SX standard.

## References

[1] R. G. Gallager, *Low-Density Parity-Check Codes*, Cambridge, MA: MIT Press, 1963.

[2] John R. Barry, David G. Messerschimitt, Edward A. Lee, *Digital Communication: Third Edition*, Kluwer Academic Publisher, Norwell, MA, USA, 2003.

[3] ETSI EN 302 307 V1.3.1, *Digital Video Broadcasting (DVB); Second generation framing structure, channel coding and modulation systems for Broadcasting, Interactive Services, News Gathering and other broadband satellite applications (DVB-S2)*, ETSI publications, Mar. 2013.

[4] Ryoo, Sunheui, Sooyoung Kim, and Sung Pal Lee. *Efficient soft demapping method for high order modulation schemes.* CDMA International Conference (CIC) 2003.

[5] G. D. Forney, Jr., *Modulation and Coding for Linear Gaussian Channels*, IEEE Trans. on Information Theory, Vol 44, No 6, Oct. 1998.

[6] Martina M., Masera G., Papaharababos S., Mathiopoulos P.T., Gioulekas F., *On Practical Implememntation and Generalization of max* Operator for Turbo and LDPC Decoders*, IEEE Trans. on Instrumentation and Measurement, Vol 61, No 4, pp. 888-895, Mar. 2012.

[7] C. E. Shannon, *Probability of error for optimal codes in a Gaussian channel*, Bell Syst. Tech. J., vol. 38, pp. 611-656, 1959

[8] Berrou, Claude, and Alain Glavieux. *Near optimum error correcting coding and decoding: Turbo-codes.* Communications, IEEE Transactions on 44.10 (1996): 1261-1271.

[9] Emran, Ahmed, and Maha Elsabrouty. *Simplified variable-scaled min sum LDPC decoder for irregular LDPC codes.* Consumer Communications and Networking Conference (CCNC), 2014 IEEE 11th. IEEE, 2014.