Decade counter using CMOS

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***Abstract*—This manual shows how to use CMOS to design logic gates for a decade counter.**

I. Components

Component	Value	Quantity
Breadboard		1
Resistor	$\geq 220\Omega$	1
CD4007	CMOS	20
Seven Segment Display	Common Anode	1
Decoder	7447	1
Jumper Wires		20

TABLE I

II. CMOS Logic Gates

The CMOS logic gates can be designed using the CD4007 IC shown in Fig. 1.

A. NOT

As shown in Fig. 2, one PMOS and one NMOS elements in Fig. 1 are required.

B. NAND

NAND gate is one of the two universal logic gates which can be used to construct any logic gate. Fig. 3 shows how to construct a 2 input NAND gate. 3-input NAND gate can be formed with the help of CMOS as per Fig. 4.

III. Seven Segment Display

Problem 1. Connect the 7447 IC in Fig. 5 to the seven segment display in Fig. 6 and display all numbers from 0-9.

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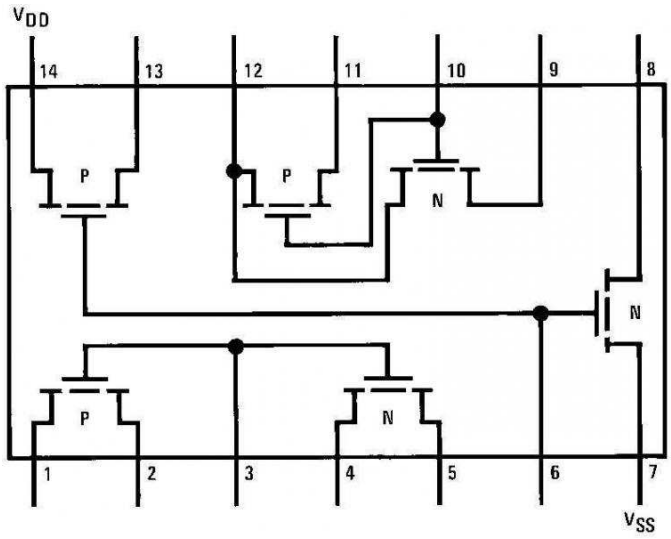

Fig. 1. CD4007

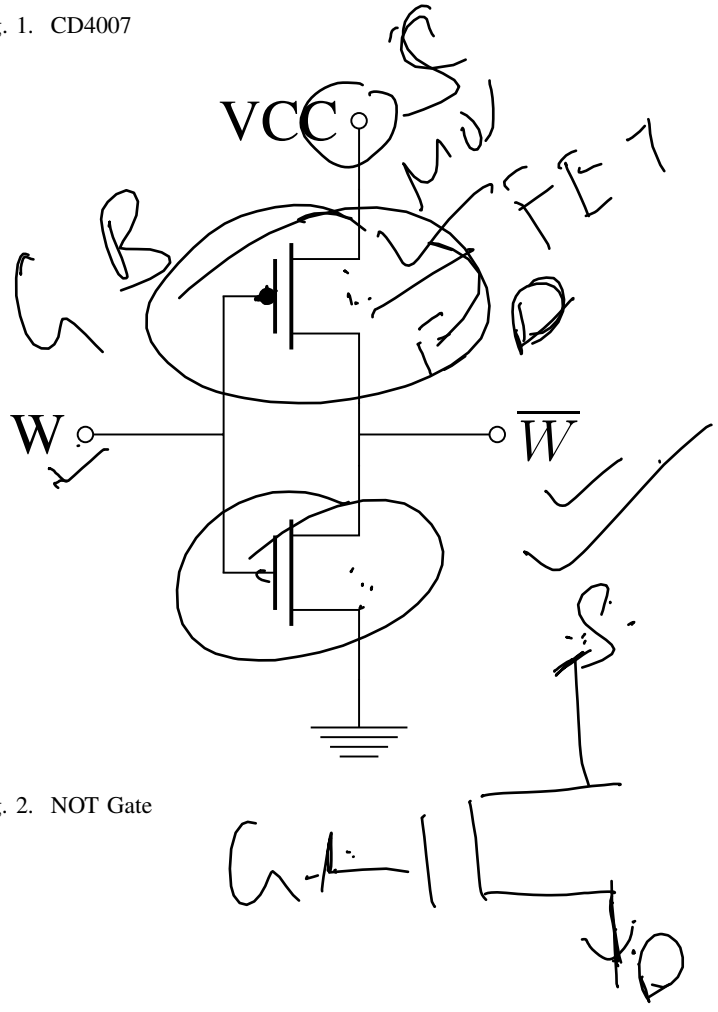

Fig. 2. NOT Gate

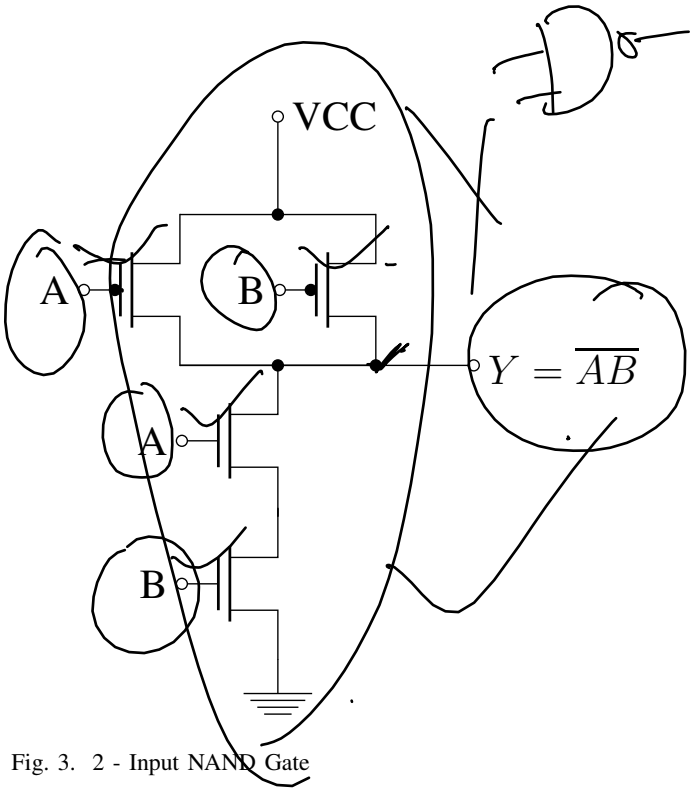

Fig. 3. 2 - Input NAND Gate

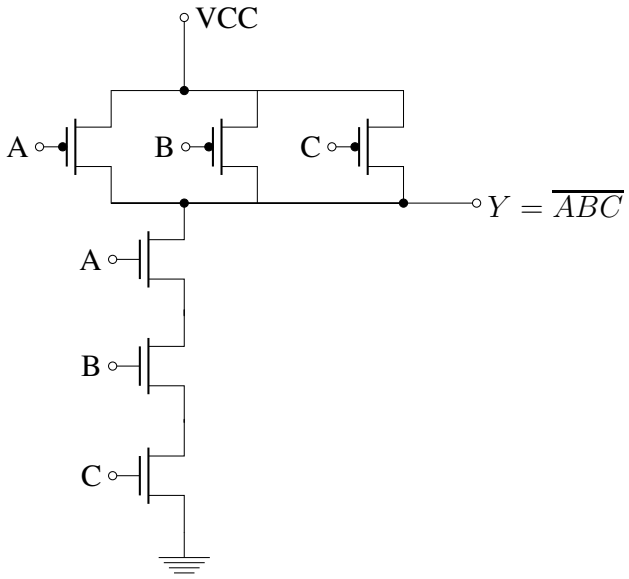

Fig. 4. 3 - Input NAND Gate

A. Counting Decoder

A counting decoder increments the input by 1 and has the following logic

$$A = \overline{W} \tag{1}$$
$$B = W\bar{X}\bar{Z} + \bar{W}X \tag{2}$$
$$C = \bar{X}Y + \bar{W}Y + W\bar{X}\bar{Y} \tag{3}$$
$$D = \bar{W}Z + WXY \tag{4}$$

where W,X,Y,Z are inputs and A,B,C,D are outputs.

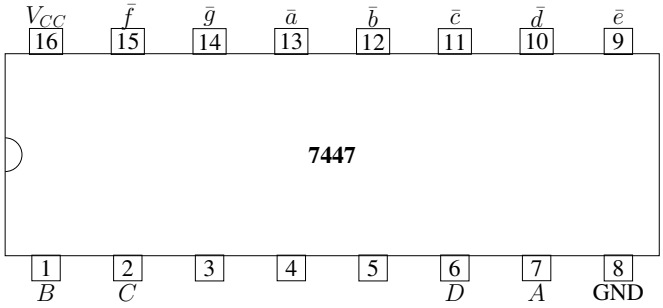

Fig. 5. 7447

B. CMOS Counting Decoder

Problem 2. Express (1)-(4) using NAND logic

Solution:

$$A = \overline{W} \tag{5}$$
$$B = W\bar{X}\bar{Z} + \bar{W}X = \overline{(\overline{W\bar{X}\bar{Z}}).(\overline{\bar{W}X})} \tag{6}$$
$$C = \bar{X}Y + \bar{W}Y + W\bar{X}\bar{Y} \tag{7}$$
$$= \overline{(\overline{\bar{X}Y}).(\overline{\bar{W}Y}).(\overline{W\bar{X}\bar{Y}})} \tag{8}$$
$$D = \bar{W}Z + WXY = \overline{(\overline{\bar{W}Z}).(\overline{WXY})} \tag{9}$$

Problem 3. Express A through CMOS logic.

Solution: The logic for A is an inverter. Construct a circuit similar to Fig.2 which is a simple NOT gate. When input is W then output is $\overline{W}$.

Problem 4. Express B through CMOS logic.

Solution: Fig. 7, followed by Fig. 2.

Problem 5. Express C through CMOS logic.

Solution: Fig. 8, followed by Fig. 2.

Problem 6. Express C through CMOS logic.

Solution: Fig. 9, followed by Fig. 2.

Problem 7. Design the 7447 IC using CMOS logic.

IV. Decade Counter

A. Clock

Fig. 10 shows a clock, which is a series of pulses with period T.

Problem 8. Design a circuit for generating Fig. 10.

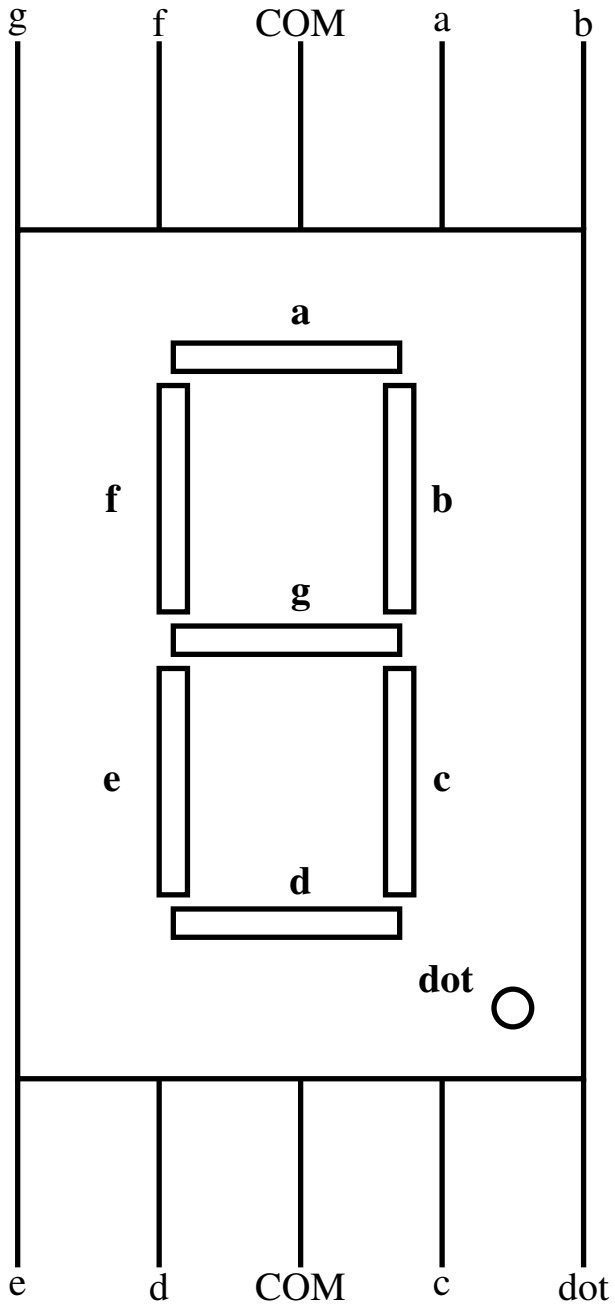

Fig. 6. Seven Segment Display

Solution: Fig. 11 can be used to generate the clock in Fig. 10.

Problem 9. Explain the circuit in Fig. 11.

Solution: In Fig. 11, let $R_1 > R_2$. The circuit is an astable multivibrator. It is made up of two NOT gates. When the output of second not gate is HIGH, the input of second not gate is LOW. The capacitor charges up which changes the output of second not gate from HIGH to LOW. Now we have

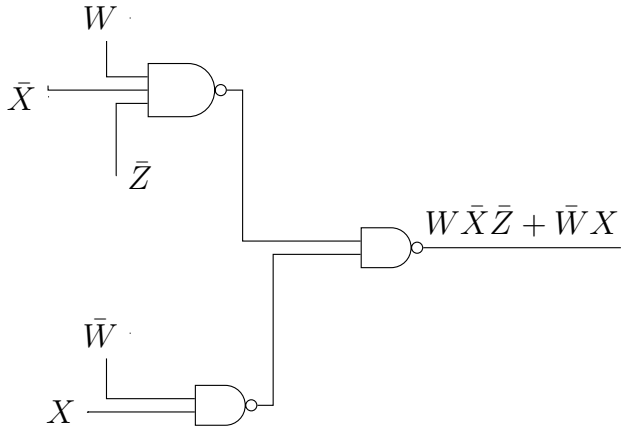

Fig. 7. CMOS Logic for $\overline{B}$

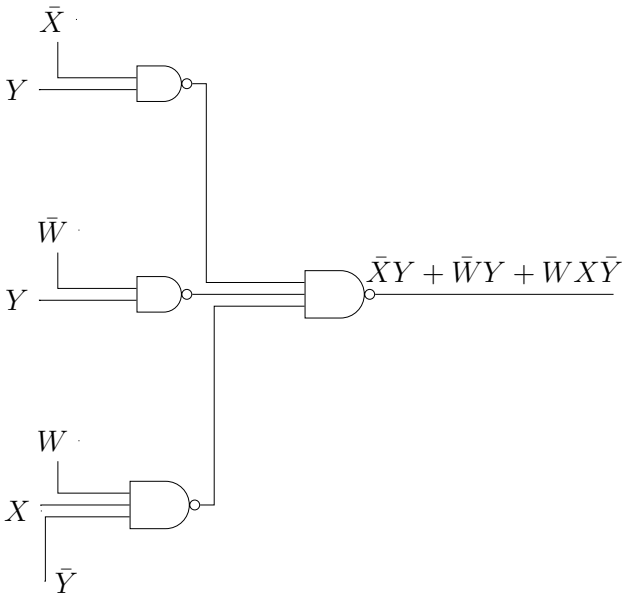

Fig. 8. CMOS Logic for $\overline{C}$

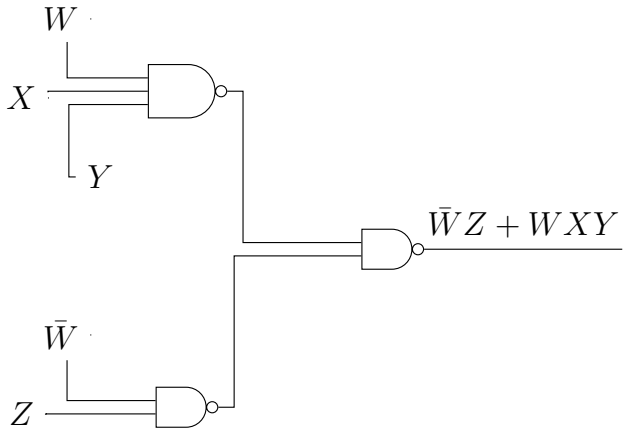

Fig. 9. CMOS Logic for $\overline{D}$

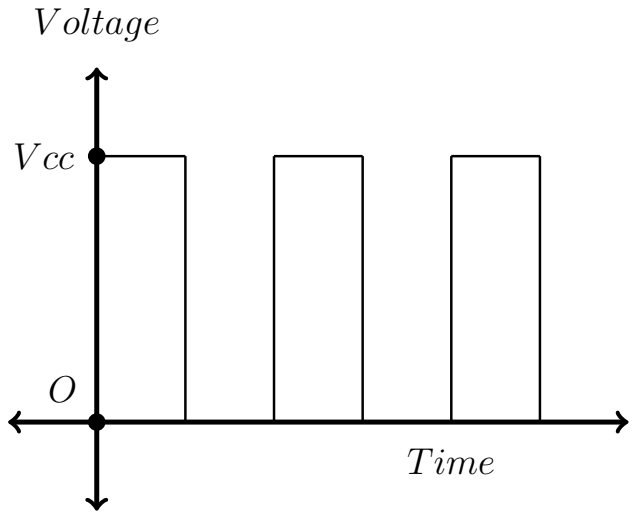

Fig. 10. clock output

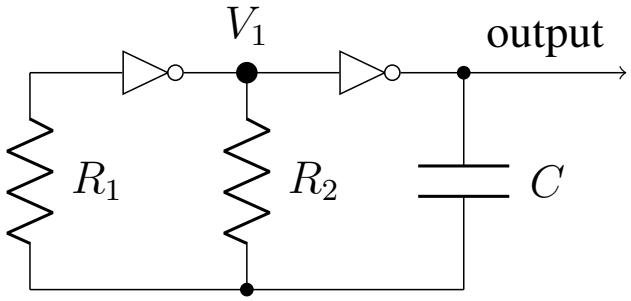

Fig. 11. Clock Circuit

output of second not gate LOW and its input HIGH. This makes the capacitor to be reverse biased. This is followed by discharging of capacitor. Due to discharging of capacitor, the output of second not gate again becomes HIGH. This process continues and what the observer observes is a series of HIGH and LOW voltages at the output.

Problem 10. Explain why $R_1 > R_2$.

Solution: The CD4007 IC in Fig. 1 has input switching voltage point at 0.5Vcc. We are using Vcc as 5V. Hence, input voltages ranging from 3.5 to 5 V are recognised as HIGH and voltages from 0 to 1.5 V as LOW for this IC. The voltages in input and output of second not gate can be only 0 or Vcc. The schematic turns in the other stage when V_1 is equal to the half of the power voltage. When the second gate output flips from 1 to 0, the capacitor is charged to -0.5Vcc (the left plate is negative), so V1 becomes -0.5Vcc and starts to increase because R_2 is connected to Vcc. R_1 does not affect the time period at all. It is placed there so that the input current of the inverter does not affect the work of the schematic. That is why it should be much bigger than R_2.

Problem 11. Obtain the time period of the clock T.

Solution: Let $\tau = R_2C$. Then,

$$V_1 = Vcc.(1 - e^{-\frac{t}{\tau}}) - \frac{Vcc}{2}.e^{-\frac{t}{\tau}} \tag{10}$$

$$= Vcc - \frac{3.Vcc}{2}.e^{-\frac{t}{\tau}} \tag{11}$$

The switching of the schematic will happen when

$$V_1 = \frac{Vcc}{2} \tag{12}$$

$$\implies \frac{Vcc}{2} = Vcc - \frac{3.Vcc}{2}.e^{-\frac{t}{\tau}} \tag{13}$$

$$\implies t = \tau \ln 3 = R_2C \ln 3 \tag{14}$$

This is the half of the period (because the schematic switches exactly on the half of the Vcc), so the period

$$T = 2t = 2 \ln 3 R_2C \tag{15}$$

We can choose a specific value of R_2 and C to achieve any particular time period for the clock.

B. Flip Flop

Problem 12. Design a circuit for the D-Flip Flop.

Solution: See Fig. 12. Note that a clock is necessary for building a Flip Flop.

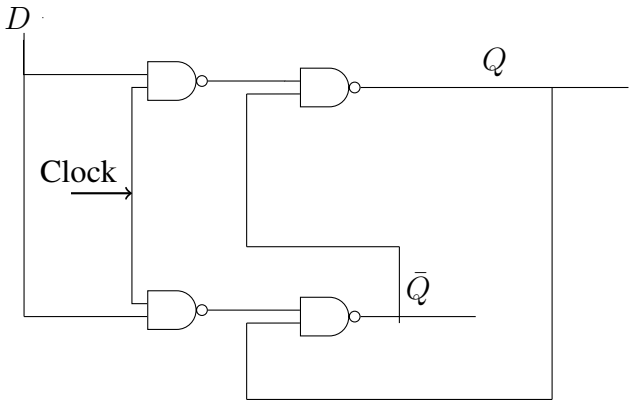

Fig. 12. D Flip-flop

Problem 13. Design a decade counter.

Solution: See Fig. 13

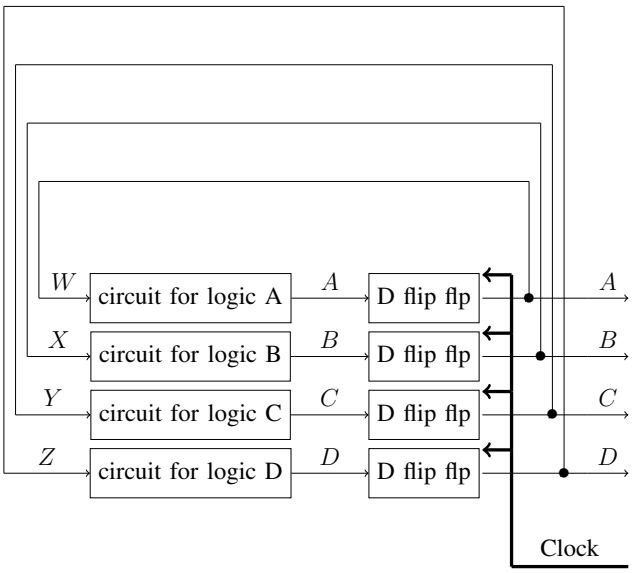

Fig. 13. circuit for decade counter