Template for Logic Gates

Parijat Mitra[†] and GVV Sharma*

Abstract—This manual shows how to draw logic gates.

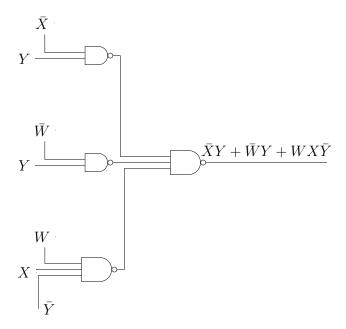


Fig. 1. CMOS Logic for \overline{C}

[†] Parijat is a UG student at IIT Bhilai. He did this work as an intern at IIT Hyderabad. *The author is with the Department of Electrical Engineering, Indian Institute of Technology, Hyderabad 502285 India e-mail: gadepall@iith.ac.in. All content in this manual is released under GNU GPL. Free and open source.