

Digital Logic Design

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Abstract—This manual provides a simple introduction to Digital Design.

1 SEVEN SEGMENT DISPLAY

- 1.1. Fig. 1.1.1 shows a seven segment display with pins a, b, c, d, e, f, g . Each of these pins is connected to an LED (light emitting device).
- 1.2. Fig. 1.2.1 shows how to generate the numbers on the display using Table 1.2.1. Complete Table 1.2.1 by drawing the figures for all numbers from 0-9.

a	b	c	d	e	f	g	decimal
1	0	0	1	1	1	1	1
0	0	1	0	0	1	0	2

TABLE 1.2.1

2 INCREMENTING DECODER

- 2.1. The incrementing decoder takes the numbers 0, 1, ..., 9 in binary as inputs and generates the consecutive number as output. The corresponding *truth table* is available in Table. 2.1.1.

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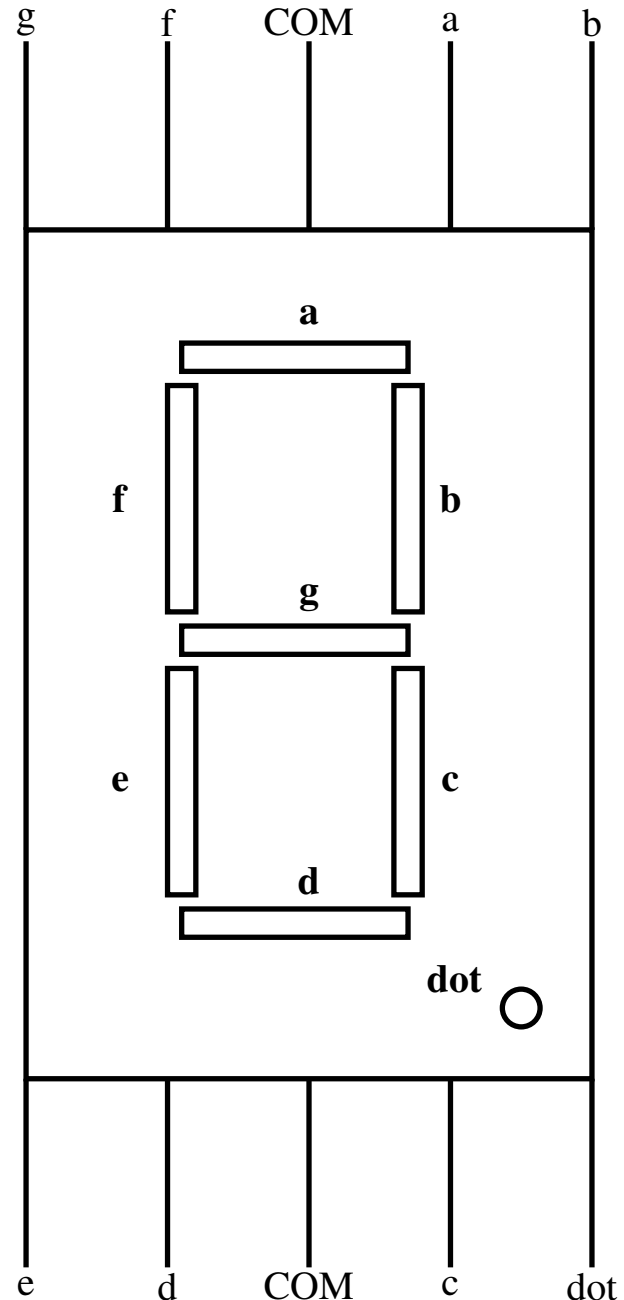


Fig. 1.1.1

- 2.2. Using Boolean logic, outputs A, B, C and D in Table 2.1.1 can be expressed in terms of the

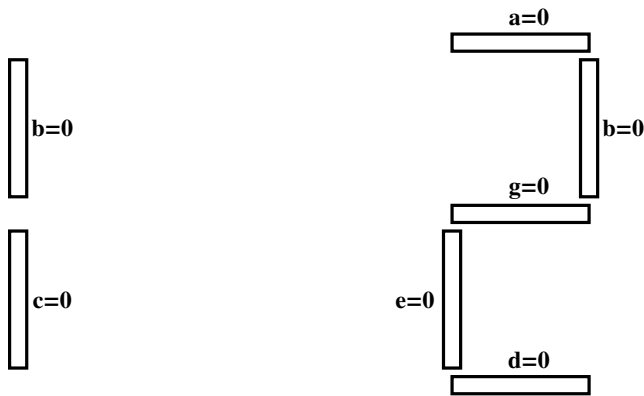


Fig. 1.2.1

Z	Y	X	W	D	C	B	A
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0

TABLE 2.1.1: Truth table for the incrementing decoder

inputs W, X, Y, Z as

$$A = W'X'Y'Z' + W'XY'Z' + W'X'YZ' + W'XYZ' + W'X'Y'Z \quad (2.2.1)$$

$$B = WX'Y'Z' + W'XY'Z' + WX'YZ' + W'XYZ' \quad (2.2.2)$$

$$C = WXY'Z' + W'X'YZ' + WX'YZ' + W'XYZ' \quad (2.2.3)$$

$$D = WXYZ' + W'X'Y'Z \quad (2.2.4)$$

2.3. Execute the following code for different input values to verify (2.2.4).

```
codes/inc_decode.c
```

2.4. Modify the above C code to verify (2.2.1), (2.2.2) and (2.2.3).

2.5. Repeat the exercise for the truth table in 2.5.1.

D	C	B	A	a	b	c	d	e	f	g	Decimal
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	2
0	0	1	1	0	0	0	0	1	1	0	3
0	1	0	0	1	0	0	1	1	0	0	4
0	1	0	1	0	1	0	0	1	0	0	5
0	1	1	0	0	1	0	0	0	0	0	6
0	1	1	1	0	0	0	1	1	1	1	7
1	0	0	0	0	0	0	0	0	0	0	8
1	0	0	1	0	0	0	1	1	0	0	9

TABLE 2.5.1: Truth table for display decoder.

3 KARNAUGH MAP

3.1. K-Map for A: The expression in (2.2.1) can be minimized using the K-map in Fig. 3.1.1. In Fig. 3.1.1, the *implicants* in boxes 0,2,4,6 result in $W'Z'$. The implicants in boxes 0,8 result in $W'X'Y'$. Thus, after minimization using Fig. 3.1.1, (2.2.1) can be expressed as

$$A = W'Z' + W'X'Y' \quad (3.1.1)$$

Using the fact that

$$\begin{aligned} X + X' &= 1 \\ XX' &= 0, \end{aligned} \quad (3.1.2)$$

derive (3.1.1) from (2.2.1) algebraically.

ZY	XW			
	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	0	0	0	0
10	1	0	0	0

Fig. 3.1.1: K-map for A.

3.2. K-Map for B : From Table 2.1.1, using boolean logic, Show that (2.2.2) can be reduced to

$ZY \backslash XW$	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	0	0	0
10	0	0	0	0

Fig. 3.2.1: K-map for B .

$$B = WX'Z' + W'XZ' \quad (3.2.1)$$

using Fig. 3.2.1.

3.3. Derive (3.2.1) from (2.2.2) algebraically using (3.1.2).

3.4. K-Map for C : From Table 2.1.1, using boolean logic, Show that (2.2.3) can be reduced to

$ZY \backslash XW$	00	01	11	10
00	0	0	1	0
01	1	1	0	1
11	0	0	0	0
10	0	0	0	0

Fig. 3.4.1: K-map for C .

$$C = WXY'Z' + X'YZ' + W'YZ' \quad (3.4.1)$$

using Fig. 3.4.1.

3.5. Derive (3.4.1) from (2.2.3) algebraically using (3.1.2).

3.6. K-Map for D : From Table 2.1.1, using boolean logic,

$$D = WXYZ' + W'X'Y'Z \quad (3.6.1)$$

$ZY \backslash XW$	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	0	0	0	0
10	1	0	0	0

Fig. 3.6.1: K-map for D .

3.7. Minimize (3.6.1) using Fig. 3.6.1.

3.8. Modify your C program to verify the the K-Map equations for A,B,C and D in (3.1.1), (3.1.1) and (3.1.1) respectively.

3.9. Revise by using don't care conditions and verify through a C code.

3.10. Display Decoder: Use K-maps to obtain the minimized expressions for a, b, c, d, e, f, g in terms of A, B, C, D in Table 2.5.1 with and without don't care conditions.