DIGITAL DESIGN

Through Embedded Programming

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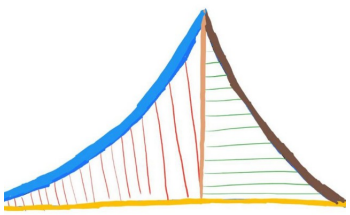


Contents

Introduction

This book introduces digital design through using the arduino framework.

Chapter 1

Installation

1.1. Termux

1. On your android device, install fdroid apk from

```
https://www.f-droid.org/
```

2. Install Termux from apkpure

3. Install basic packages on termux

```
#Give termux access to your user directory in android
termux-setup-storage

#Upgrade packages
apt update && apt upgrade
apt install build-essential openssh

#Mandatory packages
apt install curl git wget subversion proot proot-distro python nmap neovim ranger
#--------------------End Install Termux
```

```
    ------------------------------
```

4. Install Ubuntu on termux

```
proot-distro install ubuntu
proot-distro login ubuntu
```

1.2. Platformio

1. Install Packages

```
apt update && apt upgrade
apt install apt-utils build-essential cmake neovim
apt install git wget subversion imagemagick nano
apt install avra avrdude gcc-avr avr-libc
#--------------------End Installing ubuntu on termux
    ------------------------------


#-------------------- Installing python3 on termuxubuntu
    ------------------------------
apt install python3-pip python3-numpy python3-scipy python3-matplotlib
    python3-mpmath python3-sympy python3-cvxopt
#-------------------- End installing python3 on termuxubuntu
    ------------------------------


#-------------------- Installing platformio on termuxubuntu
```

```
    ------------------------------
pip3 install platformio
#-------------------- End installing python3 on termuxubuntu
    ------------------------------
```

2. Execute the following on ubuntu

```
cd ide/piosetup/codes
pio run
```

3. Connect your arduino to the laptop/rpi and type

```
pio run -t nobuild -t upload
```

4. The LED beside pin 13 will start blinking

1.3. Arduino Droid

1. Install ArduinoDroid from apkpure

2. Open ArduinoDroid and grant all permissions

3. Connect the Arduino to your phone via USB-OTG

4. For flashing the bin files, in ArduinoDroid,

```
Actions->Upload->Upload Precompiled
```

then go to your working directory and select

```
pio/build/uno/firmwarehex
```

for uploading hex file to the Arduino Uno

5. The LED beside pin 13 will start blinking

Chapter 2

Seven Segment Display

We show how to control a seven segment display.

2.1. Components

Component	Value	Quantity
Breadboard		1
Resistor	$\geq 220\Omega$	1
Arduino	Uno	1
Seven Segment Display	Common Anode	1
Jumper Wires		20

Table 2.1:

2.1.1. Breadboard

The breadboard can be divided into 5 segments. In each of the green segements, the pins are internally connected so as to have the same voltage. Similarly, in the central segments, the pins in each column are internally connected in the same fashion as the blue columns.

2.1.2. Seven Segment Display

The seven segment display in Fig. 2.2 has eight pins, a, b, c, d, e, f, g and *dot* that take an active LOW input, i.e. the LED will glow only if the input is connected to ground. Each of these pins is connected to an LED segment. The *dot* pin is reserved for the $\cdot$ LED.

2.1.3. Arduino

The Arduino Uno has some ground pins, analog input pins A0-A3 and digital pins D1-D13 that can be used for both input as well as output. It also has two power pins that can generate $3.3V$ and $5V$. In the following exercises, only the GND, $5V$ and digital pins will be used.

2.2. Display Control through Hardware

2.2.1. Powering the Display

1. Plug the display to the breadboard in Fig. 2.1 and make the connections in Table 2.2. Henceforth, all 5V and GND connections will be made from the breadboard.

Arduino	**Breadboard**
5V	Top Green
GND	Bottom Green

Table 2.2: Supply for Bread board

2. Make the connections in Table 2.3.

3. Connect the Arduino to the computer. The DOT led should glow.

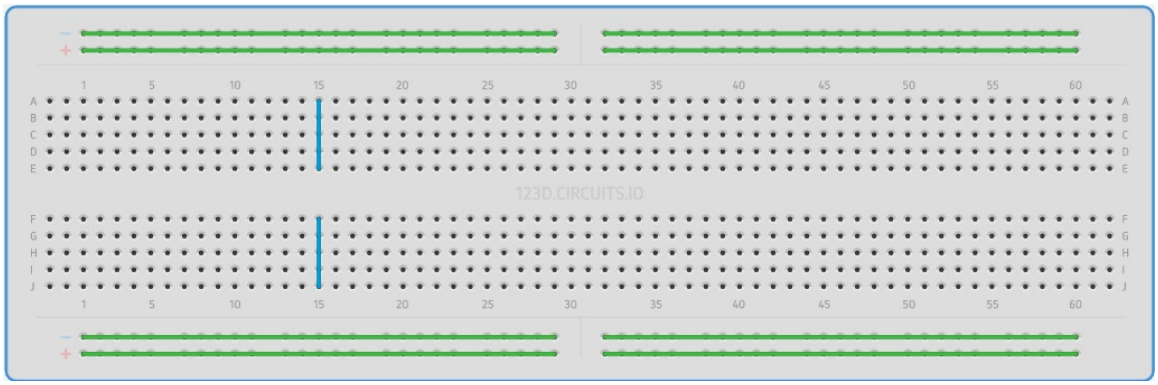


Figure 2.1: Bread board connnections

Breadboard		**Display**
5V	Resistor	COM
GND		DOT

Table 2.3: Connecting Seven segment display on Bread board

2.2.2. Controlling the Display

Fig. 2.3 explains how to get decimal digits using the seven segment display. GND=0.

1. Generate the number 1 on the display by connecting only the pins b and c to GND (=0). This corresponds to the first row of 2.4. 1 means not connecting to GND.

2. Repeat the above exercise to generate the number 2 on the display.

3. Draw the numbers 0-9 as in Fig. 2.3 and complete Table 2.4

a	**b**	**c**	**d**	**e**	**f**	**g**	**decimal**
0	0	0	0	0	0	1	0

Table 2.4:

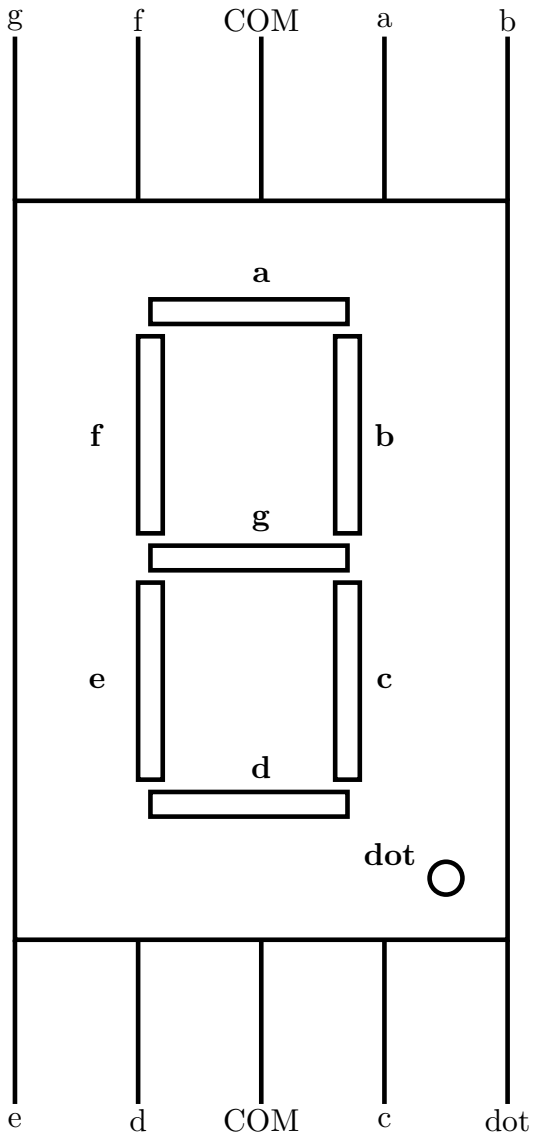


Figure 2.2: Seven Segment pins

2.3. Display Control through Software

1. Make connections according to Table 2.5

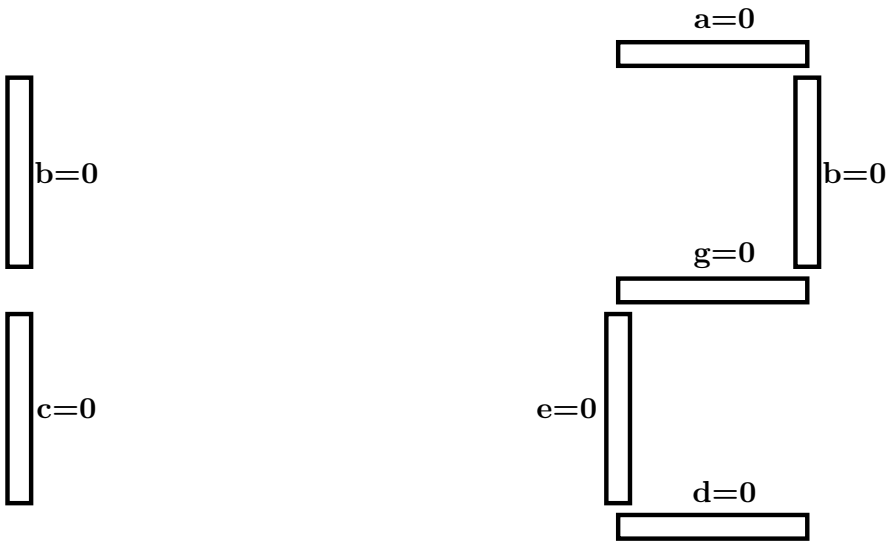


Figure 2.3: Seven Segment connections

Arduino	2	3	4	5	6	7	8
Display	a	b	c	d	e	f	g

Table 2.5:

2. Download the following code using the arduino IDE and execute

ide/sevenseg/codes/sevenseg/sevenseg.ino

3. Now generate the numbers 0-9 by modifying the above program.

Chapter 3

7447

Here we show how to use the 7447 BCD-Seven Segment Display decoder to learn Boolean logic.

3.1. Components

Component	Value	Quantity
Resistor	220 Ohm	1
Arduino	UNO	1
Seven Segment Display		1
Decoder	7447	1
Jumper Wires	M-M	20
Breadboard		1

Table 3.1:

3.2. Hardware

1. Make connections between the seven segment display in Fig. 2.2 and the 7447 IC in Fig. 3.1 as shown in Table 3.2

7447	$\bar{a}$	$\bar{b}$	$\bar{c}$	$\bar{d}$	$\bar{e}$	$\bar{f}$	$\bar{g}$
Display	a	b	c	d	e	f	g

Table 3.2:

2. Make connections to the lower pins of the 7447 according to Table 3.3 and connect $V_{CC} = 5$V. You should see the number 0 displayed for 0000 and 1 for 0001.

D	**C**	**B**	**A**	**Decimal**
0	0	0	0	0
0	0	0	1	1

Table 3.3:

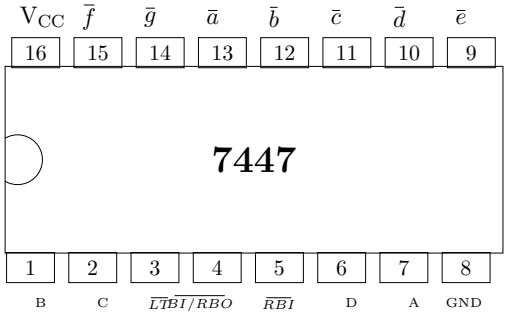


Figure 3.1:

3. Complete Table 3.3 by generating all numbers between 0-9.

3.3. Software

1. Now make the connections as per Table 3.4 and execute the following program

ide/7447/codes/gvv_ard_7447/gvv_ard_7447.cpp

7447	D	C	B	A
Arduino	5	4	3	2

Table 3.4:

Z	Y	X	W	**D**	**C**	**B**	**A**
0	0	0	0	**0**	**0**	**0**	**1**
0	0	0	1	**0**	**0**	**1**	**0**
0	0	1	0	**0**	**0**	**1**	**1**
0	0	1	1	**0**	**1**	**0**	**0**
0	1	0	0	**0**	**1**	**0**	**1**
0	1	0	1	**0**	**1**	**1**	**0**
0	1	1	0	**0**	**1**	**1**	**1**
0	1	1	1	**1**	**0**	**0**	**0**
1	0	0	0	**1**	**0**	**0**	**1**
1	0	0	1	**0**	**0**	**0**	**0**

Table 3.5: Truth table for incrementing Decoder.

In the truth table in Table 3.5, W, X, Y, Z are the inputs and A, B, C, D are the outputs. This table represents the system that increments the numbers 0-8 by 1 and resets the number 9 to 0 Note that $D = 1$ for the inputs 0111 and 1000. Using boolean logic,

$$D = WXYZ^{'} + W^{'}X^{'}Y^{'}Z \tag{3.1}$$

Note that 0111 results in the expression $WXYZ^{'}$ and 1000 yields $W^{'}X^{'}Y^{'}Z$.

2. The code below realizes the Boolean logic for B, C and D in Table 3.5. Write the logic for A and verify.

ide/7447/codes/inc_dec/inc_dec.ino

3. Now make additional connections as shown in Table 3.6 and execute the following code. Comment.

ide/7447/codes/ip_inc_dec/ip_inc_dec.cpp

Solution: In this exercise, we are taking the number 5 as input to the arduino and displaying it on the seven segment display using the 7447 IC.

	Z	Y	X	W
Input	0	1	0	1
Arduino	9	8	7	6

Table 3.6:

4. Verify the above code for all inputs from 0-9.

5. Now write a program where

   (a) the binary inputs are given by connecting to 0 and 1 on the breadboard

   (b) incremented by 1 using Table 3.5and

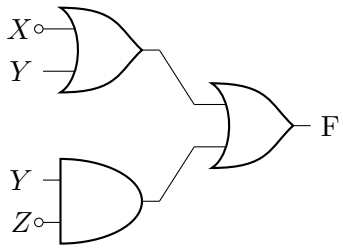
   (c) the incremented value is displayed on the seven segment display.

6. Write the truth table for the 7447 IC and obtain the corresponding boolean logic equations.

7. Implement the 7447 logic in the arudino. Verify that your arduino now behaves like the 7447 IC.

3.4. Problems

1. Obtain the Boolean Expression for the Logic circuit shown below (CBSE 2013)



2. Verify the Boolean Expression (CBSE 2013)

$$A + C = A + A'C + BC \tag{3.2}$$

3. Draw the Logic Circuit for the following Boolean Expression (CBSE 2015)

$$f(x, y, z, w) = (x' + y)z + w' \tag{3.3}$$

4. Verify the following (CBSE 2015)

$$U' + V = U'V' + U'V + UV \tag{3.4}$$

5. Draw the Logic Circuit for the given Boolean Expression (CBSE 2015)

$$(U + V')W' + Z \tag{3.5}$$

6. Verify the following using Boolean Laws (CBSE 2015)

$$X + Y' = XY + XY' + X'Y' \tag{3.6}$$

7. Write the Boolean Expression for the result of the Logic Circuit as shown in Fig. 3.2 (CBSE 2016)

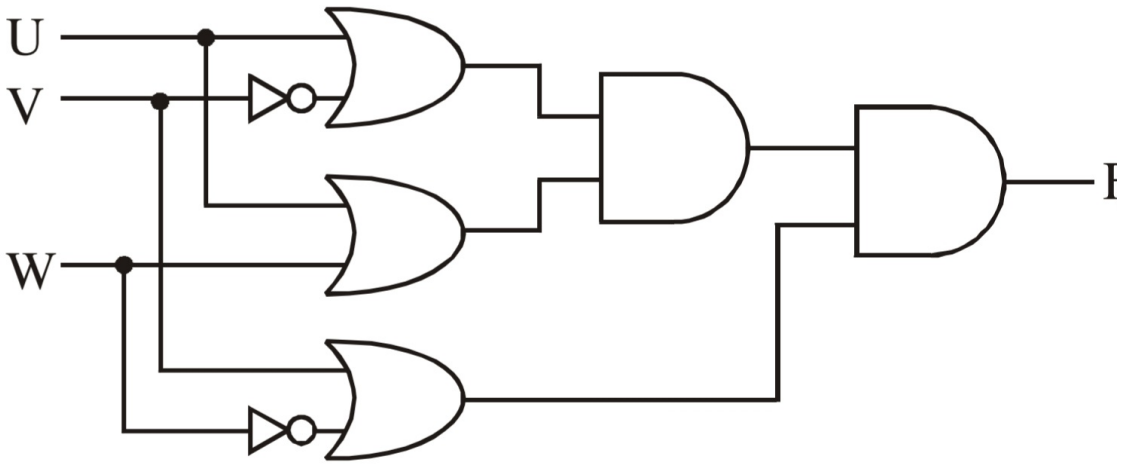


Figure 3.2:

8. Draw the logic circuit of the following Boolean Expression using only NAND Gates. (CBSE 2017)

$$XY + YZ \tag{3.7}$$

9. Draw the Logic Circuit of the following Boolean Expression using only NOR Gates (CBSE 2017)

$$(A + B)(C + D) \tag{3.8}$$

10. Draw the Logic Circuit of the following Boolean Expression (CBSE 2018)

$$(U' + V)(V' + W') \tag{3.9}$$

11. Derive a Canonical POS expression for a Boolean function F, represented by Table 3.7 (CBSE 2019)

X	Y	Z	F(X,Y,Z)
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

Table 3.7:

12. For the logic circuit shown in Fig.3.3, find the simplified Boolean expression for the output. (GATE EC 2000)

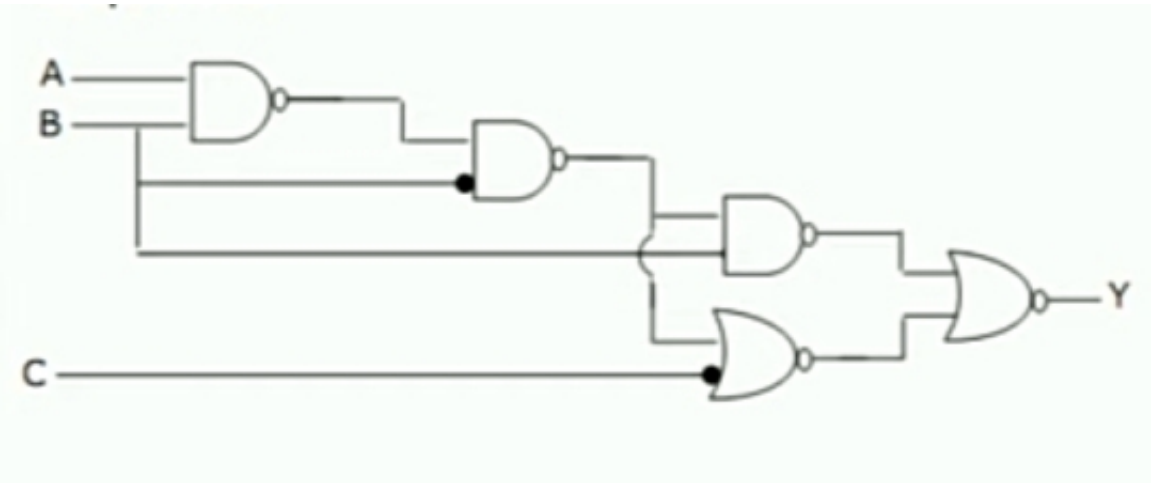
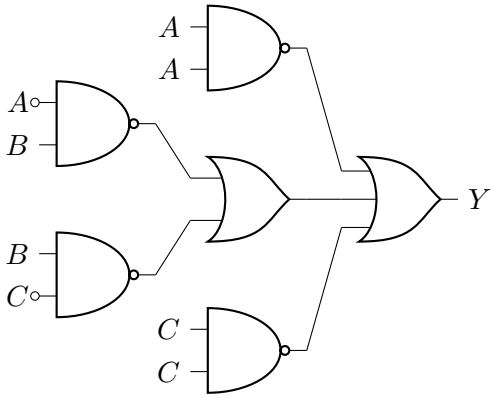


Figure 3.3:

13. Obtain the Boolean Expression for the Logic circuit shown below (GATE EC 1993)



14. Implement Table 3.8 using XNOR logic. (GATE EC 1993)

A	**B**	**Y**
0	0	1
0	1	0
1	0	0
1	1	1

Table 3.8:

15. For a binary half-sub-tractor having two inputs A and B, find the correct set of logical expressions for the outputs D (=A minus B) and X (=borrow). (GATE EC 1999)

16. Find X in the following circuit in Fig. 3.4 (GATE EC 2007)

17. A logic circuit implements the boolean function F=X'.Y+X.Y'.Z'. It is found that the input combination X=Y=1 can never occur. Taking this into account, find a simplified expression for F. (GATE IN 2007)

18. Find the Boolean logic realised by the following circuit in Fig. 3.5 (GATE EC 2010)

19. Find the logic function implemented by the circuit given below in Fig. 3.6 (GATE EC 2011)

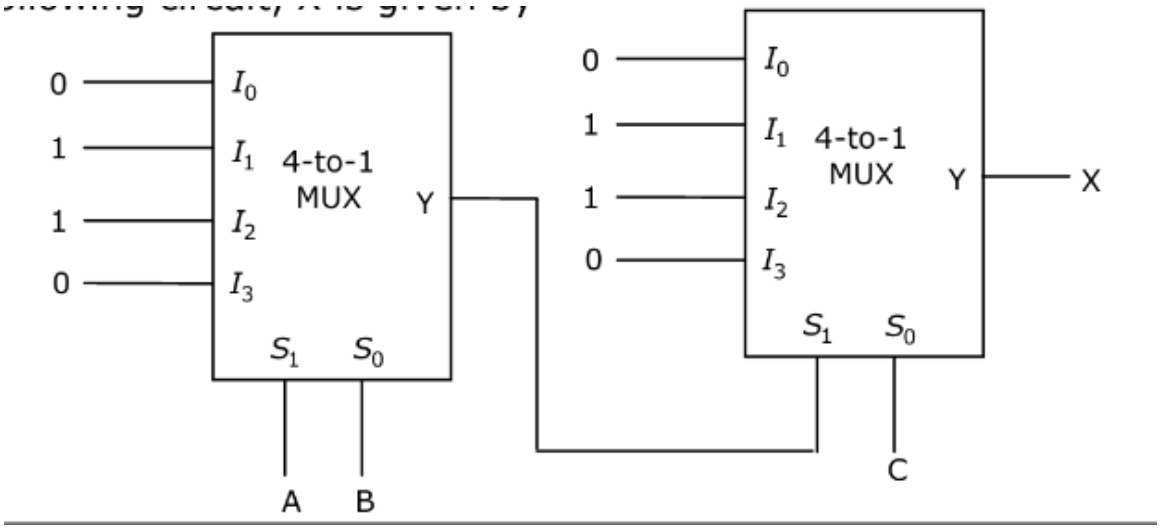


Figure 3.4:

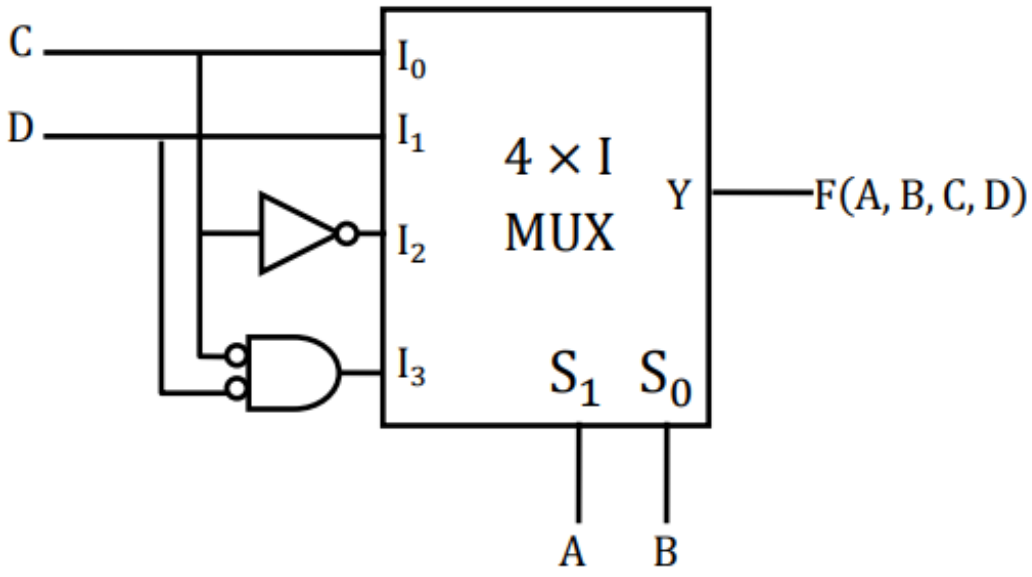


Figure 3.5:

20. Find F in the Digital Circuit given in the figure below in Fig. 3.7. (GATE IN 2016)

21. Find the logic function implemented by the circuit given below in Fig. 3.8 (GATE

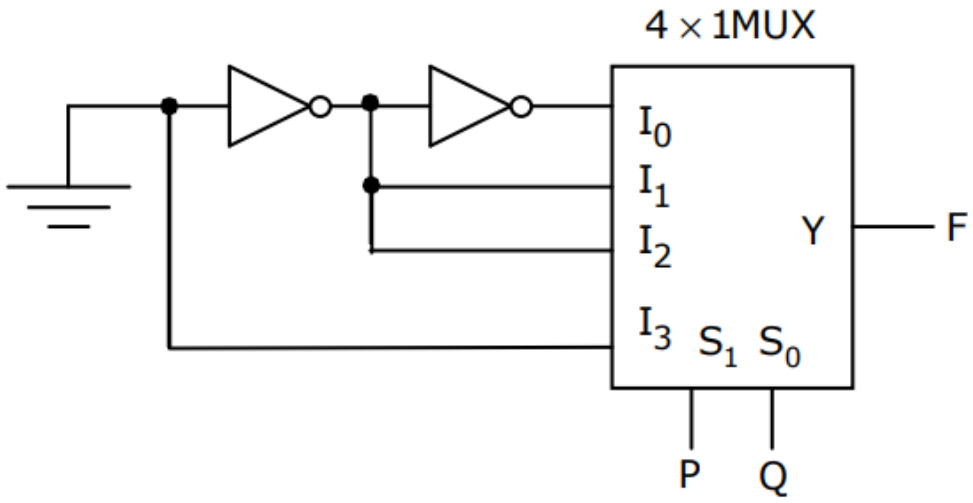


Figure 3.6:

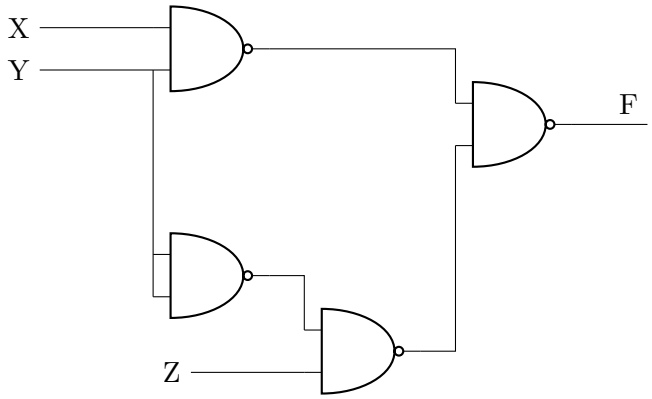


Figure 3.7:

EC 2017)

22. Find the logic function implemented by the circuit given below in Fig. 3.9 (GATE EC 2018)

23. Find the logic function implemented by the circuit given below in Fig. 3.10 (GATE EE 2018)

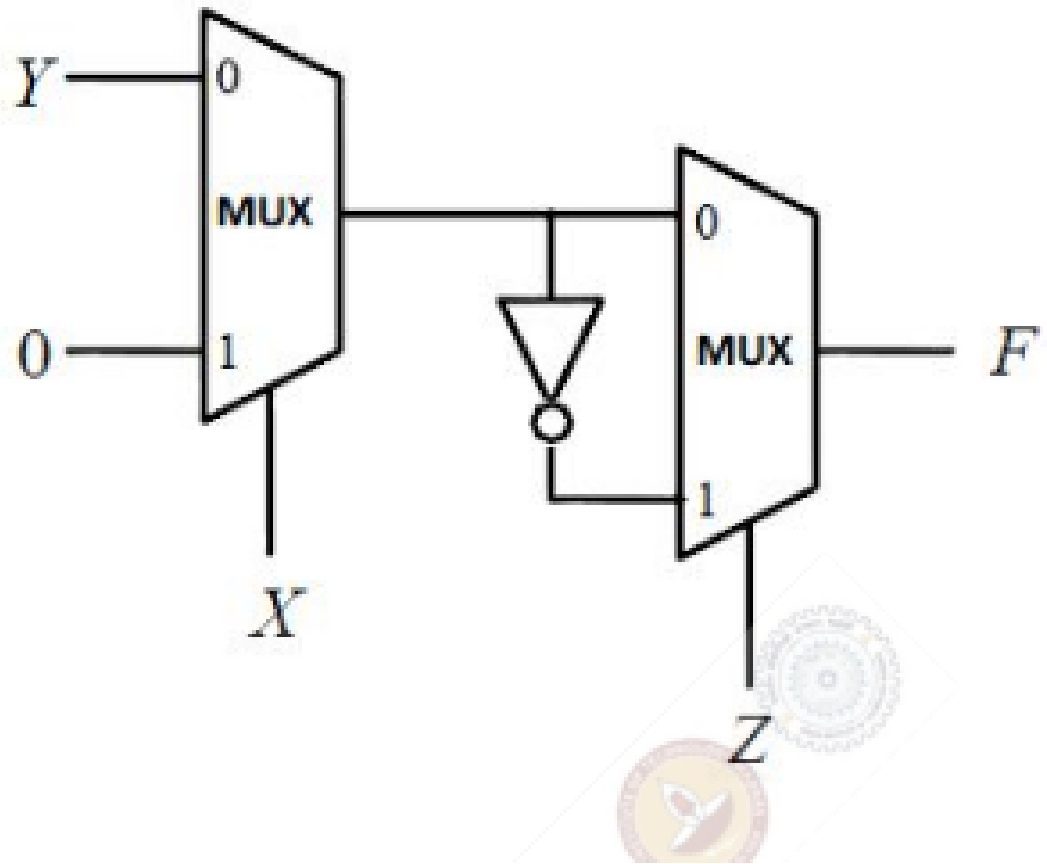


Figure 3.8:

24. Find the logic function implemented by the circuit given below in Fig. 3.11 (GATE EE 2019)

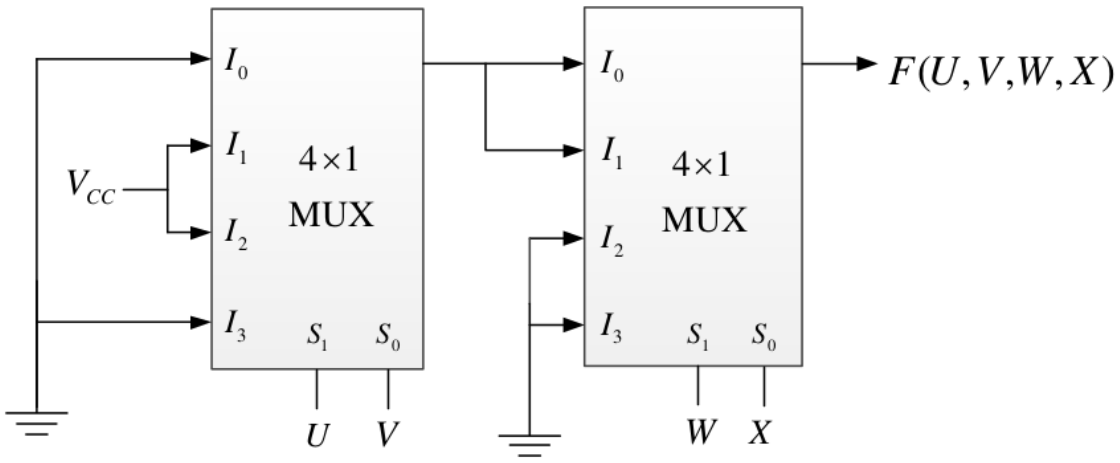


Figure 3.9:

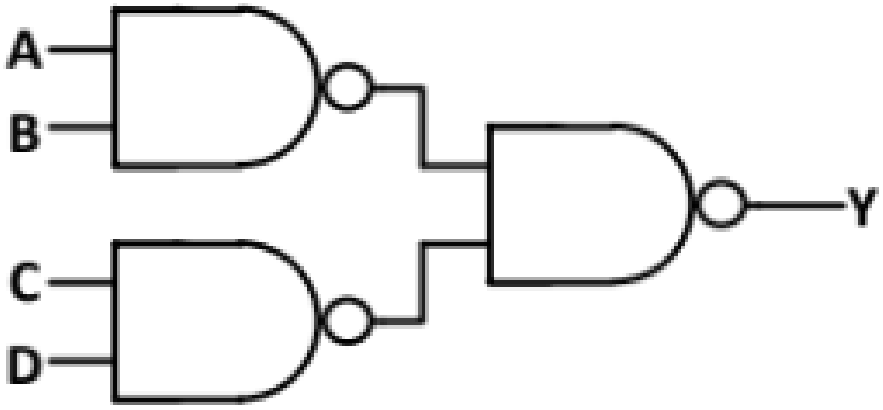


Figure 3.10:

25. Let $\oplus$ and $\odot$ denote the Exclusive OR and Exclusive NOR operations, respectively.Which one of the following is NOT CORRECT ? 25 (GATE CS 2018)

(A) $\overline{P \oplus Q} = P \odot Q$

(B) $\overline{P} \oplus Q = P \odot Q$

(C) $\overline{P} \oplus \overline{Q} = P \oplus Q$

(D) $(P \oplus \overline{P}) \oplus Q = (P \odot \overline{P}) \odot \overline{Q}$

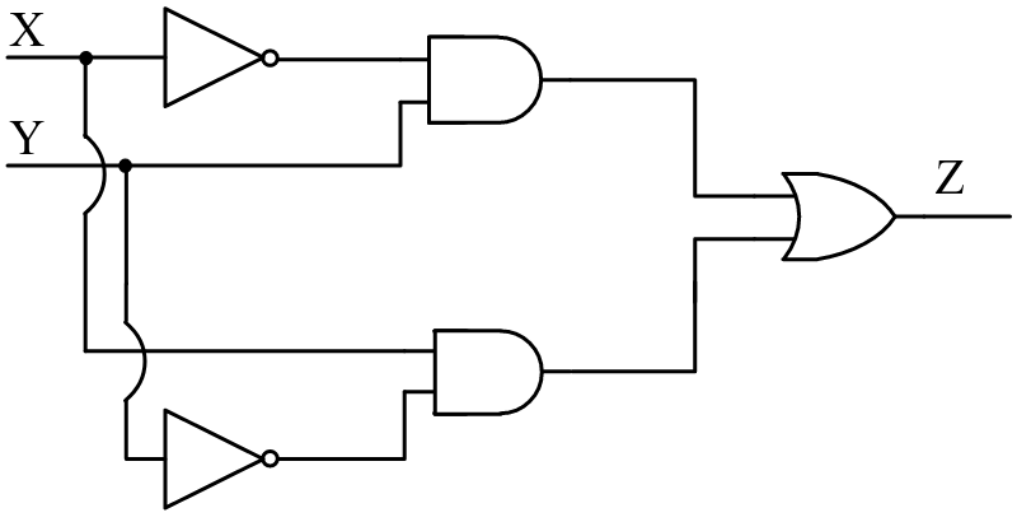


Figure 3.11:

Chapter 4

Karnaugh Map

4.1. Introduction

We explain Karnaugh maps (K-map) by finding the logic functions for the incrementing decoder

4.2. Incrementing Decoder

The incrementing decoder takes the numbers $0, , \ldots, 9$ in binary as inputs and generates the consecutive number as output The corresponding truth table is available in Table 3.5

4.3. Karnaugh Map

Using Boolean logic, output A in Table 3.5 can be expressed in terms of the inputs W, X, Y, Z as

$$A = W'X'Y'Z' + W'XY'Z' + W'X'YZ' + W'XYZ' + W'X'Y'Z \quad (4.1)$$

1. K-Map for A: The expression in (4.1) can be minimized using the K-map in Fig 4.1 In Fig 4.1, the implicants in boxes 0,2,4,6 result in $W'Z'$ The implicants in boxes 0,8 result in $W'X'Y'$ Thus, after minimization using Fig 4.2, (4.1) can be expressed as

$$A = W'Z' + W'X'Y' \tag{4.2}$$

Using the fact that

$$\begin{aligned} X + X' &= \\ XX' &= 0, \end{aligned} \tag{4.3}$$

derive (4.2) from (4.1) algebraically

2. K-Map for B: From Table 3.5, using boolean logic,

$$B = WX'Y'Z' + W'XY'Z' + WX'YZ' + W'XYZ' \tag{4.4}$$

Show that (4.4) can be reduced to

$$B = WX'Z' + W'XZ' \tag{4.5}$$

using Fig 4.2

3. Derive (4.5) from (4.4) algebraically using (4.3)

4. K-Map for C: From Table 3.5, using boolean logic,

$$C = WXY'Z' + W'X'YZ' + WX'YZ' + W'XYZ' \tag{4.6}$$

Show that (4.6) can be reduced to

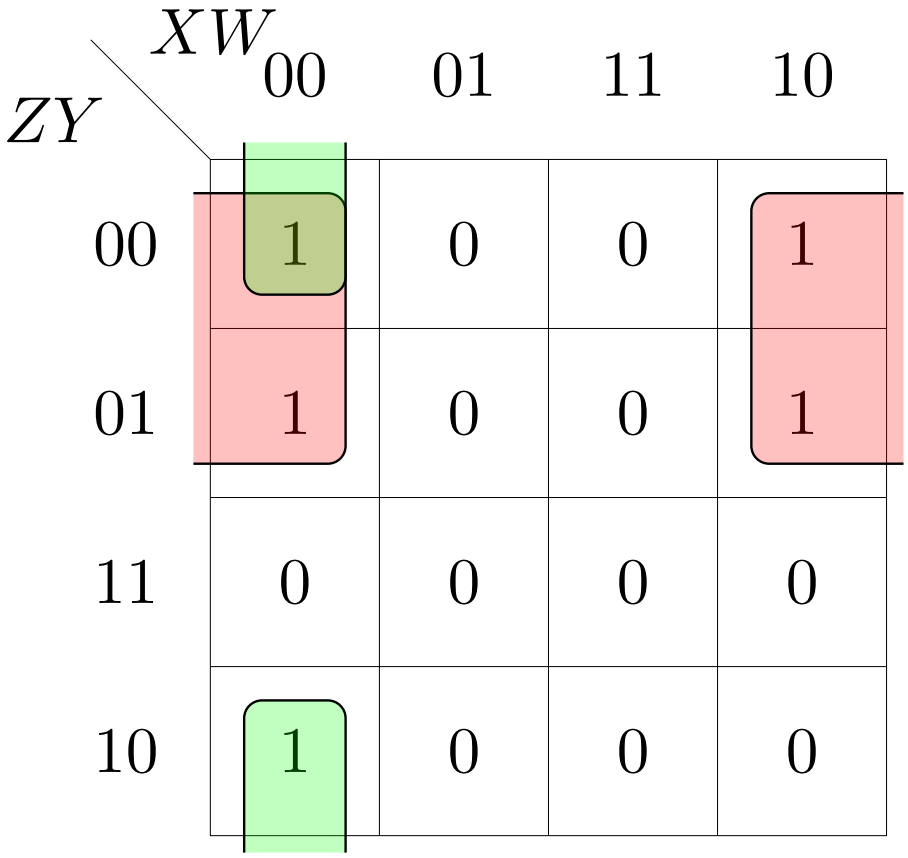


Figure 4.1: K-map for A

$$C = WXY'Z' + X'YZ' + W'YZ' \tag{4.7}$$

using Fig 4.3

5. Derive (4.7) from (4.6) algebraically using (4.3)

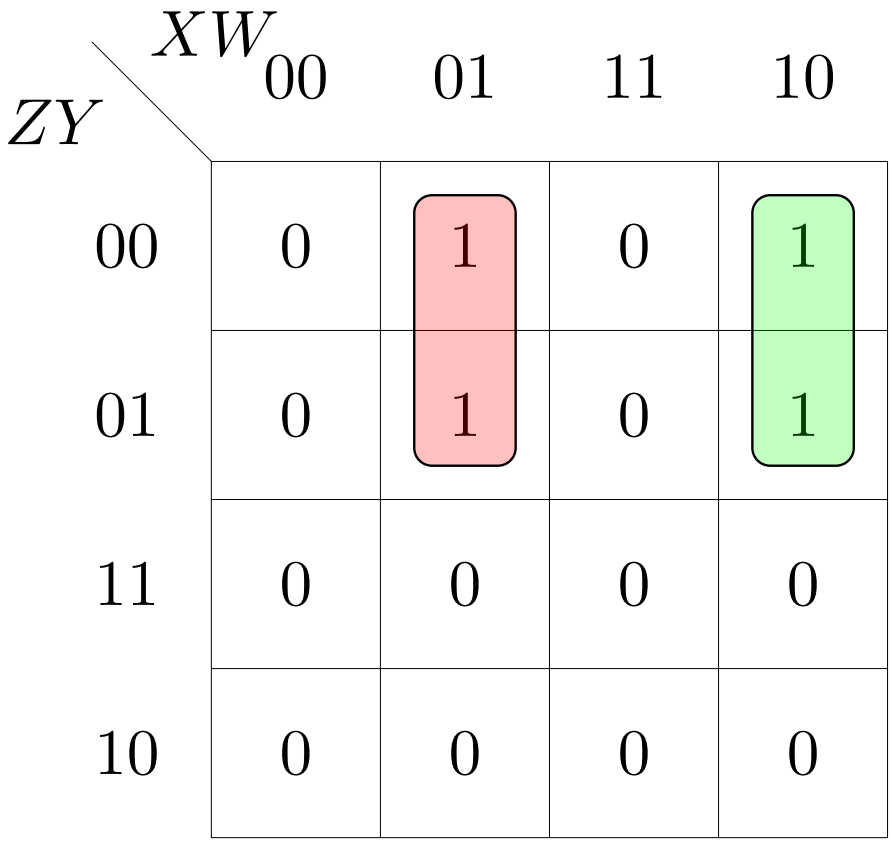


Figure 4.2: K-map for B

6. K-Map for D: From Table 3.5, using boolean logic,

$$D = WXYZ' + W'X'Y'Z \tag{4.8}$$

7. Minimize (4.8) using Fig 4.4

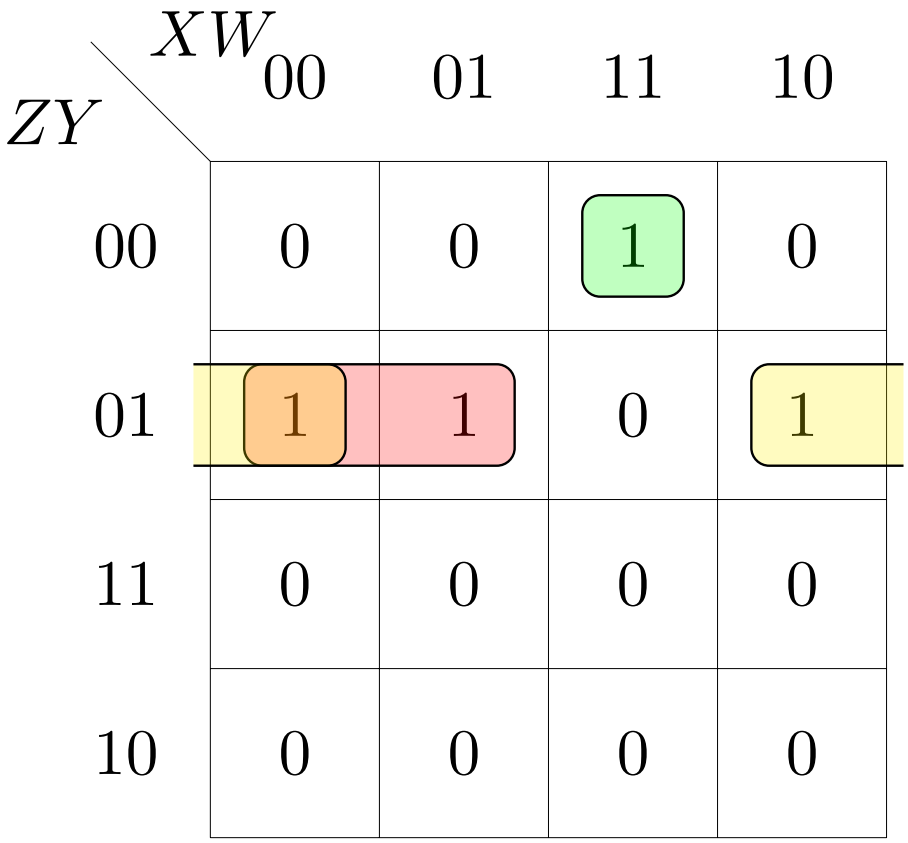


Figure 4.3: K-map for C

8. Execute the code in

ide/7447/codes/inc_dec/inc_dec.cpp

   and modify it using the K-Map equations for A,B,C and D Execute and verify

9. Display Decoder: Table 4.1 is the truth table for the display decoder in Fig. 3.1. Use K-maps to obtain the minimized expressions for a, b, c, d, e, f, g in terms of A, B, C, D

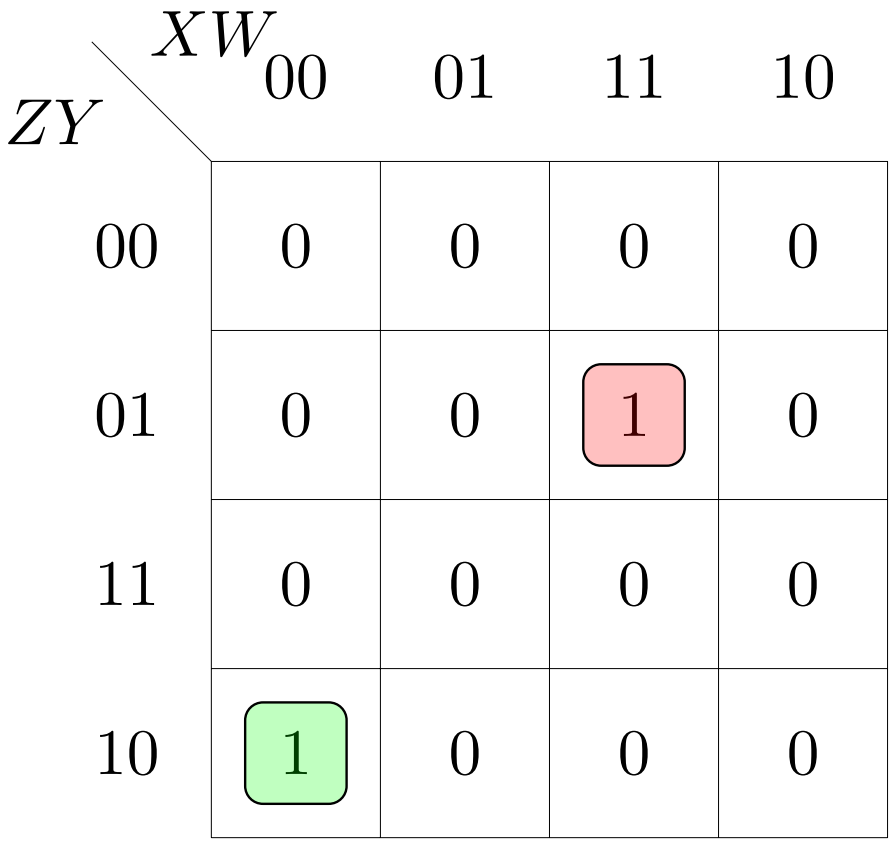


Figure 4.4: K-map for D

with and without don't care conditions

4.4. Dont Care

We explain Karnaugh maps (K-map) using don't care conditions

D	C	B	A	**a**	**b**	**c**	**d**	**e**	**f**	**g**	Decimal
0	0	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	0
0	0	0	1	**1**	**0**	**0**	**1**	**1**	**1**	**1**	1
0	0	1	0	**0**	**0**	**1**	**0**	**0**	**1**	**0**	2
0	0	1	1	**0**	**0**	**0**	**0**	**1**	**1**	**0**	3
0	1	0	0	**1**	**0**	**0**	**1**	**1**	**0**	**0**	4
0	1	0	1	**0**	**1**	**0**	**0**	**1**	**0**	**0**	5
0	1	1	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	6
0	1	1	1	**0**	**0**	**0**	**1**	**1**	**1**	**1**	7
1	0	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	8
1	0	0	1	**0**	**0**	**0**	**1**	**1**	**0**	**0**	9

Table 4.1: Truth table for display decoder.

4.5. Don't Care Conditions

1. Don't Care Conditions: 4 binary digits are used in the incrementing decoder in Table 4.1 However, only the numbers from 0-9 are used as input/output in the decoder and we don't care about the numbers from 0-5 This phenomenon can be addressed by revising the truth table in Table 4.1 to obtain Table 4.2

2. The revised K-map for A is available in Fig 4.5. Show that

$$A = W' \tag{4.9}$$

3. The revised K-map for B is available in Fig 4.6 Show that

$$B = WX'Z' + W'X \tag{4.10}$$

Z	Y	X	W	**D**	**C**	**B**	**A**
0	0	0	0	**0**	**0**	**0**	**1**
0	0	0	1	**0**	**0**	**1**	**0**
0	0	1	0	**0**	**0**	**1**	**1**
0	0	1	1	**0**	**1**	**0**	**0**
0	1	0	0	**0**	**1**	**0**	**1**
0	1	0	1	**0**	**1**	**1**	**0**
0	1	1	0	**0**	**1**	**1**	**1**
0	1	1	1	**1**	**0**	**0**	**0**
1	0	0	0	**1**	**0**	**0**	**1**
1	0	0	1	**0**	**0**	**0**	**0**
1	0	1	0	**-**	**-**	**-**	**-**
1	0	1	1	**-**	**-**	**-**	**-**
1	1	0	0	**-**	**-**	**-**	**-**
1	1	0	1	**-**	**-**	**-**	**-**
1	1	1	0	**-**	**-**	**-**	**-**
1	1	1	1	**-**	**-**	**-**	**-**

Table 4.2:

4. The revised K-map for C is available in Fig 4.7 Show that

$$C = X'Y + W'Y + WXY' \tag{4.11}$$

5. The revised K-map for D is available in Fig 4.8 Show that

$$D = W'Z + WXY \tag{4.12}$$

6. Verify the incrementing decoder with don't care conditions using the arduino

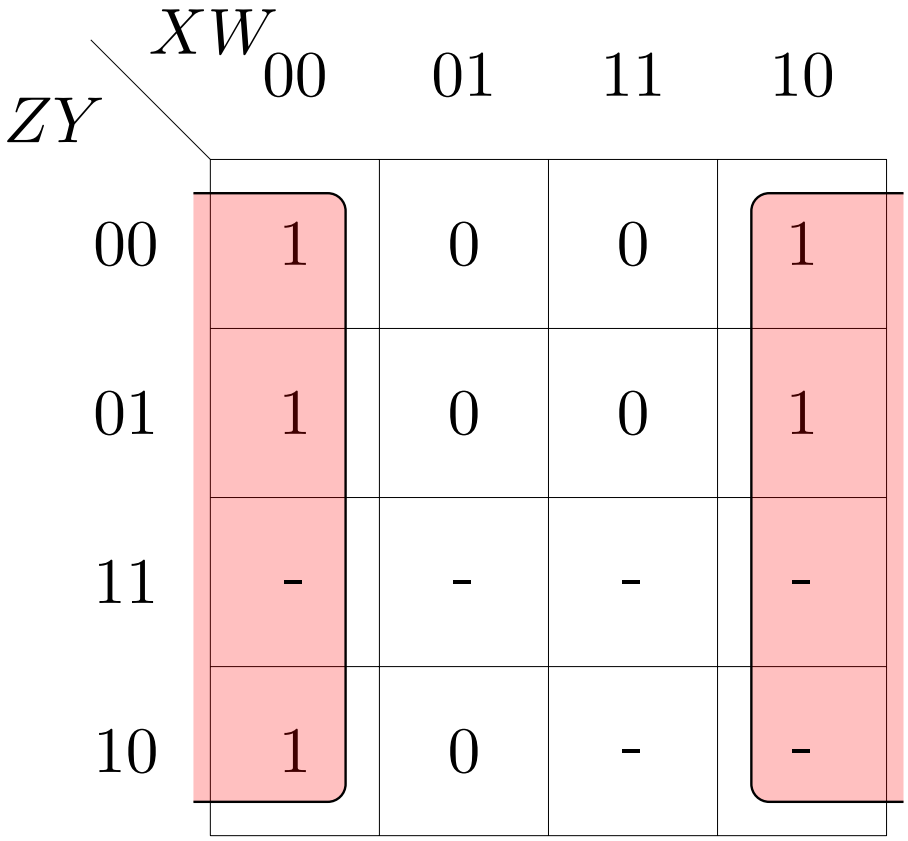


Figure 4.5: K-map for A with don't cares

7. Display Decoder: Use K-maps to obtain the minimized expressions for a, b, c, d, e, f, g in terms of A, B, C, D with don't care conditions

8. Verify the display decoder with don't care conditions using arduino

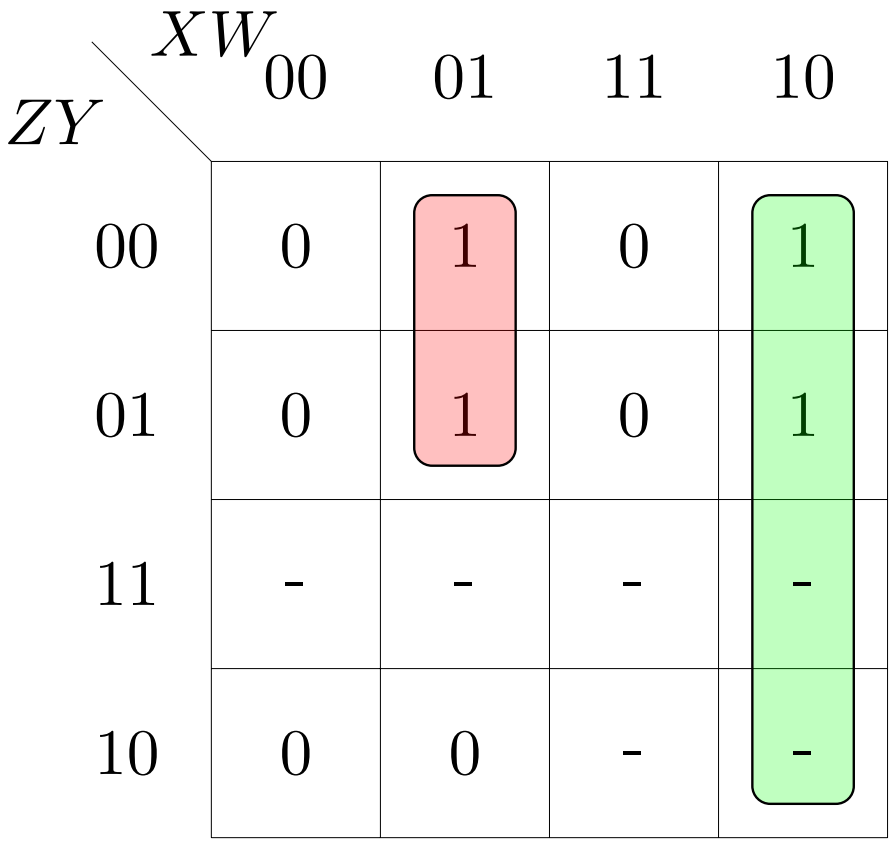


Figure 4.6: K-map for B with don't cares

4.6. Problems

1. Obtain the Minimal Form for the Boolean Expression (CBSE 2013)

$$H(P, Q, R, S) = \sum(0, 1, 2, 3, 5, 7, 8, 9, 10, 14, 15) \tag{4.13}$$

2. Write the POS form for the function G shown in Table 4.3. (CBSE 2013)

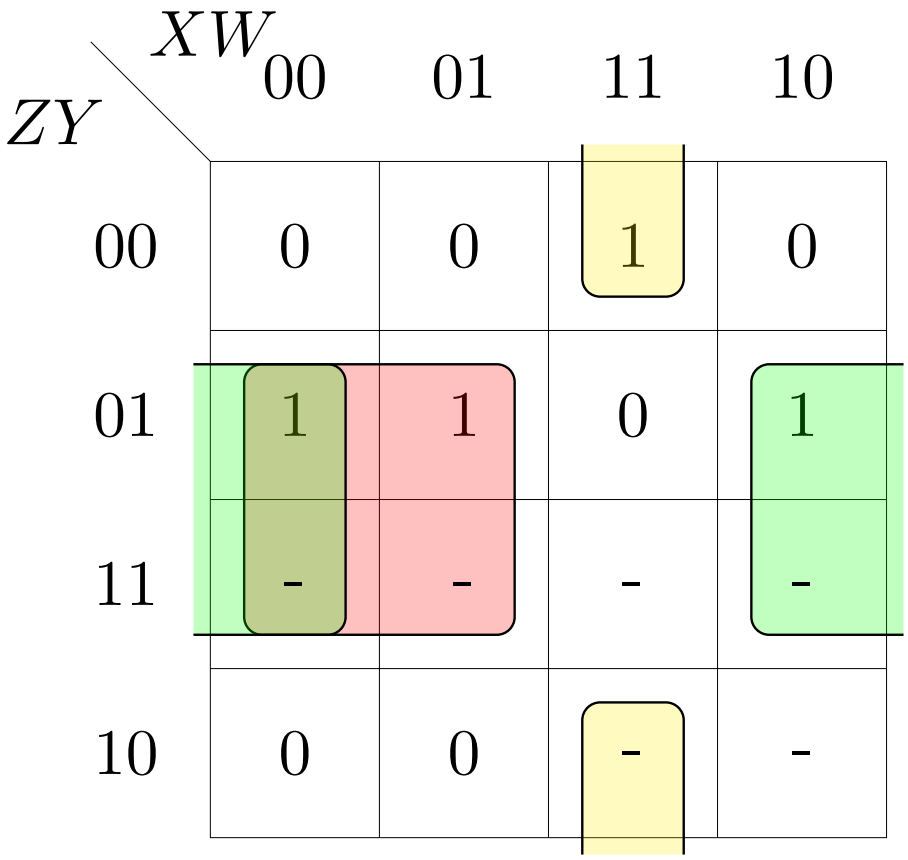


Figure 4.7: K-map for C with don't cares

3. Reduce the following Boolean Expression to its simplest form using K-Map (CBSE 2015)

$$F(X, Y, Z, W) = (0, 1, 4, 5, 6, 7, 8, 9, 11, 15) \tag{4.14}$$

4. Derive a Canonical POS expression for a Boolean function F, represented by the

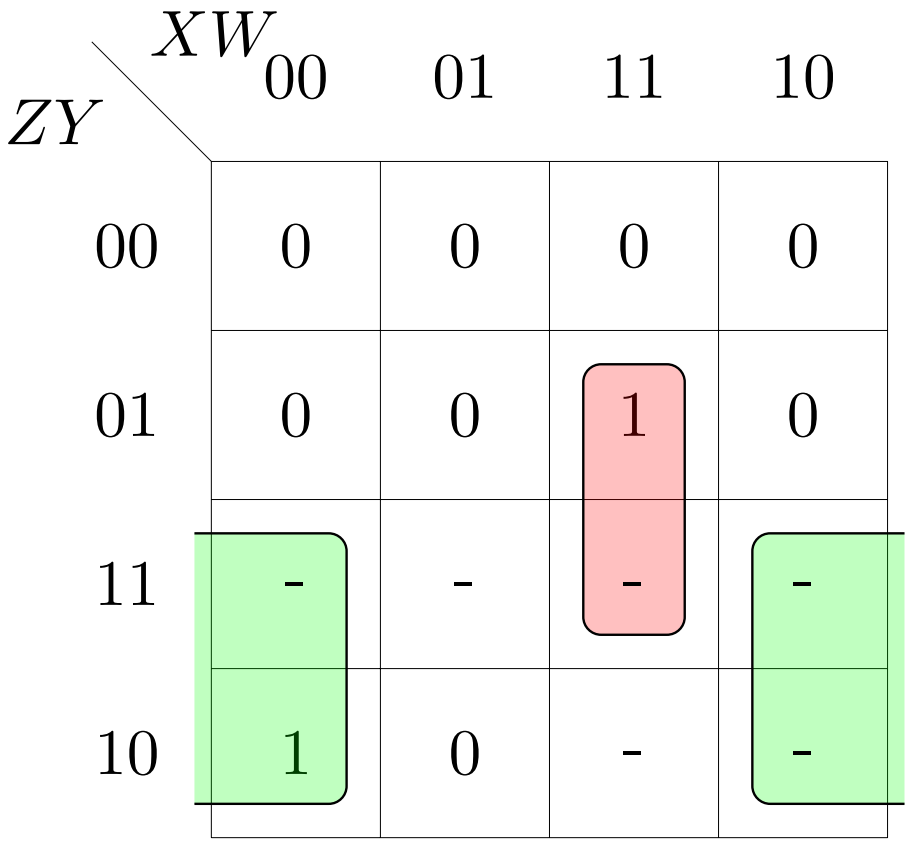


Figure 4.8: K-map for D with don't cares

following truth table (CBSE 2015)

5. (CBSE 2015) Reduce the following Boolean Expression to its simplest form using K-map

$$F(X, Y, Z, W) = \sum(0, 1, 6, 8, 9, 10, 11, 12, 15) \tag{4.15}$$

U	V	W	G
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Table 4.3:

X	Y	Z	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Table 4.4:

6. Reduce the following Boolean Expression to its simplest form using K-map. (CBSE 2016)

$$F(X, Y, Z, W) = \sum(2, 6, 7, 8, 9, 10, 11, 13, 14, 15) \tag{4.16}$$

7. Derive a Canonical POS expression for a Boolean function F, represented in Table 4.5 (CBSE 2016)

P	Q	R	F(P, Q, R)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Table 4.5:

8. Verify the following (CBSE 2016)

$$A' + B'C = A'B'C' + A'BC' + A'BC + A'B'C + AB'C \tag{4.17}$$

9. Reduce the following boolean expression to it's simplest form using K-Map (CBSE 2017)

$$F(X, Y, Z, W) = \sum(0, 1, 2, 3, 4, 5, 10, 11, 14) \tag{4.18}$$

10. Reduce the following Boolean Expression to its simplest form using K-Map. (CBSE 2017)

$$E(U, V, Z, W) = (2, 3, 6, 8, 9, 10, 11, 12, 13) \tag{4.19}$$

11. Derive a canonical POS expression for a Boolean function G, represented by Table 4.6 (CBSE 2017)

12. Derive a canonical POS expression for a Boolean function FN, represented by Table

X	Y	Z	G(X,Y,Z)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Table 4.6:

4.7. (CBSE 2018)

X	Y	Z	FN(X,Y,Z)
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Table 4.7:

13. Reduce the following Boolean expression in the simplest form using K-Map.

$$F(P,Q,R,S) = \sum(0,1,2,3,5,6,7,10,14,15) \tag{4.20}$$

(CBSE 2019)

14. Fig. 4.9 below shows a muliplexer where S0 and S1 are the select lines, I0 to I3 are the input lines, EN is the enable line and F(P,Q,R) is the output. Find the boolean

expression for output F as function of inputs P,Q,R using K-map. (GATE EC 2020)

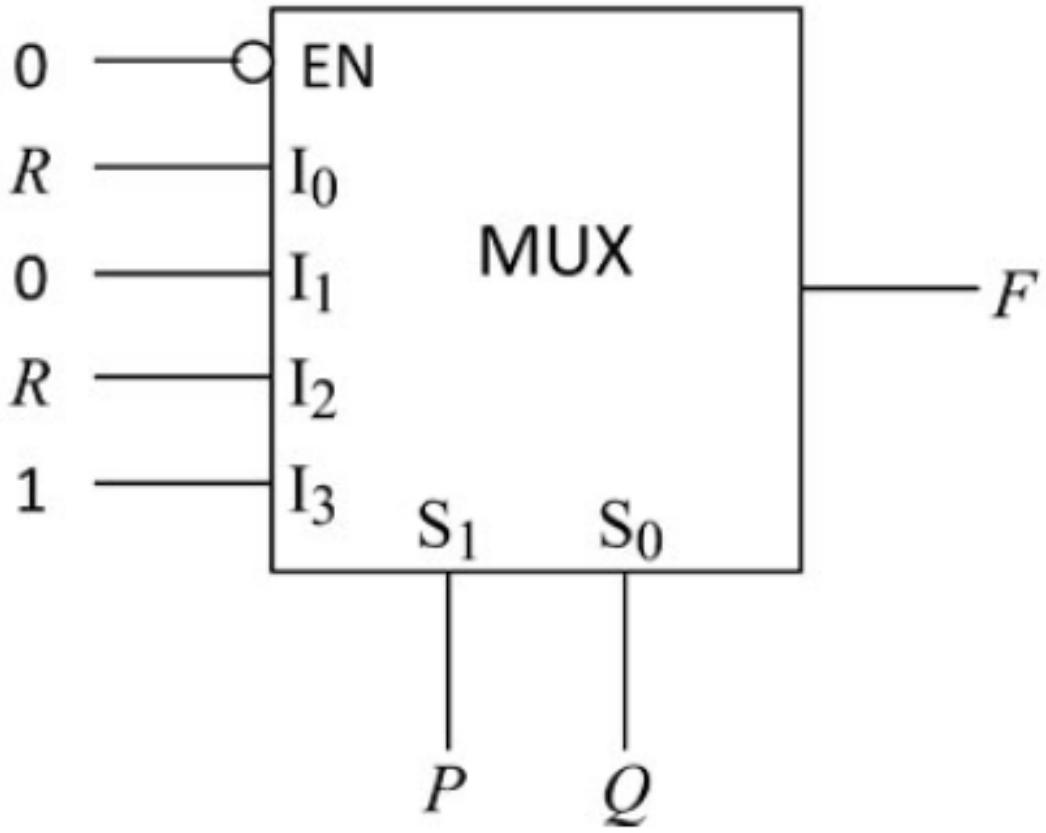


Figure 4.9:

15. The four variable function f is given in terms of min-terms as

$$f(A, B, C, D) = \sum m(2, 3, 8, 10, 11, 12, 14, 15) \tag{4.21}$$

Using the K-map minimize the function in the sum of products form. (GATE EC 1991)

16. Find the logic realized by the circuit in Fig. 4.10. (GATE EC 1992)

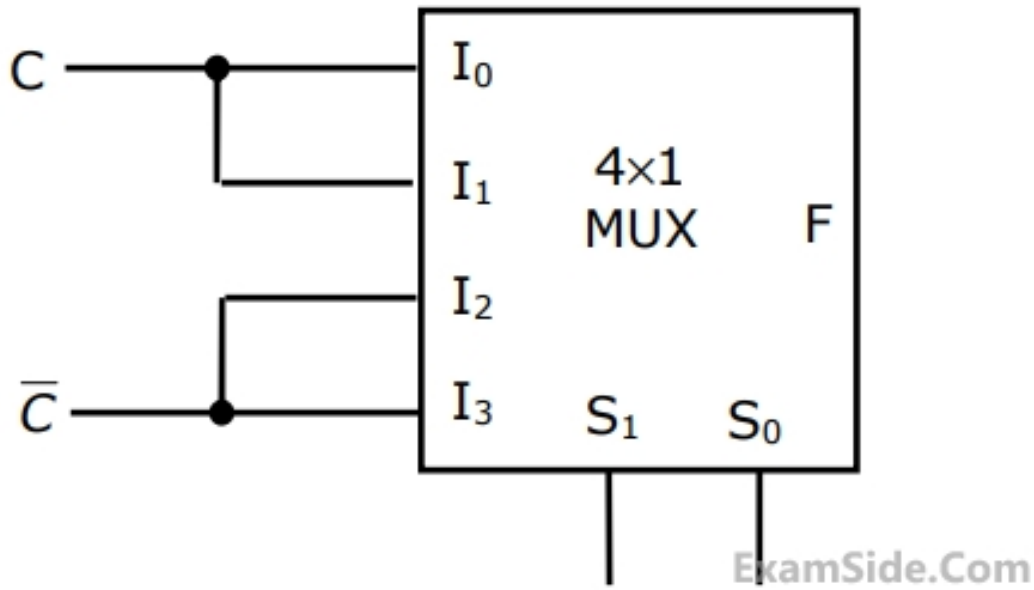


Figure 4.10:

17. A combinational circuit has three inputs A, B and C and an output F. F is true only for the following input combinations. (GATE EC 1992)

    (a) A is false and B is true

    (b) A is false and C is true

    (c) A, B and C are all false

    (d) A, B and C are all true

    (a) Write the truth table for F. use the convention, true = 1 and false = 0.

(b) Write the simplified expression for F as a Sum of Products.

(c) Write the simplified expression for F as a product of Sums.

18. Draw the logic circuit for Table 4.8 using only NOR gates. (GATE EC 1993)

C	**B**	**A**	**Y**
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Table 4.8:

19. Implement the following Boolean function in a 8x1 multiplexer. (GATE EC 1993)

$$Q = BC + ABD' + A'C'D \tag{4.22}$$

20. Minimize the following Boolean function in 4.23.

$$F = A'B'C' + A'BC' + A'BC + ABC' \tag{4.23}$$

21. Find the Boolean expression for Table 4.9. (GATE EC 2005)

22. Minimize the logic function represented by the following Karnaugh map. (CBSE

A	**B**	**C**	**X**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Table 4.9:

		YZ			
		00	01	11	10
X	0	1	1	1	0
	1	0	0	1	0

2021)

23. Find the output for the Karnaugh map shown below (GATE EE 2019)

		PQ			
		00	01	11	10
RS	00	0	1	1	0
	01	1	1	1	1
	11	1	1	1	1
	10	0	0	0	0

24. The propogation delays of the XOR gate, AND gate and multiplexer (MUX) in the

circuit shown in the Fig. 4.11 are 4 ns, 2 ns and 1 ns, respectively. If all the inputs P, Q, R, S and T are applied simultaneously and held constant, the maximum propogation delay of the circuit is (Gate EC-2021)

(a) 3 ns

(b) 5 ns

(c) 6 ns

(d) 7 ns

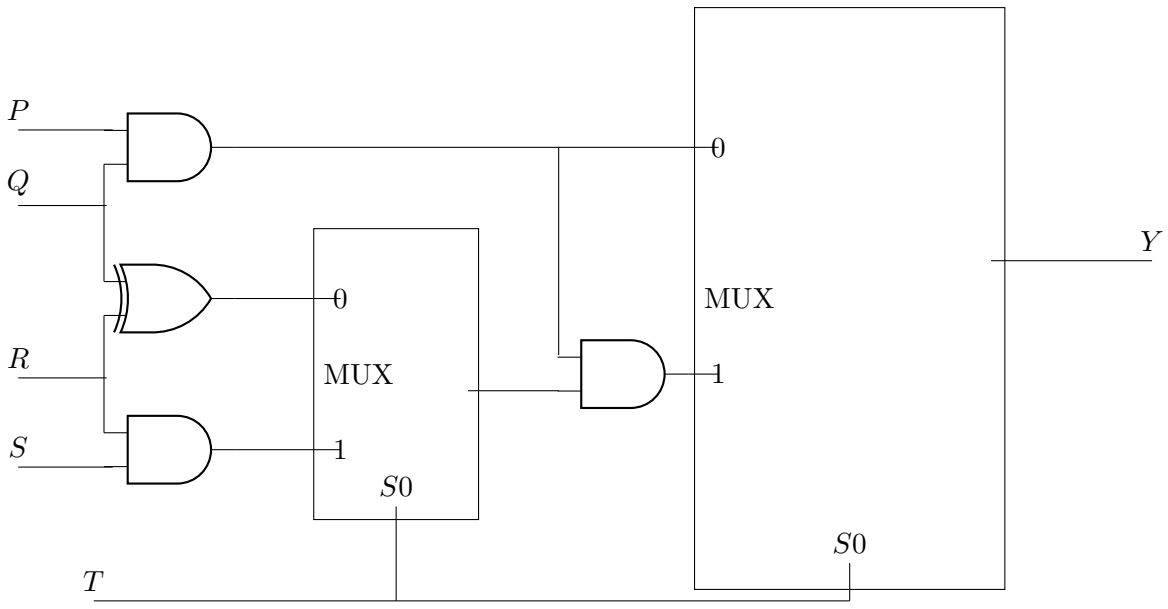


Figure 4.11:

25. Consider the 2-bit multiplexer(MUX) shown in the figure. For output to be the XOR of R and S, the values for W, X, Y and Z are ? (GATE EC-2022)

(a) $W = 0, X = 0, Y = 1, Z = 1$

(b) $W = 1, X = 0, Y = 1, Z = 0$

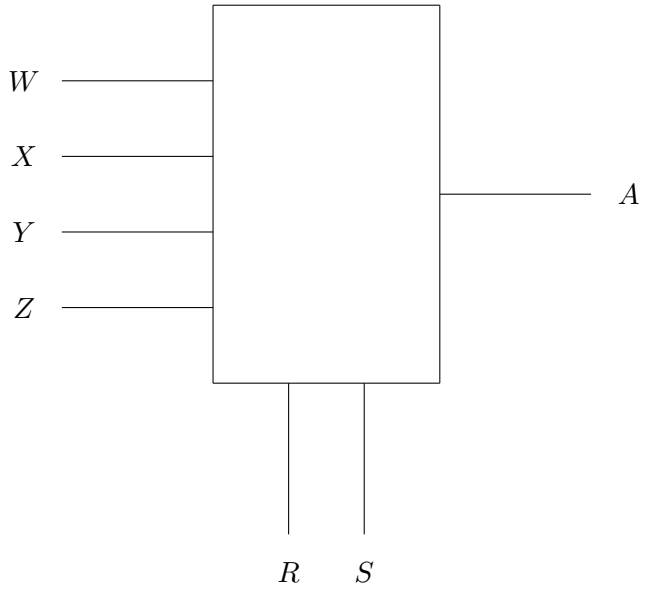


Figure 4.12:

(c) $W = 0, X = 1, Y = 1, Z = 0$

(d) $W = 1, X = 1, Y = 0, Z = 0$

26. $A = a_1a_0$ and $B = b_1b_0$ are two 2-bit unsigned binary numbers. If $F(a_1, a_0, b_1, b_0)$ is a Boolean function such that $F = 1$ only when $A > B$, and $F = 0$ otherwise, then F can be minimized to the form _____. (GATE IN-2022)

27. The logic block shown has an output F given by _____. (GATE IN 2022)

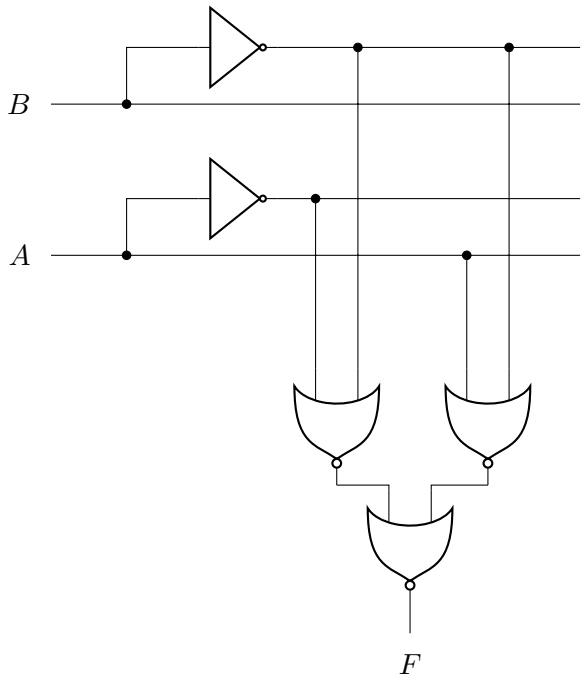


Figure 4.13: Circuit

(a) $A + B$

(b) $A.\bar{B}$

(c) $A + \bar{B}$

(d) $\bar{B}$

28. A 4×1 multiplexer with two selector lines is used to realize a Boolean function F having four Boolean variables X, Y, Z, and W as shown below. S_0 and S_1 denote the least significant bit (LSB) and most significant bit (MSB) of the selector lines of the multiplexer, respectively. I_0, I_1, I_2, I_3 are the input lines of the multiplexer.

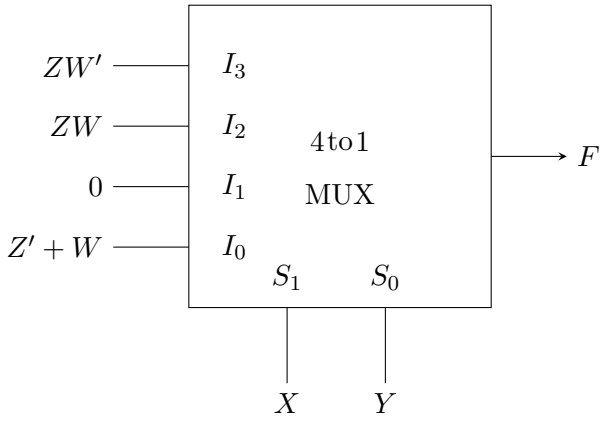


Figure 4.14: 4×1 multiplexer

(GATE IN-2021)

The canonical sum of product representation of F is:

(A) $F(X, Y, Z, W) = \Sigma m(0, 1, 3, 14, 15)$

(B) $F(X, Y, Z, W) = \Sigma m(0, 1, 3, 11, 14)$

(C) $F(X, Y, Z, W) = \Sigma m(2, 5, 9, 11, 14)$

(D) $F(X, Y, Z, W) = \Sigma m(1, 3, 7, 9, 15)$

29. The output expression for the Karnaugh map shown below is (GATE EE 2019)

RS \ PQ	00	01	11	10
00	0	1	1	0
01	1	1	1	1
11	1	1	1	1
10	0	0	0	0

Figure 4.15:

(a) QR'+S

(b) QR+S

(c) QR'+S'

(d) QR+S'

30. In the circuit shown below , X and Y are digital inputs, and Z is a digital output. The quivalent circuit is a (GATE EE 2019)

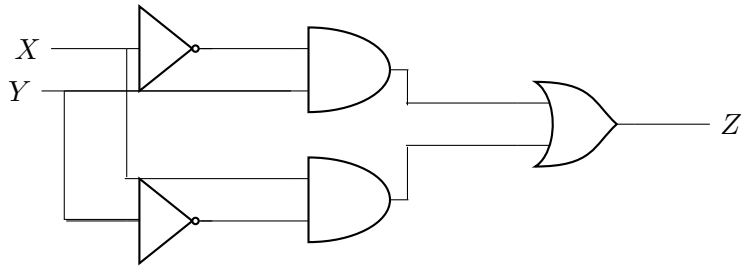


Figure 4.16:

(a) NAND gate

(b) NOR gate

(c) XOR gate

(d) XNOR gate

31. The output F of the digital circuit shown can be written in the form(s)_____ (GATE IN 2022)

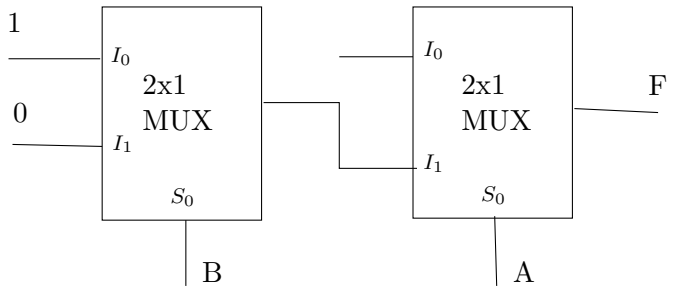


Figure 4.17:

(a) $\overline{A \cdot B}$

(b) $\overline{A}+\overline{B}$

(c) $\overline{A + B}$

(d) $\overline{A} \cdot \overline{B}$

32. If $X = X_1X_0$ and $Y = Y_1Y_0$ are 2-bit binary numbers. The Boolean function S that satisfies the condition "If $X>Y$, then $S = 1$", in its minimized form, is ?

(a) $X_1Y_1+X_0Y_0$

(b) $X_1\overline{Y_1} + X_0\overline{Y_0Y_1} + X_0\overline{Y_0}X_1$

(c) $X_1\overline{Y_1}X_0\overline{Y_0}$

(d) $X_1Y_1 + X_0\overline{Y_0}Y_1 + X_0\overline{Y_0X_1}$

(GATE IN 2019)

33. The figure below shows the i^{th} full-adder block of a binary adder circuit.C_i is the input carry and C_{i+1} is the output carry of the circuit. Assume that each logic gate has a delay of 2 nanosecond, with no additional time delay due to the interconnecting wires. Of the inputs A_i , B_i are available and stable throughout the carry propagation, the maximum time taken for an input C_i to produce a steady-state output C_{i+1} is _____ nanosecond. (GATE IN 2019)

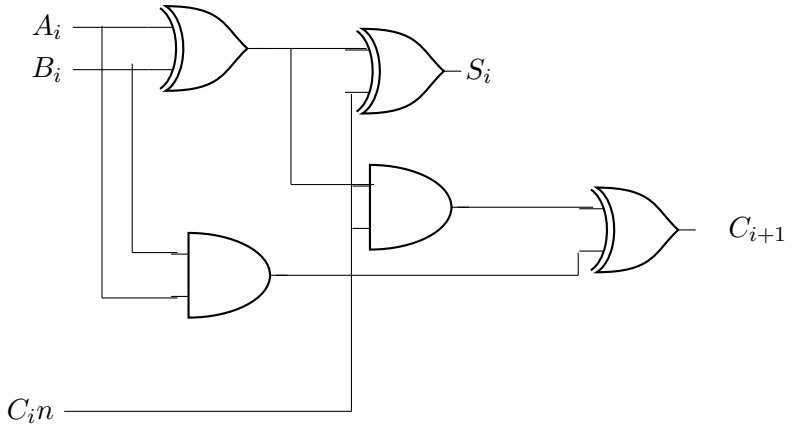


Figure 4.18:

34. The Product of sun expression of a Boolean function $F(A, B, C)$ three variables is given by

$$F(A, B, C) = (A + B + \overline{C}) \times (A + \overline{B} + \overline{C} \times (\overline{A} + B + C) \times (\overline{A} + \overline{B} + \overline{C}) \quad (4.24)$$

The canonical sum of product expression of $F(A, B, C)$ is given by

(a) $\overline{A}\overline{B}C + \overline{A}BC + A\overline{B}\overline{C} + ABC$

(b) $\overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + A\overline{B}C + AB\overline{C}$

(c) $AB\overline{C} + A\overline{BC} + \overline{A}BC + \overline{ABC}$

(d) $\overline{ABC} + \overline{A}BC + AB\overline{C} + ABC$

(GATE IN 2018)

35. A four-variable Boolean function is realized using 4×1 multiplexers as shown in the figure.

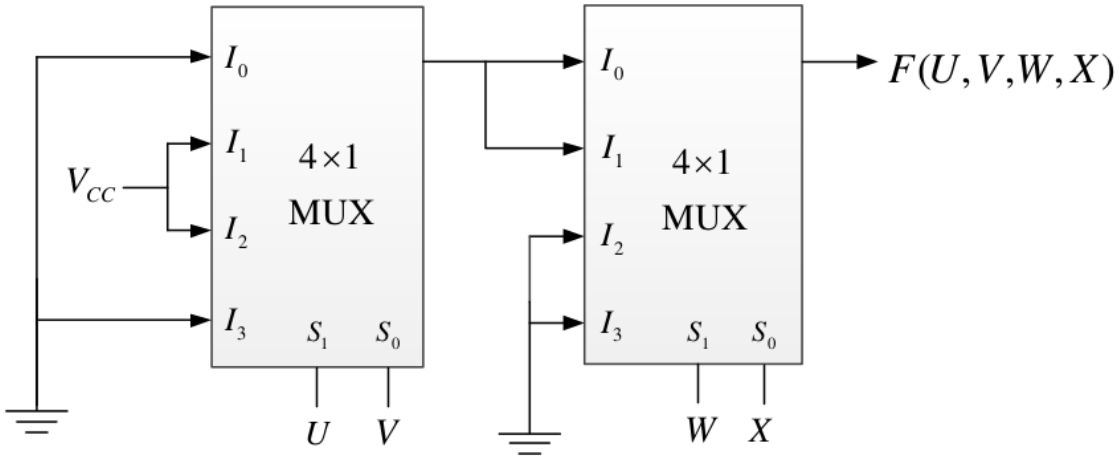


Figure 4.19:

The minimized expression for

(a) $\left(UV + \bar{U}\bar{V}\right)\bar{W}$

(b) $\left(UV + \bar{U}\bar{V}\right)\left(\bar{W}\bar{X} + \bar{W}X\right)$

(c) $\left(U\bar{V} + \bar{U}V\right)\bar{W}$

(d) $\left(U\bar{V} + \bar{U}V\right)\left(\bar{W}\bar{X} + \bar{W}X\right)$

(GATE EC 2018)

36. A function $F(A, B, C)$ defined by three Boolean variables A, B and C when expressed as sum of products is given by

$F = \left(\overline{A} \cdot \overline{B} \cdot \overline{C}\right) + \left(\overline{A} \cdot B \cdot \overline{C}\right) + \left(A \cdot \overline{B} \cdot \overline{C}\right)$ where, $\overline{A}, \overline{B}$ and $\overline{C}$ are the complements of the respective variables.The product of sums (POS) form of the function F is

(A) $(A + B + C) \cdot \left(A + \overline{B} + C\right) \cdot \left(\overline{A} + B + C\right)$

(B) $\left(\overline{A} + \overline{B} + \overline{C}\right) \cdot \left(\overline{A} + B + \overline{C}\right) \cdot \left(A + \overline{B} + \overline{C}\right)$

(C) $\left(A + B + \overline{C}\right) \cdot \left(A + \overline{B} + \overline{C}\right) \cdot \left(\overline{A} + B + \overline{C}\right) \cdot \left(\overline{A} + \overline{B} + C\right) \cdot \left(\overline{A} + \overline{B} + C\right)$

(D) $\left(\overline{A} + \overline{B} + C\right) \cdot \left(\overline{A} + B + C\right) \cdot \left(A + \overline{B} + C\right) \cdot \left(A + B + \overline{C}\right) \cdot (A + B + C)$

(GATE EC 2018)

37. In the Karnaugh map shown below, X denotes a don't care term. What is the minimal form of the function represented by the Karnaugh map?

cd \ ba	00	01	11	10
00	1	1	0	1
01	X	0	0	0
11	X	0	0	0
10	1	1	0	X

(A) $b'd' + a'd'$

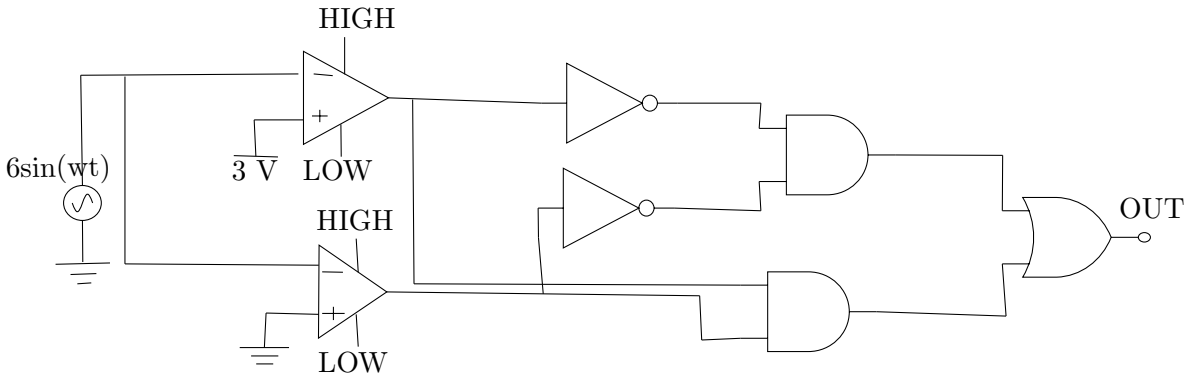
(B) $a'b' + b'd' + a'bd'$

(C) $b'd' + a'bd'$

(D) $a'b' + b'd' + a'd'$

(GATE EC 2008)

38. In the circiut shown below , assume that the comparators are ideal and all components have zero propagation delay . In one period of the input signal Vin=6sin(wt),the fraction of the time which the output OUT is in login state HIGH is



(a) $\frac{1}{12}$

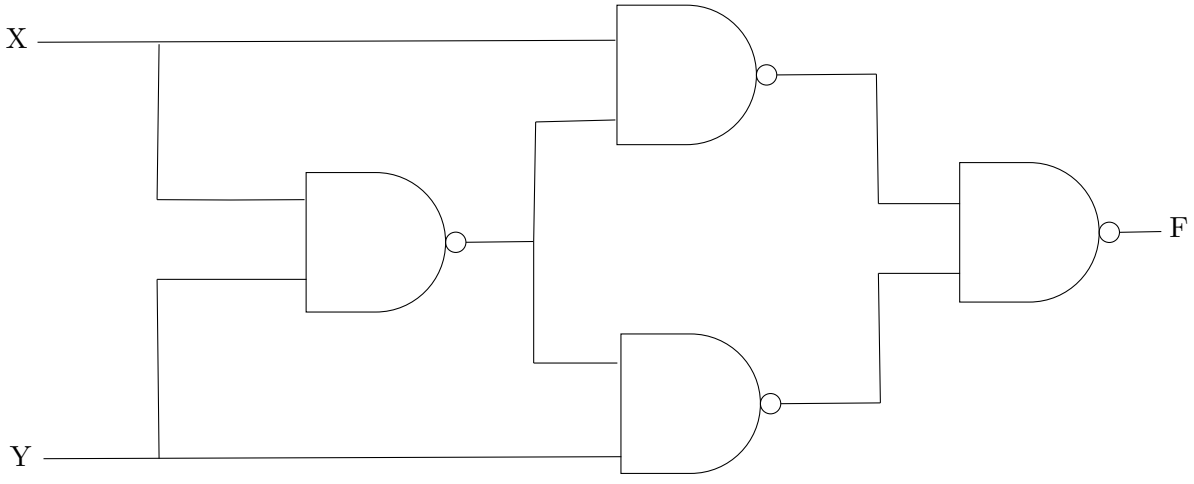
(b) $\frac{1}{2}$

(c) $\frac{2}{3}$

(d) $\frac{5}{6}$

(GATE EC 2018)

39. The Boolean function $F(X, Y)$ realized by the given circuit is



(a) $\bar{X}Y + X\bar{Y}$

(b) $\bar{X}\bar{Y} + XY$

(c) $X + Y$

(d) $\bar{X}.\bar{Y}$

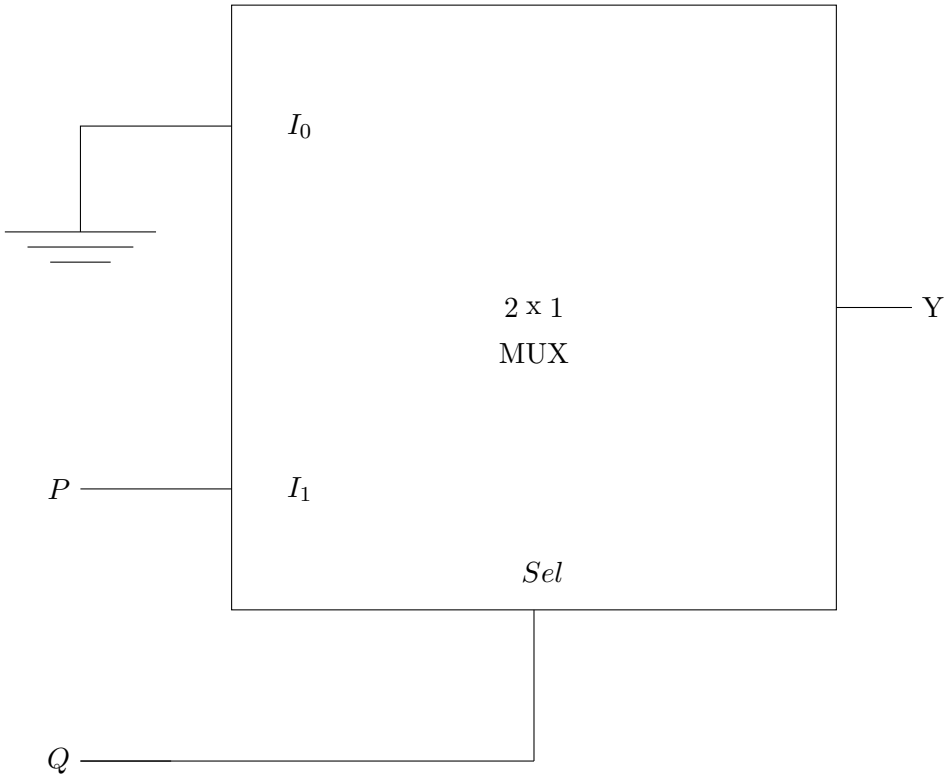
(GATE IN 2019)

40. Consider the minterm list form of a Boolean function given below.

$$F(P, Q, R, S) = \sum m(0, 2, 5, 7, 9, 11) + d(3, 8, 10, 12, 14)$$

Here, denotes a minterm and denotes a don't care term. The number of essential prime implicants of the function is (GATE CS 2018)

41. In the circuit shown below, P and Q are the inputs. The logical function realized by the circuit shown below



(a) Y=PQ

(b) Y=P+Q

(c) Y= $\overline{PQ}$

(d) Y= $\overline{P+Q}$

(GATE EC2023,23)

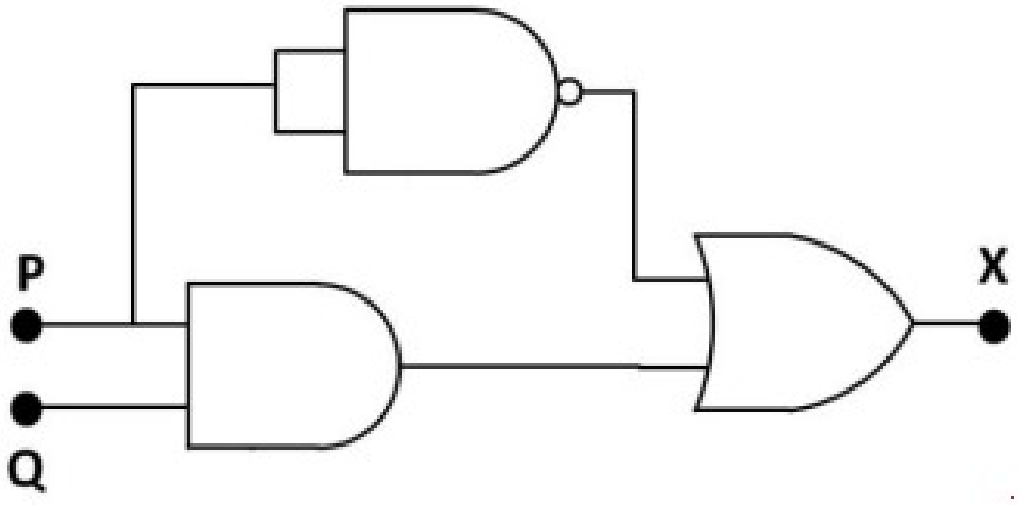


Figure 4.20: k-maps

Fig. 1

(a) P = 1, Q = 1; X = 0

(b) P = 1, Q = 0; X = 0

(c) P = 0, Q = 1; X = 0

(d) P = 0, Q = 0; X = 1

(GATE PH2023,24)

Chapter 5

7474

We show how to use the 7474 D-Flip Flop ICs in a sequential circuit to realize a decade counter.

5.1. Components

Component	Value	Quantity
Breadboard		1
Resistor	$\geq 220\Omega$	1
Arduino	Uno	1
Seven Segment Display	Common Anode	1
Decoder	7447	1
Flip Flop	7474	2
Jumper Wires		20

Table 5.1:

5.2. Decade Counter

1. Generate the CLOCK signal using the **blink** program.

	INPUT				**OUTPUT**				CLOCK		5V			
	W	X	Y	Z	A	B	C	D						
Arduino	D6	D7	D8	D9	D2	D3	D4	D5	D13					
7474	5	9			2	12			CLK1	CLK2	1	4	10	13
7474			5	9			2	12	CLK1	CLK2	1	4	10	13
7447					7	1	2	6			16			

Table 5.2:

2. Connect the Arduino, 7447 and the two 7474 ICs according to Table 5.2 and Fig. 5.2.

   The pin diagram for 7474 is available in Fig. 5.1

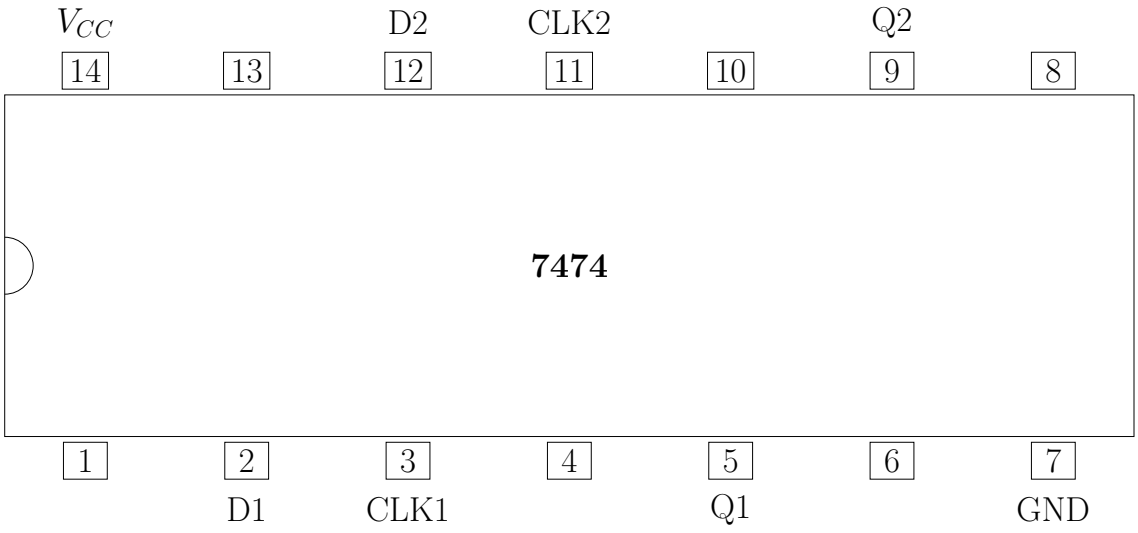


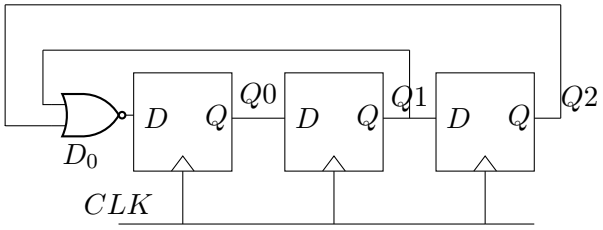
Figure 5.1:

3. Realize the decade counter in Fig. 5.2.

5.3. Problems

1. The maximum clock frequency in MHz of a 4-stage ripple counter, utilizing flip-flops, with each flip-flop having a propagation delay of 20 ns, is _____. (round off to one decimal place) (GATE EE 2022)

2. The digital circuit shown _____



   (A) is a divide-by-5 counter

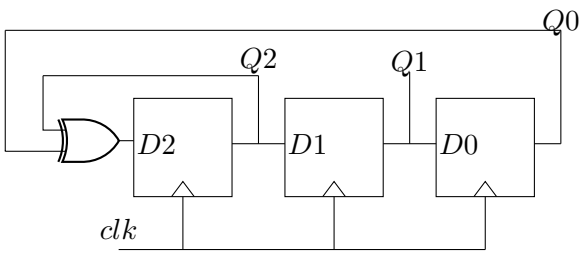
   (B) is a divide-by-7 counter

   (C) is a divide-by-8 counter

   (D) does not function as a counter due to disjoint cycles of states

   GATE IN 2022

3. The propogation delay of the exclusive-OR(XOR) gate in the circuit in the figure is 3ns.The propogation delay of all the flip-flops is assumed to be zero.The clock(Clk) frequency provided to the circuit is 500MHz. (GATE EC 2021)



Starting from the initial value of the flip-flop outputs $Q2Q1Q0 = 111$ with $D2 = 1$,the minimum number of triggering clock edges after which the flip-flop outputs $Q2Q1Q0$ becomes 1 0 0*(in integer)* is __

4. For the 3-bit binary counter shown in the figure, the output increments at every positive transition in the clock (CLK). Assume ideal diodes and the starting state of the counter as 000. If output high is $1V$ and output low is $0V$, the current I(in mA) flowing through the 50Ω resistor during the 5th clock cycle is (up to one decimal place) (GATE IN 2018)

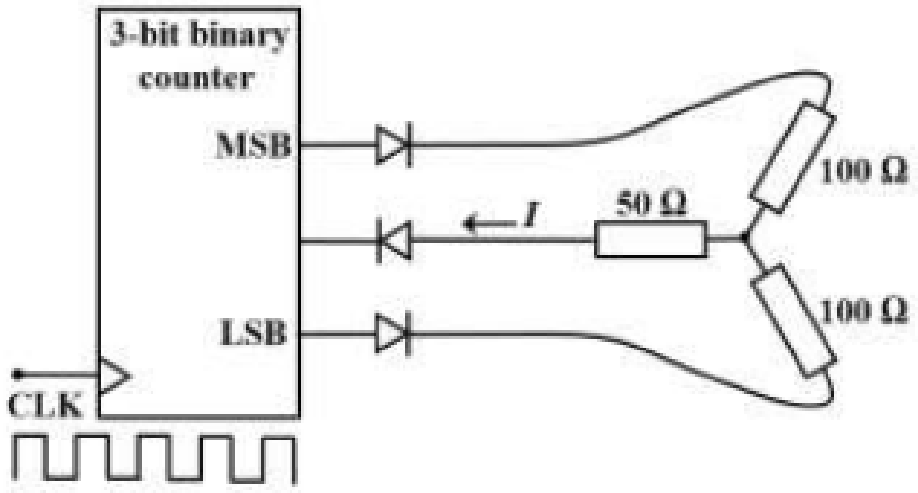


Figure 5.3: circuit

5. Consider the sequential circuit shown in the figure, where both flip-flops used are positive edge-triggered D flip-flops.

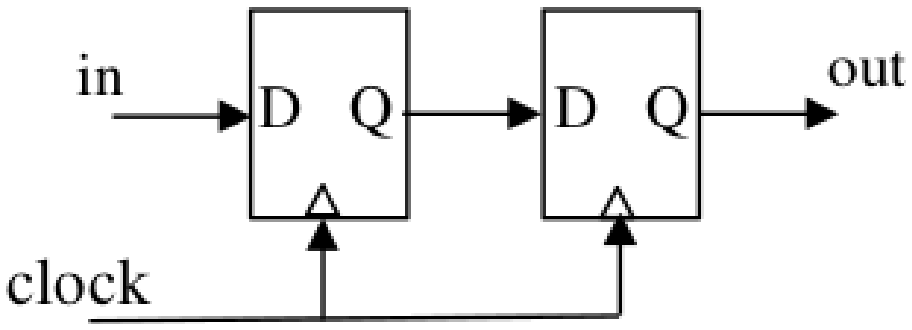
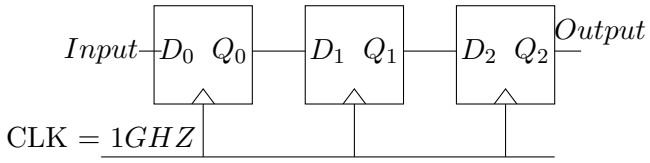


Figure 5.4: ckt

6. The number of states in the state transition diagram of this circuit that have a transition back to the same state on some value of "in" is _____. (GATE IN 2018)

7. The synchronous sequential circuit shown below works at a clock frequency of $1GHz$. The throughput, in $Mbits/s$,and the latency, in ns, respectively, are



   (a) $1000, 3$

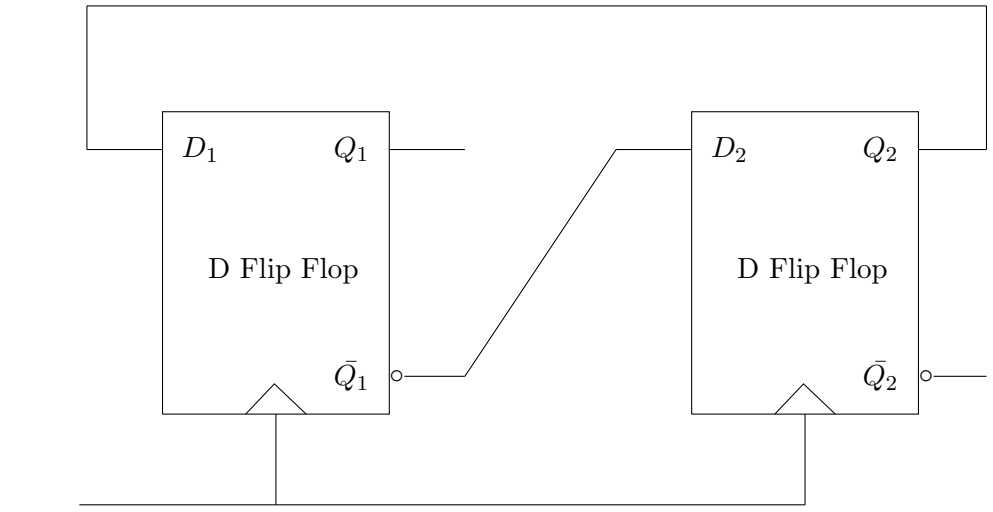
   (b) $333.33, 1$

   (c) $2000, 3$

   (d) $333.33, 3$

(GATE EC 2023)

8. In a given sequential circuit, initial states are $Q1 = 1$ and $Q2 = 0$. For a clock frequency of $1MHz$, the frequency of signal $Q2$ in kHz, is(rounded off to the nearest integer)



CLK =1Mhz

(GATE EC 2023)

9. Neglecting the delays due to the logic gates in the circuit shown in figure, the decimal equivalent of the binary sequence $[ABCD]$ of initial logic states, which will not change with clock, is _____.

(EE GATE 2023)

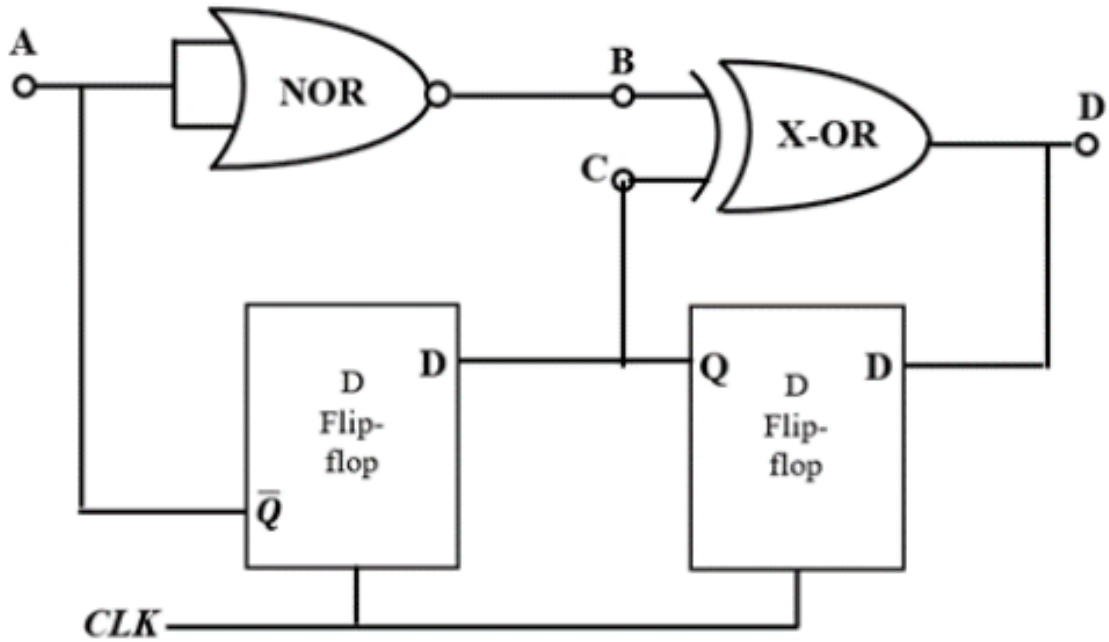


Figure 5.5: Neglecting the delays

10. Consider a sequential digital circuit consisting of T flip-flops and D flip-flops as shown in the figure. CLKIN is is the clock input to the circuit. At the beginning,Q1,Q2 and Q3 have values 0,1 and 1, respectively. (GATE CS2023,43)

    Which of the given values of(Q1,Q2,Q3) can NEVER be obtained with this digital circuit?

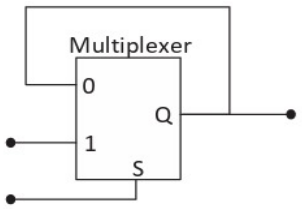
    (a) $(0, 0, 1)$

    (b) $(1, 0, 0)$

    (c) $(1, 0, 1)$

    (d) $(1, 1, 1)$

11. The output of a 2-input multiplexer is connected back to one of its inputs as shown in the figure.



Match the functional equivalence of this circuit to one of the following option.

(A) $DFlip - Flop$

(B) $DLatch$

(C) $Half - adder$

(D) $Demultiplexer$

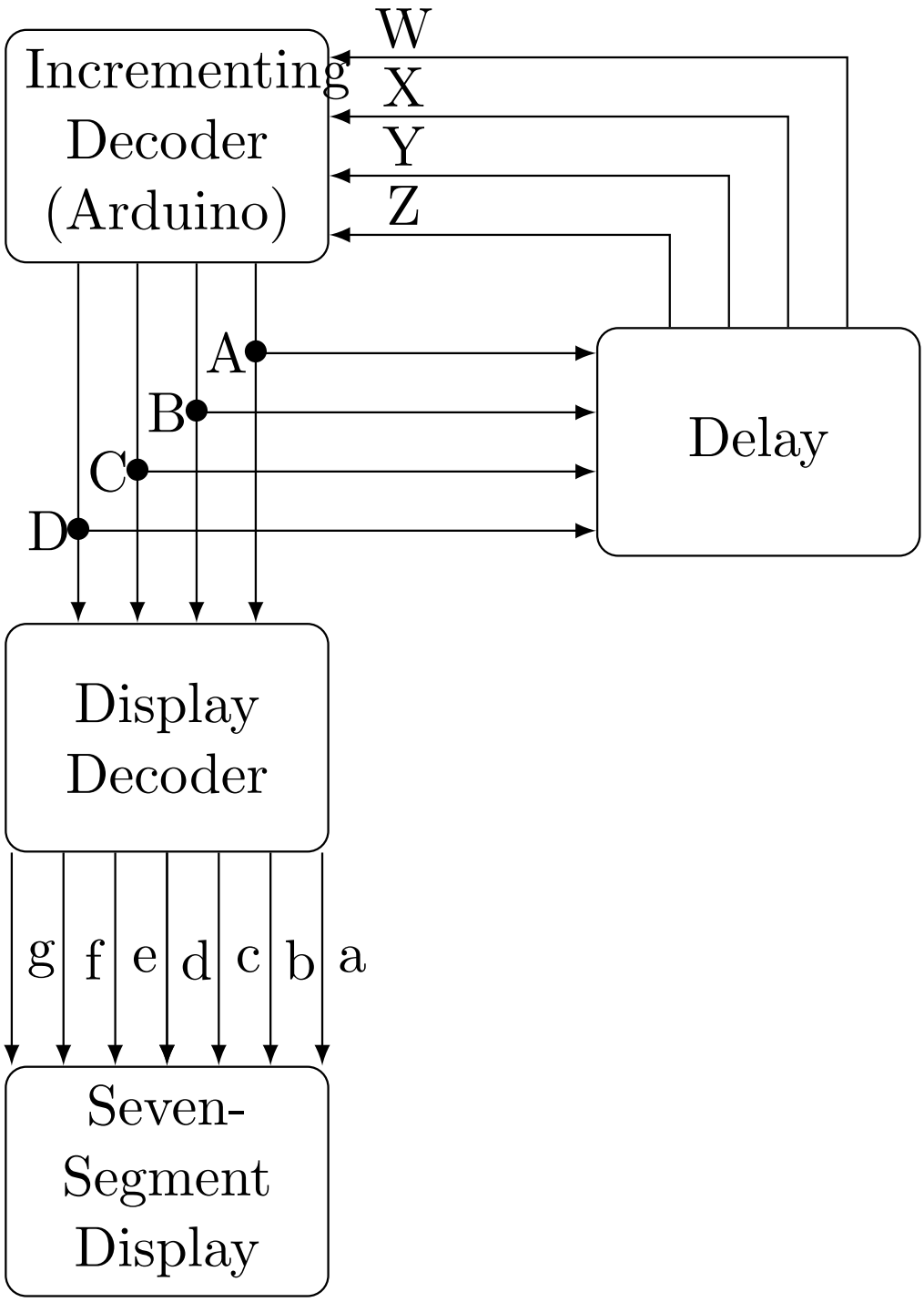
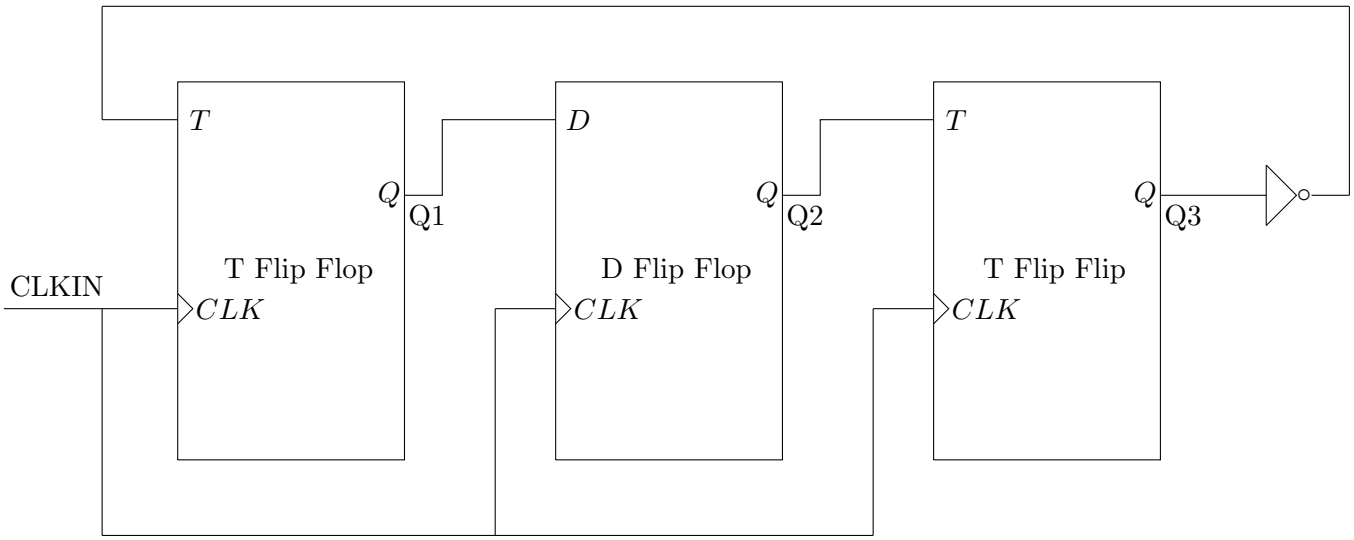

Incrementing
Decoder
(Arduino)
W
X
Y
Z
A
B
C
D
Delay
Display
Decoder
g
f
e
d
c
b
a
Seven-
Segment
Display

Figure 5.2:


T
Q
Q1
T Flip Flop
CLKIN
CLK
D
Q
Q2
D Flip Flop
CLK
T
Q
Q3
T Flip Flip
CLK