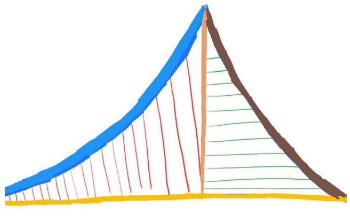
SIGNAL PROCESSING
Through GATE

G. V. V. Sharma



Contents

Introduction iii

1 Harmonics 1

2 Filters 3

3 Z-transform 5

4 Systems 7

5 Sequences 13

6 Sampling 15

7 Contour Integration 19

8 Laplace Transform 21

Introduction

This book provides solutions to signal processing problems in GATE.

Chapter 1

Harmonics

Chapter 2

Filters

Chapter 3

Z-transform

Chapter 4

Systems

4.1 Consider a unity-gain negative feedback system consisting of the plant $G(s)$ and a proportional-integral controller. Let the proportional gain and integral gain be 3 and 1, respectively. For a unit step reference input, the final values of the controller output and the plant output, respectively, are

$$G(s) = \frac{1}{(s-1)}$$

Solution:

Parameter	**Description**	**Value**
K_p	Proportional Gain	3
K_i	Integral Gain	1
$r(t)$	Reference Input	$u(t)$
$w(t)$	Controller Output	?
$y(t)$	Plant Output	?
$e(t)$	Error Input	$r(t) - y(t)$

Table 1: Parameter Table

From theFig. 4.1:

$$E(s) = U(s) - Y(s) \tag{4.1}$$

$$W(s) = 3E(s) + \frac{1}{s}E(s) \tag{4.2}$$

$$Y(s) = G(s)W(s) \tag{4.3}$$

Some results:

$$tx(t) \overset{\mathcal{L}}{\longleftrightarrow} -\frac{dX(s)}{ds} \tag{4.4}$$

$$e^{-at}x(t) \overset{\mathcal{L}}{\longleftrightarrow} X(s+a) \tag{4.5}$$

By using (4.4) and (4.5):

$$e^{-t}u(t) \overset{\mathcal{L}}{\longleftrightarrow} \frac{1}{s+1}, Re(s) > -1 \tag{4.6}$$

$$te^{-t}u(t) \overset{\mathcal{L}}{\longleftrightarrow} \frac{1}{(s+1)^2}, Re(s) > -1 \tag{4.7}$$

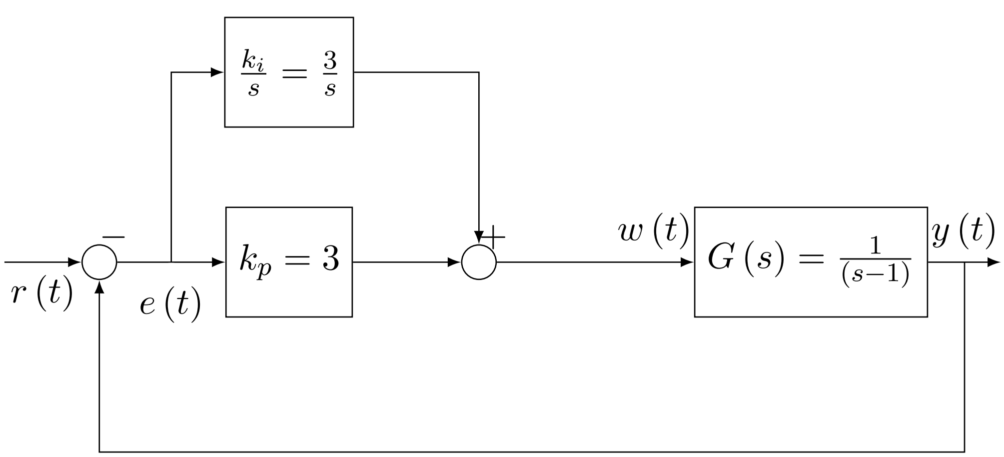


Figure 4.1: Block Diagram of System

(a) **Plant Output:**

From (4.1) , (4.2) and (4.3):

$$Y\left(s\right)=\frac{3s+1}{s\left(s+1\right)^{2}},Re\left(s\right)>-1 \tag{4.8}$$

Final Value Theorem:

$$\lim_{t\to\infty}x\left(t\right)=\lim_{s\to0}sX\left(s\right) \tag{4.9}$$

Using (4.9) on Y(s):

$$\begin{aligned}\lim_{t\to\infty}y\left(t\right)&=\lim_{s\to0}sY\left(s\right) &(4.10)\\ &=1 &(4.11)\end{aligned}$$

Taking partial fraction of (4.8) :

$$Y\left(s\right)=\frac{1}{s}+\frac{2}{\left(s+1\right)^{2}}-\frac{1}{s+1} \tag{4.12}$$

Using (4.6) and (4.7):

$$\therefore y\left(t\right)=u\left(t\right)+2te^{-t}u\left(t\right)-e^{-t}u\left(t\right) \tag{4.13}$$

(b) **Controller Output:**

From (4.2)

$$W\left(s\right)=\frac{3}{s}+\frac{1}{s^{2}}-Y\left(s\right)\left(3+\frac{1}{s}\right) \tag{4.14}$$

Substituting (4.8)

$$W\left(s\right)=\frac{\left(s-1\right)\left(3s+1\right)}{s\left(s+1\right)^{2}}, Re\left(s\right)>-1 \tag{4.15}$$

Using (4.9) on W(s)

$$\lim_{t\to\infty} w\left(t\right)=\lim_{s\to 0} sW\left(s\right) \tag{4.16}$$

$$=-1 \tag{4.17}$$

Taking partial fraction of equation(4.15) :

$$W\left(s\right)=-\frac{1}{s}-\frac{4}{\left(s+1\right)^{2}}+\frac{4}{s+1} \tag{4.18}$$

Using equations (4.6) and (4.7) and taking inverse lapalace transform:

$$w\left(t\right)=-u\left(t\right)-4te^{-t}u\left(t\right)+4e^{-t}u\left(t\right) \tag{4.19}$$

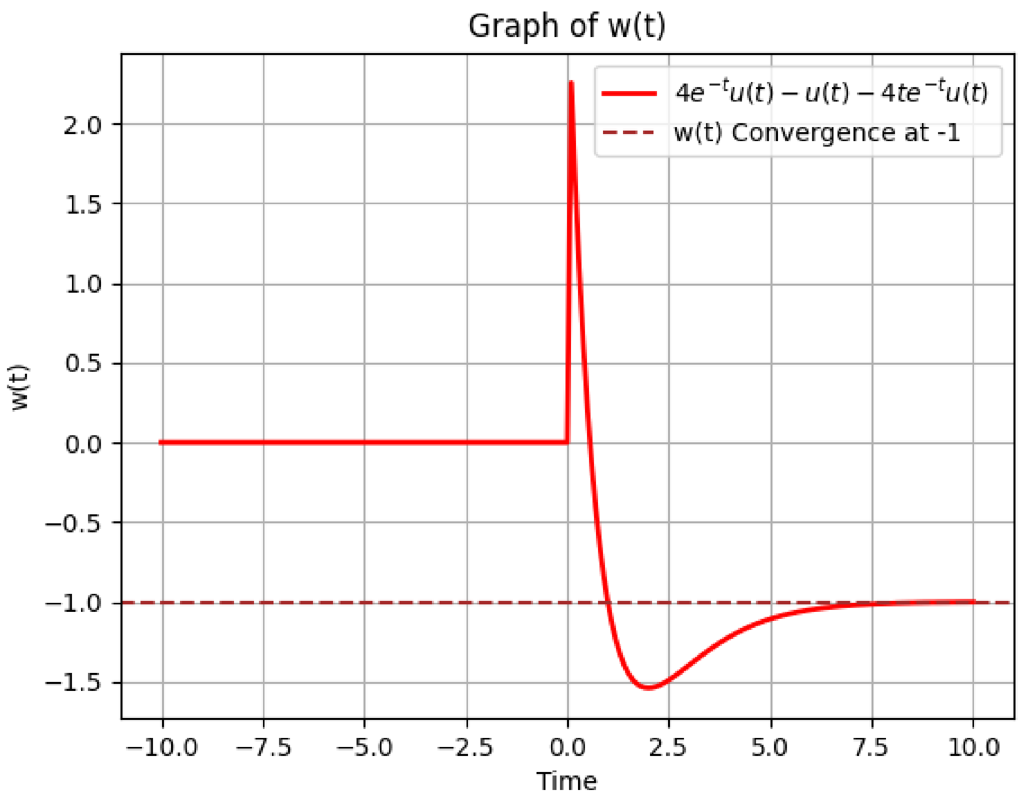


Figure 4.2: $w(t)$ converges at -1.

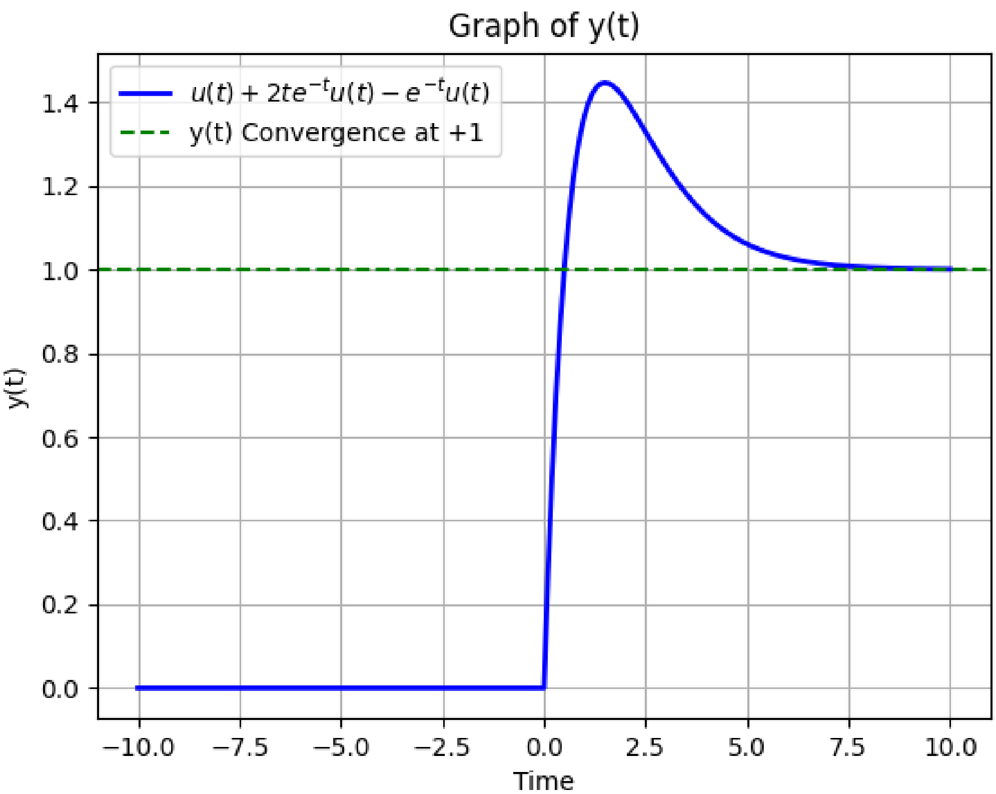


Figure 4.3: $y\left(t\right)$ converges at $+1$

Chapter 5

Sequences

5.1 Consider the discrete time signal $x[n] = u[-n+5] - u[n+3]$, where

$$u[n] = \begin{cases} 1; n \geq 0 \\ 0; n < 0 \end{cases}$$

The smallest n for which $x[n] = 0$ is?

Solution: From Fig. 1, the minimum value of n is given as

$$n = -3 \tag{5.1}$$

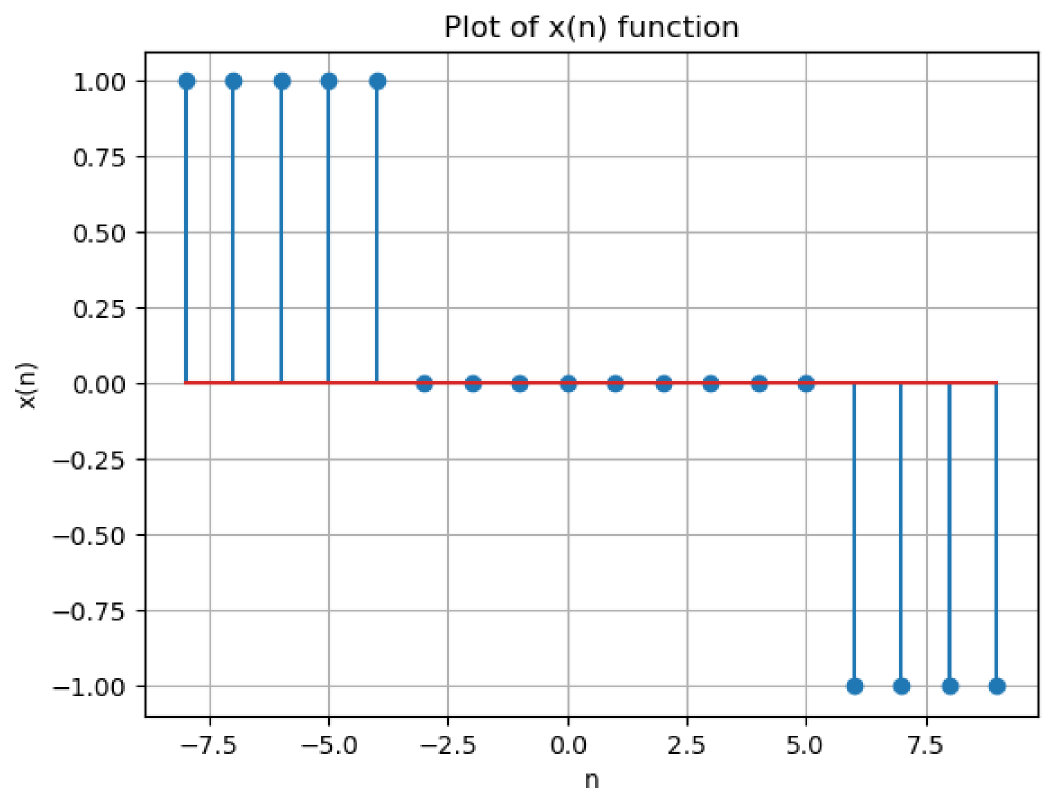


Figure 1: Plot of function $x\left(n\right)$ taken from python3

Chapter 6

Sampling

6.1 An 8 bit ADC converts analog voltage in the range of 0 to $+5\,V$ to the corresponding digital code as per the conversion characteristics shown in figure. For $V_{in} = 1.9922\,V$, which of the following digital output, given in hex, is true?

(a) $64H$

(b) $65H$

(c) $66H$

(d) $67H$

GATE EE 40

Solution:

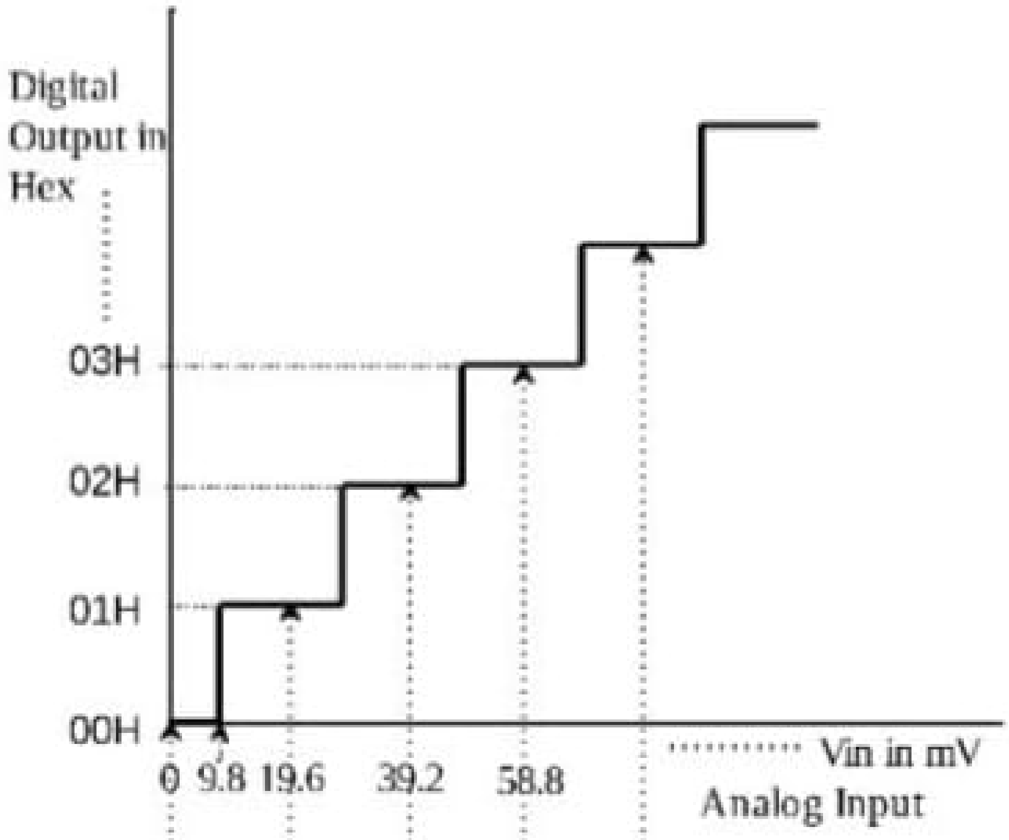


Figure 6.1:

Calculating the step-size:

$$\Delta V_{in} = \frac{V_{max} - V_{min}}{2^n - 1} \tag{6.1}$$

$$= \frac{5 - 0}{2^8 - 1} \tag{6.2}$$

$$= \frac{5}{255} \tag{6.3}$$

$$\implies V_{out} = \frac{V_{in}}{\Delta V_{in}} \tag{6.4}$$

$$= \frac{1.9922 \times 255}{5} \tag{6.5}$$

$$= 101.59 \tag{6.6}$$

$$\approx 102_{10} \tag{6.7}$$

Symbol	Value	Description
n	8	Number of bits of ADC
V_{min}	$0V$	Minimum Analog Voltage
V_{max}	$5V$	Maximum Analog Voltage
V_{in}	$1.9922V$	Input Voltage
V_{out}		Output Voltage

Table 6.1: Given Parameters

$\therefore$ correct answer is option (c).

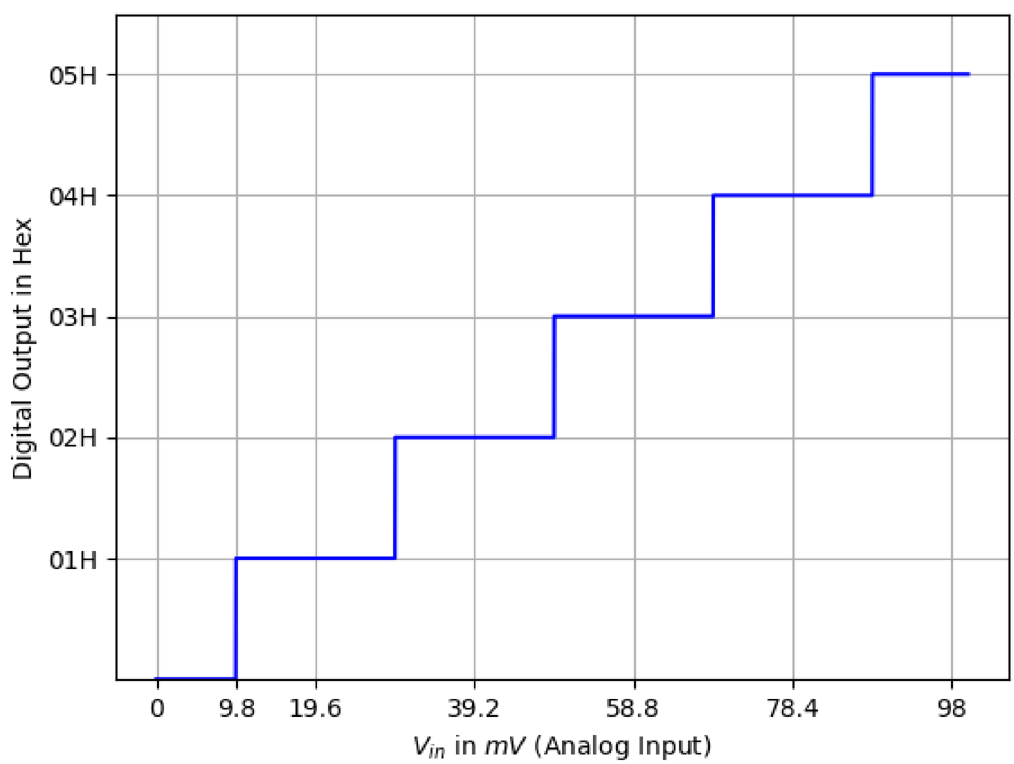

05H
04H
03H
02H
01H
Digital Output in Hex
0
9.8
19.6
39.2
58.8
78.4
98
V_{in} in mV (Analog Input)

Figure 6.2:

Chapter 7

Contour Integration

Chapter 8

Laplace Transform

8.1 The number of zeroes of the polynomial $P(s) = s^3 + 2s^2 + 5s + 80$ in the right side of the plane? (GATE IN 2023)

Solution: The table below shows the Routh array of the n^{th}- order characteristic polynomial :

$$a_0 s^n + a_1 s^{n-1} ...... + a_{n-1} s^1 + a_n s^0 \tag{8.1}$$

s^n	a_0	a_2	a_4	...
s^{n-1}	a_1	a_3	a_5	...
s^{n-2}	$b_1 = \frac{a_1 a_2 - a_3 a_0}{a_1}$	$b_2 = \frac{a_1 a_4 - a_5 a_0}{a_1}$	...	..
s^{n-3}	$c_1 = \frac{b_1 a_3 - b_2 a_1}{b_1}$	$\vdots$		
$\vdots$	$\vdots$	$\vdots$		
s^1	$\vdots$	$\vdots$		
s^0	a_n			

Table 8.1: Routh Array

Characteristic Equation:

$$s^3 + 2s^2 + 5s + 80 = 0 \tag{8.2}$$

From Table 8.1:

s^3	1	5
s^2	2	80
s^1	$\frac{2 \times 5 - 80 \times 1}{2} = -35$	
s^0	$\frac{-35 \times 80}{-35} = 80$	

Table 8.2:

From Table 8.2:

Since there are 2 sign changes in the first column of the Routh tabulation. So, the number of zeros in the right half of the s-plane will be 2.

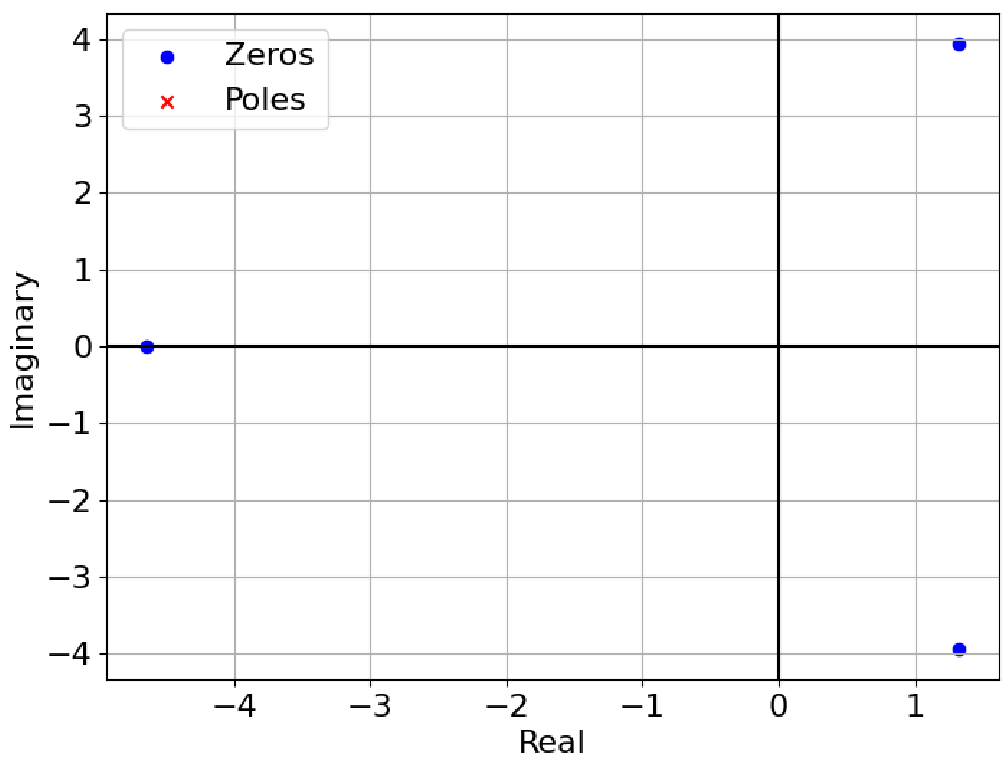


Figure 8.1:

8.2 The circuit shown in the figure is initially in the steady state with the switch K in open condition and $\overline{K}$ in closed condition. The switch K is closed and $\overline{K}$ is opened simultaneously at the instant $t = t_1$, where $t_1 > 0$. The minimum value of t_1 in milliseconds such that there is no transient in the voltage across the 100 μF capacitor, is ______ (Round off to 2 decimal places) (GATE EE 2023)