```
//status: OPERATIONAL
module TimeCounter(
    input clk,
    input CE,
    input Qsec,
    input Reset,
    output Signal
    );
    wire [3:0]Q;
    wire utc;
    wire active = CE & Qsec;
    countUD4L counter1 (.Up(active),
.Dw(1'b0), .LD(Reset | Signal),
.Q(4'b0),
                        .UTC(utc),
.clk(clk), .Qout(Q[3:0]));


    assign Signal = Q[1];
```

```
endmodule
```