```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:


module Top_Module_Main(
    input [7:0] sw,
    input btnL,
    input btnC,
    input btnR,
    input clkin,
    output [6:0] seg,
    output dp,
    output [3:0] an
    );
    wire [1:0] button;
    wire [7:0] sum_output;
    wire [6:0] left_disp, right_disp;
    assign button[0] = btnL, button[1] =
btnC, an[3] = 1, an[2] = 1, dp = 1;

    //Incrementer(a [7:0], [1:0] b, [7:0]
```

```
s)
    Incrementer inc (.a(sw), .b(button),
.s(sum_output));    //sum_output bus 4 to
hex7seg1 and hex7seg2

    hex7seg sgmt_cnvtr1
(.n(sum_output[3:0]), .seg(left_disp));
//left display
    hex7seg sgmt_cnvtr2
(.n(sum_output[7:4]), .seg(right_disp));
//right display

    wire dig_sel;
    lab3_digsel lab3_digselect
(.clkin(clkin), .greset(btnR),
.digsel(dig_sel));
    assign an[0] = dig_sel, an[1] =
!dig_sel;
    //m2_1x8(.in0 [7:0], .in1 [7:0], .sel,
out [7:0])
    m2_1x8 mux8_1(.in0(right_disp),
.in1(left_disp), .sel(dig_sel),
.out(seg));    //seg is the output of the
display
```

```
endmodule
```