```
//status: IN PROGRESS
module Time_Counter(
    input CE,
    input R,
    input run,
    input clk,
    output [7:0] Q
    );
    wire UTC; wire [7:0] hold;

    countUD4L counter1 (.Up(CE&run),
.Dw(R), .LD(1'b0), .clk(clk),
.UTC(UTC), .Qout(hold[3:0]));

    wire start_cnt;
    assign start_cnt = UTC & CE & run;
    countUD4L counter2
(.Up(start_cnt), .LD(1'b0), .Dw(R),
.clk(clk), .Qout(hold[7:4]));
   // assign Q = hold;
   assign Q[7] = hold[4], Q[6] =
```

```
hold[5], Q[5] = 1'b0, Q[4] = 1'b0,
Q[3] = hold[0], Q[2] = hold[1], Q[1]
= hold[2], Q[0] = hold[3];
endmodule
```