```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:


module m8_1(    //m8_1(in [7:0], [2:0] sel, [7:0] out)
    input [7:0] in,
    input [2:0] sel,
    output out
    );
    assign out = (!sel[0] & !sel[1] & !sel[2]) ? !in[0] :     //000
                 (!sel[0] & !sel[1] & sel[2]) ? !in[1] :     //001
                 (!sel[0] &  sel[1] & !sel[2]) ? !in[2] :     //010
                 (!sel[0] &  sel[1] & sel[2]) ? !in[3] :     //011
                 (sel[0]  & !sel[1] & !sel[2]) ? !in[4] :     //100
                 (sel[0]  & !sel[1] &
```

```
sel[2]) ? !in[5] :      //101
                (sel[0]  &  sel[1] &
!sel[2]) ? !in[6] :      //110
                !in[7]
             ;      //111
endmodule
```