```verilog
module VSync_Tracker(
    input clk,
    input NextCol,
    output Frame,
    output [11:0] Position
    );
    wire Reset;
    wire utc1, utc2, utc3;
    wire [11:0]out;
    countUD4L tracker1 (.Up(!clk&NextCol),               .Dw(1'b0), .LD(1'b0),
.Reset(Reset), .Q(4'b0), .clk(clk), .UTC(utc1), .Qout(out[3:0] ));
    countUD4L tracker2 (.Up(!clk&NextCol&utc1),          .Dw(1'b0), .LD(1'b0),
.Reset(Reset), .Q(4'b0), .clk(clk), .UTC(utc2), .Qout(out[7:4] ));
    countUD4L tracker3 (.Up(!clk&NextCol&utc1&utc2), .Dw(1'b0), .LD(1'b0),
.Reset(Reset), .Q(4'b0), .clk(clk), .UTC(utc3), .Qout(out[11:8]));

    assign Reset = out > 524 ? 1'b1 : 1'b0;
    Edge_Detector end_frame (.clk(clk), .btn(Reset), .out(Frame));  //end of a full
frame when HIGH
    assign Position = out;


endmodule
```