```verilog
//status: COMPLETE
module TurkeyCounter(
    input Add,
    input Subtract,
    input clk,
    output Negative,
    output [7:0]Turkeys
);
    wire utc, utc2, dtc, dtc2, zero, MAX;
    wire [11:0] out;
    wire increment, decrement, negative;
    assign increment = (Add & !negative & !MAX) |
(Subtract &  (negative | zero) & !MAX);
    assign decrement = (Add &  negative)        |
(Subtract & !negative & !zero);
    assign MAX = out[0] & out[1] & out[2] & out[3] &
out[7] & out[6];
    countUD4L counter  (.Up(increment),
.Dw(decrement),      .LD(1'b0), .Q(4'b0),
                        .clk(clk), .UTC(utc),
.DTC(dtc), .Qout(out[3:0]));
    countUD4L counter2 (.Up(increment&utc),
.Dw(decrement&dtc), .LD(1'b0), .Q(4'b0),
                        .clk(clk), .DTC(dtc2),
.Qout(out[7:4]));

    assign zero = dtc&dtc2;
    FDRE #(.INIT(1'b0)) neg (.C(clk), .R(1'b0),
.CE(zero), .D(Subtract), .Q(negative)); //adds a
negative sign
    assign Negative = negative;
```

```verilog
    assign Turkeys[4] = 1'b0;
    assign Turkeys[3:0] = out[3:0];
    assign Turkeys[7:5] = out[7:5];


endmodule
```