```
//status: OPERATIONAL
module RingCounter(
    input digsel,
    input clk,
    output [3:0]Q
    );
    //wire start;
    FDRE #(.INIT(1'b1)) ff1 (.C(clk), .R(1'b0), .CE(digsel), .D(Q[0]), .Q(Q[3]));
    FDRE #(.INIT(1'b0)) ff2 (.C(clk), .R(1'b0), .CE(digsel), .D(Q[3]), .Q(Q[2]));
    FDRE #(.INIT(1'b0)) ff3 (.C(clk), .R(1'b0), .CE(digsel), .D(Q[2]), .Q(Q[1]));
    FDRE #(.INIT(1'b0)) ff4 (.C(clk), .R(1'b0), .CE(digsel), .D(Q[1]), .Q(Q[0]));
endmodule
```