```
module HSync_Tracker(
    input clk,
    output RowFinish,
    output [11:0] Position
    );
    wire Reset;
    wire utc1, utc2, utc3;
    wire [11:0]out;
   //the !clk simulated the negative clock edge
    countUD4L tracker1 (.Up(!clk),           .Dw(1'b0), .LD(1'b0), .Reset(Reset),
.Q(4'b0), .clk(clk), .UTC(utc1), .Qout(out[3:0] ));
    countUD4L tracker2 (.Up(!clk&utc1),      .Dw(1'b0), .LD(1'b0), .Reset(Reset),
.Q(4'b0), .clk(clk), .UTC(utc2), .Qout(out[7:4] ));
    countUD4L tracker3 (.Up(!clk&utc1&utc2), .Dw(1'b0), .LD(1'b0), .Reset(Reset),
.Q(4'b0), .clk(clk), .UTC(utc3), .Qout(out[11:8]));

    assign Reset = out > 798 ? 1'b1 : 1'b0;
    assign RowFinish = out >= 798;
    assign Position = out;

endmodule
```