```
module Blink(
    input InputSignal,
    input Framerate,
    input clk,
    output OutputSignal
    );
wire [7:0]timer;
wire utc,blink, utc2;
wire TIME_UP = timer == 64;
countUD4L blink1 (.Up(InputSignal),     .Dw(1'b0), .LD(1'b0), .Reset(TIME_UP),
.UTC(utc),  .Q(4'b0), .clk(Framerate), .Qout(timer[3:0]));
countUD4L blink2 (.Up(InputSignal&utc), .Dw(1'b0), .LD(1'b0), .Reset(TIME_UP),
.UTC(utc2), .Q(4'b0), .clk(Framerate), .Qout(timer[7:4]));

wire XOR_OUT = InputSignal & (TIME_UP ^ blink);
FDRE #(.INIT(1'b0) ) ffB2 (.C(Framerate), .R(1'b0), .CE(1'b1), .D(XOR_OUT), .Q(blink)

assign OutputSignal = blink;
endmodule
```