```
//status: COMPLETE
module Selector(
  input [3:0] sel,
  input [15:0] N,
 output [3:0] H
  );
 assign H = (sel[3] \& !sel[2] \&
!sel[1] & !sel[0]) ? N[15:12]:
//3
             (!sel[3] & sel[2] &
!sel[1] & !sel[0]) ? N[11:8] :
//2
             (!sel[3] & !sel[2] &
sel[1] & !sel[0]) ? N[7:4] :
//1
             (!sel[3] & !sel[2] &
!sel[1] & sel[0]) ? N[3:0] : 0;
//0
 assign NegDisp = (!sel[3] \& sel[2]
& !sel[1] & !sel[0]);
```

