```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:


module Full_Adder(  //Full_Adder(cin, [1:0] selct, s, cout)
    input cin,
    input [1:0] select, //select[0] = b, select[1] = cin
    output s,
    output cout
    );
    wire [3:0] a0, a1;
    wire w0;
    assign a0[0] = cin, a0[1] = !cin, a0[2] = !cin, a0[3] = cin;
    assign a1[0] = 0, a1[1] = cin, a1[2] = cin, a1[3] = 1;
    //m4_1(.in[3:0], .sel[1:0], .out)
    m4_1 mltplx1(.in(a0), .sel(select), .out(s));
```

```
    m4_1 mltplx2 (.in(a1), .sel(select),
.out(cout));

endmodule
```