```
//status: COMPLETE
module countUD16L(
    input clk,
    input Up,
    input Dw,
    input LD,   //iff pressed, load the switch value
    input [15:0] Din,
    output UTC, output DTC, output [15:0] Q
    );
    wire [3:0] utc,  dtc;
    wire m1, m2, m3, d1, d2, d3;
    countUD4L count4bit1 (.Up(Up), .Dw(Dw), .LD(LD), .Q(Din[3:0]), .clk(clk),   //cnt
        .UTC(utc[0]), .DTC(dtc[0]), .Qout(Q[3:0]));
    assign m1 = Up & utc[0];
    assign d1 = Dw & dtc[0];

    countUD4L count4bit2 (.Up(m1), .Dw(d1), .LD(LD), .Q(Din[7:4]), .clk(clk),   //cnt
        .UTC(utc[1]), .DTC(dtc[1]), .Qout(Q[7:4]));
    assign m2 = Up & utc[0] & utc[1];
    assign d2 = Dw & dtc[0] & dtc[1];

    countUD4L count4bit3 (.Up(m2), .Dw(d2), .LD(LD), .Q(Din[11:8]), .clk(clk),  //cnt
        .UTC(utc[2]), .DTC(dtc[2]), .Qout(Q[11:8]));
    assign m3 = Up & utc[0] & utc[1] & utc[2];
    assign d3 = Dw & dtc[0] & dtc[1] & dtc[2];

    countUD4L count4bit4 (.Up(m3), .Dw(d3), .LD(LD), .Q(Din[15:12]), .clk(clk), //cnt
        .UTC(utc[3]), .DTC(dtc[3]), .Qout(Q[15:12]));

    assign UTC = utc[0]&utc[1]&utc[2]&utc[3] ? 1 : 0;
    assign DTC = dtc[0]&dtc[1]&dtc[2]&dtc[3] ? 1 : 0;

endmodule
```