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`timescale 1ns / 1ps

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// Company:
// Engineer:
//coming in is a 4 bit number to display
as a hex value
module hex7seg(//hex7seg(n [3:0]. seg
[7:0])
    input [3:0] n,
    output [6:0] seg //seg[0] = a, seg[1]
= b...etc
    );
    //m8_1(in [7:0], [2:0] sel, [7:0] out)
    wire [7:0] inputs0, inputs1, inputs2,
inputs3, inputs4, inputs5, inputs6;
    wire [2:0] selectors;
    assign selectors[0] = n[0],
selectors[1] = n[1], selectors[2] = n[2];
    wire W; assign W = n[3];

    assign inputs0[0] = 1, inputs0[1] = 1,
inputs0[2] = !W, inputs0[3] = W,
inputs0[4] = 1, inputs0[5] = !W,

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inputs0[6] = W, inputs0[7] = 0;    //my: B,
vid: A

    m8_1 mux0 (.in(inputs0),
.sel(selectors), .out(seg[1]));

    assign inputs1[0] = 1, inputs1[1] = W,
inputs1[2] = 1, inputs1[3] = 1, inputs1[4]
= 1, inputs1[5] = 1, inputs1[6] = W,
inputs1[7] = 0;    //my C, vid: B

    m8_1 mux1 (.in(inputs1),
.sel(selectors), .out(seg[2]));

    assign inputs2[0] = !W, inputs2[1] =
1, inputs2[2] = W, inputs2[3] = !W,
inputs2[4] = 1, inputs2[5] = W, inputs2[6]
= 1, inputs2[7] = !W;    //my D, Vid: C

    m8_1 mux2 (.in(inputs2),
.sel(selectors), .out(seg[3]));

    assign inputs3[0] = !W, inputs3[1] =
!W, inputs3[2] = 0, inputs3[3] = !W,
inputs3[4] = !W, inputs3[5] = 1,
inputs3[6] = 1, inputs3[7] = 1;    //my E,
vid: D

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        m8_1 mux3 (.in(inputs3),
.sel(selectors), .out(seg[4]));

        assign inputs4[0] = !W, inputs4[1] =
0, inputs4[2] = 1, inputs4[3] = !W,
inputs4[4] = 1, inputs4[5] = 1, inputs4[6]
= !W, inputs4[7] = 1;    //my F, vid: E
        m8_1 mux4 (.in(inputs4),
.sel(selectors), .out(seg[5]));

        assign inputs5[0] = !W, inputs5[1] = 1,
inputs5[2] = W, inputs5[3] = 1, inputs5[4]
= 1, inputs5[5] = !W, inputs5[6] = !W,
inputs5[7] = 1;    //my A, vid: F
        m8_1 mux5 (.in(inputs5),
.sel(selectors), .out(seg[0]));

        assign inputs6[0] = 0, inputs6[1] = 1,
inputs6[2] = 1, inputs6[3] = !W,
inputs6[4] = 1, inputs6[5] = 1, inputs6[6]
= W, inputs6[7] = 1;    //my G, vid: G
        m8_1 mux6 (.in(inputs6),
.sel(selectors), .out(seg[6]));
endmodule

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