```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:

module Incrementer( //Incrementer(a [7:0], [1:0] b, [7:0] s)
    input [7:0] a,
    input [1:0] b,
    output [7:0] s
    );
    //Full_Adder(cin, [1:0] selct, s, cout)
    wire [7:0] b_convert;
    assign b_convert[7:2] = 6'b000000;
assign b_convert[0] = b[1]; assign
b_convert[1] = b[0]; //00000b[

    wire [7:0] w;
    wire [1:0] t0, t1, t2, t3, t4, t5, t6,
t7;

    assign t0[0] = b_convert[0], t0[1] = 0;
    Full_Adder fa1 (.cin(a[0]),
```

```
.select(t0), .s(s[7]), .cout(w[0]));

    assign t1[0] = b_convert[1], t1[1] =
w[0];
    Full_Adder fa2 (.cin(a[1]),
.select(t1), .s(s[6]), .cout(w[1]));

    assign t2[0] = b_convert[2], t2[1] =
w[1];
    Full_Adder fa3 (.cin(a[2]),
.select(t2), .s(s[5]), .cout(w[2]));

    assign t3[0] = b_convert[3], t3[1] =
w[2];
    Full_Adder fa4 (.cin(a[3]),
.select(t3), .s(s[4]), .cout(w[3]));

    assign t4[0] = b_convert[4], t4[1] =
w[3];
    Full_Adder fa5 (.cin(a[4]),
.select(t4), .s(s[3]), .cout(w[4]));

    assign t5[0] = b_convert[5], t5[1] =
w[4];
```

```
    Full_Adder fa6 (.cin(a[5]),
.select(t5), .s(s[2]), .cout(w[5]));

    assign t6[0] = b_convert[6], t6[1] =
w[5];
    Full_Adder fa7 (.cin(a[6]),
.select(t6), .s(s[1]), .cout(w[6]));

    assign t7[0] = b_convert[7], t7[1] =
w[6];
    Full_Adder fa8 (.cin(a[7]),
.select(t7), .s(s[0]), .cout(w[7]));
endmodule
```