```verilog
//status: SEEMING TO WORK
module Edge_Detector(
    input clk, input btn,
    output out
);
    wire feed, temp;
    FDRE #(.INIT(1'b0)) flip_flop1
(.C(clk), .R(1'b0), .CE(1'b1),
.D(btn), .Q(feed));
    assign temp = (btn & !feed);
//src1
    FDRE #(.INIT(1'b0)) flip_flop2
(.C(clk), .R(1'b0), .CE(1'b1),
.D(temp), .Q(out));
endmodule
```