```
module Top Module Main(
    input clkin,
    input btnR,
    input btnU,
    input btnC,
    output [15:0] led,
    output [3:0] an,
    output dp,
    output [6:0] seg
    );
   wire clk, digsel, qsec;
    wire [15:0] bit16out;
    lab5 clks sys clock
(.clkin(clkin), .greset(btnR),
.clk(clk), .digsel(digsel),
.qsec(qsec));
    wire four secs, two secs, match,
delay, delay 4sec;
    wire show num, reset timer,
```

```
run game, scored, flash both,
flash alt;
    wire edge C, edge U;
    Edge Detector bC (.clk(clk),
.btn(btnC), .out(edge_C));
    Edge Detector bU (.clk(clk),
.btn(btnU), .out(edge U));
    StateMachine state machine
(.Go(edge C), .Stop(edge U),
.FourSecs (four secs),
.TwoSecs(two secs), .Match(match),
.ShowNum(show num),
.ResetTimer(reset timer),
.RunGame (run game), .Scored (scored),
.Delay(delay),
.Sec4Delay(delay 4sec),
.FlashBoth (flash both),
.FlashAlt(flash alt), .clk(clk));
```

```
Two Second Delay two sec delay
(.clk(clk), .CE(delay),
.Reset(run game), .Qsec(qsec),
.Signal(two secs));
    Four Second Delay four sec delay
(.clk(clk), .CE(delay 4sec),
.Reset(run game), .Qsec(qsec),
.Signal(four secs));
   wire [7:0] CMPUTR, USER;
   wire [7:0] rand ints;
   LFSR rand num (.clk(clk),
.CE(!show num), .Q(rand ints));
  wire btnC ED;
  Edge Detector ED (.clk(clk),
.btn(btnC), .out(btnC ED));
  Game Counter game cnt (.CE(btnC ED
& !show num), .R(1'b0),
.in(rand ints), .clk(clk),
```

```
.Q(CMPUTR)); //from LFSR changed to
reset timer
   wire [7:0]equal;
   wire rstTimer;
   Edge Detector timerst (.clk(clk),
.btn(run game), .out(rstTimer));
    Time Counter time cnt (.CE (qsec),
.R(rstTimer), .run(run game),
.clk(clk), .Q(USER)); //added a RESET
    assign equal[7] = !(CMPUTR[7]^
USER[7]);
    assign equal[6] = !(CMPUTR[6])^
USER[6]);
   assign equal[5] = !(CMPUTR[5]^
USER[5]);
    assign equal[4] = !(CMPUTR[4])^
USER[4]);
   assign equal[3] = !(CMPUTR[3] ^
USER[3]);
    assign equal[2] = !(CMPUTR[2]^
```

```
USER[2]);
    assign equal[1] = !(CMPUTR[1] ^
USER[1]);
    assign equal[0] = !(CMPUTR[0] ^
USER[0]);
    assign match =
equal[0]&equal[1]&equal[2]&
equal[3] & equal[4] & equal[5]
                    &equal[6]&equal[7];
    assign bit16out[15:8] = CMPUTR;
    assign bit16out[7:0] = USER;
    wire [15:0] led shift;
    wire scored ED;
    Edge Detector score ED
(.clk(clk), .btn(scored),
.out(scored ED));
    LED Shifter led lights
```

```
(.In(1'b1), .CE(scored ED),
.clk(clk), .Q(led shift));
    //FLASH ALT
   wire alt1, alt2, both1, both2;
    FDRE # (.INIT(1'b1) ) ffA1
(.C(clk), .R(1'b0),
.CE(qsec&flash alt), .D(alt1),
.Q(alt2));
    FDRE # (.INIT(1'b0) ) ffA2
(.C(clk), .R(1'b0),
.CE(qsec&flash alt), .D(alt2),
.Q(alt1));
    //FLASH BOTH
    FDRE #(.INIT(1'b1)) ffB1
(.C(clk), .R(1'b0),
.CE(qsec&flash both), .D(both2),
.Q(both1));
    FDRE #(.INIT(1'b0)) ffB2
(.C(clk), .R(1'b0),
```

```
.CE(qsec&flash both), .D(both1),
.Q(both2));
    //below is from lab 4
   wire [3:0]Qring;
    RingCounter ring cntr
(.digsel(digsel), .clk(clk),
.Q(Qring));
    assign led = led shift;
    assign an[3] =
!(show num&(Qring[3] & !flash both &
!flash alt) | (Qring[3] &alt1 &
!flash both & flash alt) | (Qring[3]
&both1 & flash both & !flash alt));
    assign an[2] =
!(show num&(Qring[2] & !flash both &
!flash alt) | (Qring[2] &alt1 &
!flash both & flash alt) | (Qring[2]
&both1 & flash both & !flash alt));
    assign an [1] = !((Qring[1] \&
```

```
!flash both & !flash alt) | (Qring[1]
&alt2 & !flash both & flash alt) |
(Qring[1] &both1 & flash both &
!flash alt));
    assign an [0] = !((Qring[0] \&
!flash both & !flash alt) | (Qring[0]
&alt2 & !flash both & flash alt) |
(Qring[0] &both1 & flash both &
!flash alt));
    wire [3:0]sel;
    Selector select (.sel (Qring),
.N(bit16out), .H(sel));
    hex7seg segment disp (.n(sel),
.seg(seg));
endmodule
```