```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:



module m4_1( //m4_1(.in[3:0], .sel[1:0],
.out)
    input [3:0] in,
    input [1:0] sel,
    output out
    );
    assign out = (!sel[0] & !sel[1]) ?
in[0] :     //00
                 (!sel[0] &  sel[1]) ?
in[1] :     //01
                 (sel[0]  & !sel[1]) ?
in[2] :     //10
                 in[3]
  ;     //11
endmodule
```