All five RV32 Load Instructions

Encodes data size and "signedness" of load operation

		funct3		opcode	
imm[11:0]	rs1	000	rd	0000011	lb
imm[11:0]	rs1	001	rd	0000011	lh
imm[11:0]	rs1	010	rd	0000011	lw
imm[11:0]	rs1	100	rd	0000011	lbu
imm[11:0]	rs1	101	rd	0000011	lhu

A bits

- **`lb`: "load byte," `lh`: "load halfword" (16 bits)**
  - *Sign extend* to fill upper bits of destination 32-bit register.
- **`lbu`: "load unsigned byte," `lhu`: "load unsigned halfword"**
  - *Zero extend* to fill upper bits of destination 32-bit register.
- **Note no `lwu` instruction in RISC-V.**
  - Simplicity: No need to sign/zero extend when copying 32 bits into 32-bit register.