Design of 4:1 Multiplexer using CMOS Logic

Gaeya Sri Satya Vinnakota, BTech, Electronics Engineering, Sardar Vallabhbhai National Institute of Technology

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Abstract

This report describes the design and implementation of 4:1 Multiplexer using CMOS logic using the Cloud-based Synopsys tool at the 28nm CMOS technology node. Multiplexer circuit selects 1 output data line from multiple input data lines with the help of input select lines. This design discussed in the report uses 4 input data lines and 2 input select lines to get the 1 output data line.

1.Reference Circuit Details

A Multiplexer circuit, shortly called MUX, is used to select a data line as output from multiple input data lines by using input select lines. To get an output data line from N input data lines that is N:1 MUX, we require $\log_2^N$ select lines.

The representation of 4:1 MUX is shown in Figure-1, and the truth table of the 4:1 MUX is shown in Figure-2.

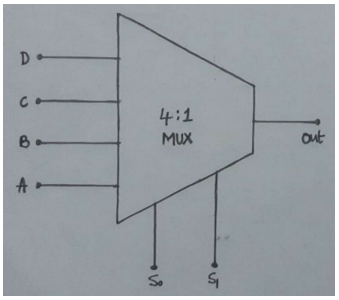

Figure 1 - Representation of 4:1 MUX

S_0	S_1	Out
0	0	A
1	0	B
0	1	C
1	1	D

Figure 2 - Truth Table of 4:1 MUX

In this report, a 4:1 MUX is designed using CMOS logic (Figure-3). Here both the Pull-up (made of the PMOS) and pull-down (made of the NMOS) networks pull the output to the input data lines, and the input select lines are given to the MOSFETs' gates.

2.Reference Circuit

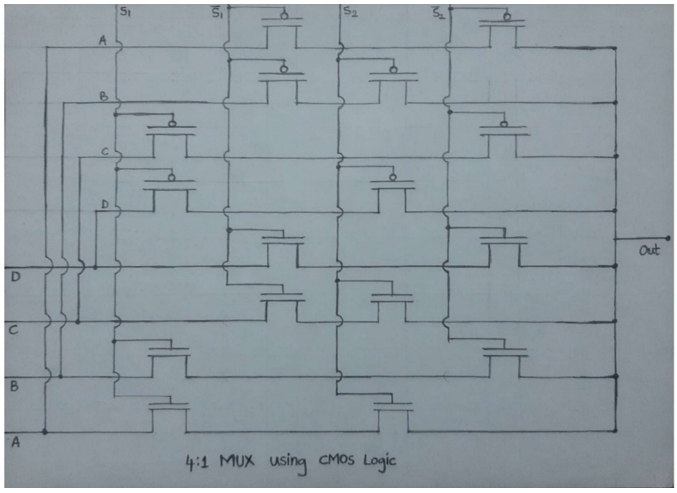

Figure 3 - Reference Circuit

3.Reference Waveforms

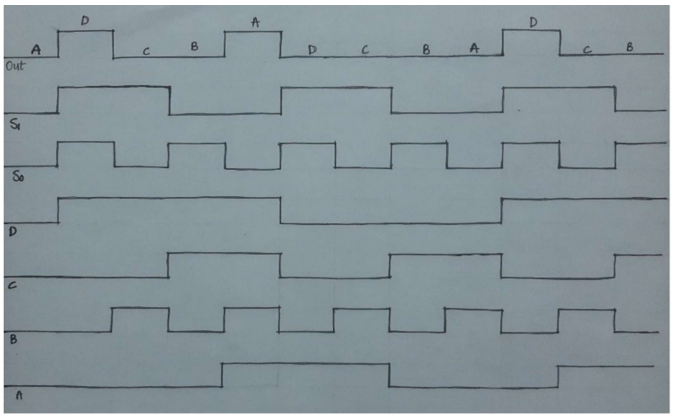

Figure 4 - Reference Waveforms

References

[1] https://en.wikipedia.org/wiki/Multiplexer

[2] https://www.electronics-tutorials.ws/combination/comb_2.html

[3] https://www.electronics-tutorial.net/Digital-CMOS-Design/Pass-Transistor-Logic/4-1-multiplexer-using-CMOS-logic/