# Design of 32bit ALU with Zero Flag

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### **Abstract**

This report describes the design and implementation of 32 bit Arithmetic and logical unit (ALU) with a zero flag. ALU block is a combinational digital circuit that performs arithmetic and bitwise operations on integer binary numbers.

## 1. REFERENCE CIRCUIT DETAILS

The 32-bit ALU has 2 inputs 'In1,In2' of 32 bits width each, these inputs to the ALU are the data to be operated on, called operands and 'ALUop' is the code that indicates the operation that have to be performed by the ALU, the width of the ALUop is determined the number of operations the ALU can perform. In this design the ALUop is considered to be of 4-bit wide. This ALU has a 32-bit output that is 'out' which is the result obtained after performing the operation described by ALUop.

Generally, ALU consists of status inputs and status outputs which are also called as flags, in this design there is one status output 'zero' from the ALU that is the Zero Flag. Zero flag will be set as one when the ALU output is zero. Block diagram of ALU with a zero flag is shown in Figure 1.

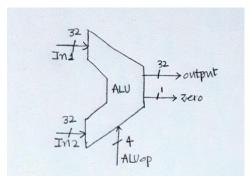


Figure 1 - Representation of 32-bit ALU with Zero Flag

This design is done by designing the ALU's computational unit using Verilog and the Zero flag using comparator in ngspice and integrating both of the using esim ngveri tool.

The block diagram of the circuit that is to be implemented in this hackathon is shown in Figure 2. Where computational unit is digital and comparator is analog thus resulting in a mixed signal circuit.

For example, Subtraction operation is considered and the sample waveform is shown in the Figure 3.

# 2. REFERENCE CIRCUIT

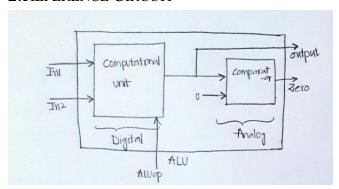


Figure 2 – Block diagram of circuit to be designed

## 3. REFERENCE WAVEFORMS

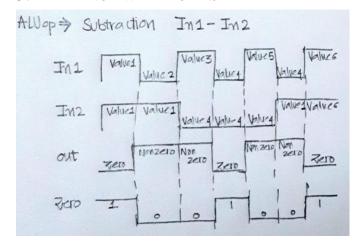


Figure 3 - Reference Waveforms for subtraction operation

### REFERENCES

- [1] https://en.wikipedia.org/wiki/Arithmetic\_logic\_unit
- [2] https://en.wikipedia.org/wiki/Zero\_flag