

# **CSE 331 HW 4**

## **REPORT**

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## Inner Modules of mini\_mips:

**mini\_mips\_instruction\_memory** : includes registers with instructions. These instructions are read from the file named "instruction\_memory.mem". Returns the 16-bit instruction which program counter points.

**instruction\_parser**: Parses the 16 bit instruction to it's properties (opcode, rs, rt, rd, func, imm).

**control\_unit**: Produces control inputs (reg\_des, alu\_src, mem\_to\_reg, reg\_write, mem\_read, mem\_write, branch, alu\_op) for inner components of the mini MIPS processor.

**alu\_control**: Takes alu\_op and func inputs and returns alu\_ctr output which tells ALU to execute which operation.

**sign\_extender**: Takes imm which is produced at instruction\_parser and produces it's 32 bit sign-extended version.

**alu32**: This module is simply modified version of alu32 from HW3. Executes operations depending on input alu\_ctr.

**mini\_mips\_memory**: Includes 2D registers named data\_memory. These registers are loaded with data from file named "data\_memory.mem". If mem\_read input is 1, read\_data is equal to memory content which address points at the data\_memory. If mem\_write is 1, memory content of the specific register's is set to write\_data. This specific register is decided due to address. In the end, content of data\_memory is written to "data\_memory.mem".

**mini\_mips\_registers**: Includes 2D registers named registers. These registers are loaded with data from file named "registers.mem". Content of read\_data\_1 is set to value of read\_address\_1'th register. Content of read\_data\_2 is set to value of read\_address\_2'th register. Content of write\_address'th register is set to value of write\_data. Zero register is always set to 0. In the end, content of registers is written to "registers.mem".

**program\_counter\_handler**: It simply handles PC. If branch input which is produced at the control\_unit and 0'th bit of alu\_result is 1 returns sign\_extended imm which is produced at the sign\_extender. Else returns 1. This part is for computing PC correctly depending on branch. If there is no branch instruction we need to add 1 to the PC. But, if there is a branch instruction is executed we can't simply add 1 to the PC. We need to add the sign extended version of the imm field at the instruction to the PC.

**mux16x1\_32**: 16x1 mux for 32 bit numbers.

**equality\_checker**: Checks whether 2 32 bit numbers are equal to each other. If they are returns 1. Else, returns 0.

I used "registers.mem" file for storing register contents, "data\_memory.mem" file for storing memory contents and "instruction\_memory.mem" file for storing instructions.

\$0 register is always equal to 0. It can't be changed. I calculated expressions for control inputs and coded on Verilog according to them

Inside alu\_32 folder there are modules of the ALU. I updated the ALU from the HW3 and used it. Inside the testbenches folder, there are testbench modules.

## Screenshots:

### Instruction Memory:

```
# time = 0, clock = 0, PC = 00000000000000000000000000000000 , instruction = 1000000001001000
# time = 10, clock = 1, PC = 00000000000000000000000000000000 , instruction = 1000000001001000
# time = 20, clock = 0, PC = 00000000000000000000000000000001 , instruction = 1000010011000010
# time = 30, clock = 1, PC = 00000000000000000000000000000001 , instruction = 1000010011000010
# time = 40, clock = 0, PC = 00000000000000000000000000000011 , instruction = 1001010101001110
# time = 50, clock = 1, PC = 00000000000000000000000000000011 , instruction = 1001010101001110
# time = 60, clock = 0, PC = 00000000000000000000000000000011 , instruction = 0000101100010000
# time = 70, clock = 1, PC = 00000000000000000000000000000011 , instruction = 0000101100010000
# time = 80, clock = 0, PC = 00000000000000000000000000000100 , instruction = 010110111000011
# time = 90, clock = 1, PC = 00000000000000000000000000000100 , instruction = 010110111000011
# time = 100, clock = 0, PC = 00000000000000000000000000000101 , instruction = 0000000000000000
# time = 110, clock = 1, PC = 00000000000000000000000000000101 , instruction = 0000000000000000
# time = 120, clock = 0, PC = 00000000000000000000000000000101 , instruction = 00001011100011
# time = 130, clock = 1, PC = 00000000000000000000000000000101 , instruction = 00001011100011
# time = 140, clock = 0, PC = 00000000000000000000000000000111 , instruction = 0100101010001100
```

### Instruction Parser:

```
# instruction = 1000000001001000, opcode = 1000, rs = 000, rt = 001, rd = 001, imm = 001000, func = 000
# instruction = 1001010101001110, opcode = 1001, rs = 010, rt = 101, rd = 001, imm = 001110, func = 110
# instruction = 0000110000111001, opcode = 0000, rs = 110, rt = 000, rd = 111, imm = 111001, func = 001
# instruction = 010110111000011, opcode = 0101, rs = 110, rt = 111, rd = 000, imm = 000011, func = 011
# instruction = 0101101000111111, opcode = 0101, rs = 101, rt = 000, rd = 111, imm = 111111, func = 111
# instruction = 0000110111100010, opcode = 0000, rs = 110, rt = 111, rd = 100, imm = 100010, func = 010
# instruction = 0000100011010011, opcode = 0000, rs = 100, rt = 011, rd = 010, imm = 010011, func = 011
# instruction = 0001001010001110, opcode = 0001, rs = 001, rt = 010, rd = 001, imm = 001110, func = 110
# instruction = 0011000111010101, opcode = 0011, rs = 000, rt = 111, rd = 010, imm = 010101, func = 101
# instruction = 0100000101011000, opcode = 0100, rs = 000, rt = 101, rd = 011, imm = 011000, func = 000
```

### Registers:

Before running "registers.mem" file:

```
00000000000000000000000000000000 // $0
00000000000000000000000000000011 // $1
00000000000000000000000000000011 // $2
00000000000000000000000000000011 // $3
00000000000000000000000000000011 // $4
00000000000000000000000000000011 // $5
00000000000000000000000000000011 // $6
00000000000000000000000000000011 // $7
```

After running "registers.mem" file:

```
00000000000000000000000000000000 // $0
00000000000001010001011000010101 // $1
00000000000000000000000000000011 // $2
00000000000001010001011000010101 // $3
00000000000000000000000000000011 // $4
00000000000001010001011000010101 // $5
00000000000000000000000000000011 // $6
00000000000001010001011000010101 // $7
```



## Memory:

**Before running “data\_memory.mem” file:**

[illegible]

**After running “data\_memory.mem” file:**

[illegible]

```
# mem_write = 0, mem_read = 1, address = 00000000000000000000000000000000, read_data = 00000000000000000000000000000001, write_data = 00000000000000000000000000000000
# mem_write = 1, mem_read = 0, address = 000000000000000000000000000000010101, read_data = 0000000000000000000000000000000001, write_data = 00000000111111100111111111011011
# mem_write = 0, mem_read = 1, address = 000000000000000000000000000000010101, read_data = 00000000111111100111111111011011, write_data = 00000000000000000000000000000000
# mem_write = 1, mem_read = 0, address = 00000000000000000000000000000000010, read_data = 00000000111111100111111111011011, write_data = 000000000000000000000000010011011
# mem_write = 0, mem_read = 1, address = 00000000000000000000000000000000010, read_data = 00000000000000000000000001011011, write_data = 00000000000000000000000000000000
# mem_write = 0, mem_read = 1, address = 00000000000000000000000000000000011, read_data = 0000000000000000000000000001111, write_data = 00000000000000000000000000000000
# mem_write = 0, mem_read = 1, address = 0000000000000000000000000000000100, read_data = 00000000000000000000000000011111, write_data = 00000000000000000000000000000000
# mem_write = 1, mem_read = 0, address = 000000000000000000000000000000010000, read_data = 00000000000000000000000000011111, write_data = 000000000000000000000001000110101
# mem_write = 0, mem_read = 1, address = 000000000000000000000000000000010000, read_data = 00000000000000000000000001000110101, write_data = 00000000000000000000000000000000
# mem_write = 1, mem_read = 0, address = 0000000000000000000000000000000001011, read_data = 00000000000000000000000001000110101, write_data = 00000000000011111111111111111111
# mem_write = 0, mem_read = 1, address = 0000000000000000000000000000000001011, read_data = 0000000000000111111111111111111111, write_data = 00000000000000000000000000000000
# mem_write = 0, mem_read = 1, address = 0000000000000000000000000000000111, read_data = 00000000000000000000000111111111, write_data = 00000000000000000000000000000000
```



## MINI MIPS:

[illegible]

[illegible]



```
# clock = 0, PC = 00000000000000000000000000000000000010110, instruction = 0000000111011011, opcode = 0000, rs = 000, rt = 111, rd = 011, imm = 011011, func = 101
ALU: input = 0000000000000000000000000000000000000000, input 2 = 00010101010101000001000100101010, result = 00010101010101000001000100101010
reg_des = 1, alu_src = 0, mem_to_reg = 0, reg_write = 1, mem_read = 0, mem_write = 0, branch = 0, alu_op = 0000, alu_ctr = 0101
MEMORY: address = 00010101010101000001000100101010, read_data = 11111111111100000000000000000000, write_data = 00010101010101000001000100101010
REGISTERS: read_address1 = 000, read_data1 = 0000000000000000000000000000000000, read_address2 = 111, read_data2 = 00010101010101000001000100101010, write_address = 011, write_data = 00010101010101000001000100101010
#
clock = 1, PC = 0000000000000000000000000000000000001011, instruction = 0000101010100101, opcode = 0000, rs = 101, rt = 010, rd = 100, imm = 100101, func = 101
ALU: input = 0000000000000000000000000000000000000000, input 2 = 0001010101010100000000000000000000, result = 11101010101010100000000000000000
reg_des = 1, alu_src = 0, mem_to_reg = 0, reg_write = 1, mem_read = 0, mem_write = 0, branch = 0, alu_op = 0000, alu_ctr = 0101
MEMORY: address = 00010101010101000001000100101010, read_data = 11111111111100000000000000000000, write_data = 11101010101010100000000000000000
REGISTERS: read_address1 = 101, read_data1 = 0000000000000000000000000000000000, read_address2 = 010, read_data2 = 11101010101010100000000000000000, write_address = 100, write_data = 11101010101010101010101010101011
#
clock = 1, PC = 0000000000000000000000000000000000000000, instruction = 0000101010100101, opcode = 0000, rs = 101, rt = 010, rd = 100, imm = 100101, func = 101
ALU: input = 0000000000000000000000000000000000000000, input 2 = 1110101010101000000000000000000000, result = 1110101010101010101010101011
reg_des = 1, alu_src = 0, mem_to_reg = 0, reg_write = 1, mem_read = 0, mem_write = 0, branch = 0, alu_op = 0000, alu_ctr = 0101
MEMORY: address = 1110101010101010101010101011, read_data = 11111111111100000000000000000000, write_data = 11101010101010100000000000000000
REGISTERS: read_address1 = 101, read_data1 = 0000000000000000000000000000000000, read_address2 = 010, read_data2 = 11101010101010100000000000000000, write_address = 100, write_data = 1110101010101010101010101011
#
clock = 0, PC = 0000000000000000000000000000000000001100, instruction = 0001000001110001, opcode = 0001, rs = 000, rt = 001, rd = 100, imm = 100001, func = 001
ALU: input = 0000000000000000000000000000000000000000, input 2 = 111111111111111111111111100001, result = 111111111111111111111111100001
reg_des = 0, alu_src = 1, mem_to_reg = 0, reg_write = 1, mem_read = 0, mem_write = 0, branch = 0, alu_op = 0001, alu_ctr = 0001
MEMORY: address = 111111111111111111111111100001, read_data = 11111111111100000000000000000000, write_data = 111010101010101010101010101010101
REGISTERS: read_address1 = 000, read_data1 = 0000000000000000000000000000000000, read_address2 = 001, read_data2 = 111010101010101010101010101010101, write_address = 001, write_data = 1111111111111111111111111111100001
#
clock = 1, PC = 0000000000000000000000000000000000001000, instruction = 0001000001110001, opcode = 0001, rs = 000, rt = 001, rd = 100, imm = 100001, func = 001
ALU: input = 0000000000000000000000000000000000000000, input 2 = 111111111111111111111111100001, result = 111111111111111111111111100001
reg_des = 0, alu_src = 1, mem_to_reg = 0, reg_write = 1, mem_read = 0, mem_write = 0, branch = 0, alu_op = 0001, alu_ctr = 0001
MEMORY: address = 111111111111111111111111100001, read_data = 11111111111100000000000000000000, write_data = 111111111111111111111111100001
REGISTERS: read_address1 = 000, read_data1 = 0000000000000000000000000000000000, read_address2 = 001, read_data2 = 1111111111111111111111111111100001, write_address = 001, write_data = 1111111111111111111111111111100001
#
clock = 0, PC = 0000000000000000000000000000000000001001, instruction = 0001001010001110, opcode = 0001, rs = 001, rt = 010, rd = 001, imm = 001110, func = 110
ALU: input = 111111111111111111111111100001, input 2 = 0000000000000000000000000000000000, result = 111111111111111111111111101111
reg_des = 0, alu_src = 1, mem_to_reg = 0, reg_write = 1, mem_read = 0, mem_write = 0, branch = 0, alu_op = 0001, alu_ctr = 0001
MEMORY: address = 1111111111111111111111101111, read_data = 11111111111100000000000000000000, write_data = 11101010101000000000000000000000
REGISTERS: read_address1 = 001, read_data1 = 1111111111111111111111100001, read_address2 = 010, read_data2 = 11101010101000000000000000000000, write_address = 010, write_data = 1111111111111111111111101111
#
clock = 1, PC = 0000000000000000000000000000000000000000, instruction = 0001001010001110, opcode = 0001, rs = 001, rt = 010, rd = 001, imm = 001110, func = 110
ALU: input = 1111111111111111111111100001, input 2 = 0000000000000000000000000000000000, result = 1111111111111111111111101111
reg_des = 0, alu_src = 1, mem_to_reg = 0, reg_write = 1, mem_read = 0, mem_write = 0, branch = 0, alu_op = 0001, alu_ctr = 0001
MEMORY: address = 11111111111111111111101111, read_data = 11111111111100000000000000000000, write_data = 1111111111111111111111101111
REGISTERS: read_address1 = 001, read_data1 = 1111111111111111111111100001, read_address2 = 010, read_data2 = 1111111111111111111111101111, write_address = 010, write_data = 1111111111111111111111101111
#
clock = 0, PC = 0000000000000000000000000000000000000000, instruction = 0010000001111111, opcode = 0010, rs = 000, rt = 001, rd = 111, imm = 111111, func = 111
ALU: input = 0000000000000000000000000000000000000000, input 2 = 11111111111111111111111111111111, result = 00000000000000000000000000000000
reg_des = 0, alu_src = 1, mem_to_reg = 0, reg_write = 1, mem
```

