



RISC-V External Debug Security Specification

Version v0.5.0, 2024-06-25: Draft

Table of Contents

Preamble.....	1
Copyright and license information.....	2
Contributors.....	3
1. Introduction.....	4
1.1. Terminology.....	4
2. External Debug Security Threat model.....	6
3. Sdsec (ISA extension).....	7
3.1. External Debug.....	7
3.1.1. Machine Mode Debug Control.....	7
3.1.2. Supervisor Domain Debug Control.....	8
3.1.3. Debug Access Privilege.....	8
Configuring dcsr for External Debugger Access Privileges.....	9
3.1.4. Privilege Level Changing Instructions.....	9
3.2. Trace.....	9
Machine Mode Trace Control.....	10
Supervisor Domain Trace Control.....	10
3.3. Trigger (Sdtrig).....	10
3.3.1. Machine mode accessibility to dmode accessibility.....	10
3.3.2. External triggers.....	11
3.3.3. Trigger chain.....	11
3.3.4. Sdtrig CSR.....	11
3.4. Other CSR updates.....	12
3.4.1. Debug Control and Status (dcsr).....	12
3.4.2. Debug PC (dpc) and Debug Scratch Register (dscratch0 and dscratch1).....	13
3.4.3. Sdsec CSR.....	13
4. Debug Module Security Extension (non-ISA extension).....	14
4.1. Debug Module Security Extension Discovery.....	14
4.2. Halt.....	14
4.3. Reset.....	14
4.4. Keepalive.....	14
4.5. Abstract Commands.....	15
4.5.1. Relaxed Permission Check relaxedpriv	15
4.5.2. Address Translation aamvirtual	15
4.6. System Bus Access.....	15
4.7. Security Fault Error Reporting.....	15
4.8. Update of Debug Module Status (dmstatus).....	16
Appendix A: Theory of Operation.....	17
A.1. Debug Module security control.....	17

A.2. Trace Encoder security control	18
Bibliography	19

Preamble



This document is in the [Development state](#)

Expect potential changes. This draft specification is likely to evolve before it is accepted as a standard. Implementations based on this draft may not conform to the future standard.

Copyright and license information

This specification is licensed under the Creative Commons Attribution 4.0 International License (CC-BY 4.0). The full license text is available at creativecommons.org/licenses/by/4.0/.

Copyright 2023-2024 by RISC-V International.

Contributors

This RISC-V specification has been contributed to directly or indirectly by (in alphabetical order): Aote Jin (editor), Beeman Strong, Gokhan Kaplayan, Greg Favor, Iain Robertson, Joe Xie (editor), Ravi Sahita, Robert Chyla, Ved Shanbhogue, Vicky Goode

Chapter 1. Introduction

Debugging and tracing are essential tools utilized by developers to identify and rectify software and hardware issues, optimize performance, and ensure robust system functionality. The debugging and tracing extensions in RISC-V ecosystem play a pivotal role in enabling these capabilities, allowing developers to monitor and control the execution of programs during the development, testing and production phases. However, the current RISC-V Debug and trace specification grants the external debugger highest privilege in the system, regardless of the privilege level at which the target system is running. It leads to privilege escalation issues when multiple actors are present.

This specification defines non-ISA extension [Debug Module Security Extension \(non-ISA extension\)](#) and ISA extension [Sdsec \(ISA extension\)](#) to address the above security issues in the current *The RISC-V Debug Specification* [1] and trace specifications [2] [3].

Below list summarizes changes introduced by *RISC-V External Debug Security Specification*:

- **Per-Hart Debug Control:** Introduce per-hart control knobs to control whether external debug is allowed in machine mode and/or supervisor domains [4]
- **Debug Mode:** External debugger can only halt the hart and enter debug mode when debug is allowed in current privilege mode; all operations are executed with [debug access privilege](#) instead of machine mode privilege
- **Memory Access:** Memory access from a hart's point of view using a Program Buffer or the Abstract Command must be checked by the hart's memory protection mechanisms as if the hart is running at [debug access privilege](#); memory access from Debug Module using System Bus Access block without involving a hart must be checked by system memory protection mechanism, such as IOPMP or WorldGuard
- **Register Access:** Register access using Program Buffer or the Abstract Command works as if the hart is running in [debug access privilege](#) instead of machine mode privilege
- **Triggers:** Triggers (with action=1) can only fire or match when external debug is allowed in current privilege
- **Per-Hart Trace Control:** Introduce per-hart knobs to control whether tracing is allowed in machine mode and supervisor domains

1.1. Terminology

Abstract command	A high-level command in Debug Module used to interact with and control harts
Debug Access Privilege	The privilege with which abstract commands or instructions in program buffers access hardware resources
Debug Mode	An additional privilege mode to support off-chip debugging
Hart	A RISC-V hardware thread
IOPMP	Input-Output Physical Memory Protection unit
Machine mode	The highest privileged mode in the RISC-V privilege model

PMA	Physical Memory Attributes
PMP	Physical Memory Protection unit
Program buffer	A buffer in Debug Module to execute arbitrary instructions on a hart
Supervisor domain	A isolated supervisor execution context defined in RISC-V Supervisor Domains Access Protection [4]
Trace encoder	A piece of hardware that takes in instruction execution information from a RISC-V hart and transforms it into trace packets

Chapter 2. External Debug Security Threat model

Modern SoC development consists of several different actors who may not trust each other, resulting in the need to isolate actors' assets during the development and debugging phases. The current RISC-V Debug specification grants external debuggers the highest privilege in the system regardless of the privilege level at which the target system is running. This leads to privilege escalation issues when multiple actors are present.

For example, the owner of a SoC, who needs to debug their machine mode firmware, may be able to use the external debugger to bypass PMP lock (pmpcfg.L=1) and attack Boot ROM (the SoC creator's asset).

Additionally, RISC-V privilege architecture supports multiple software entities or "supervisor domains" that do not trust each other. The supervisor domains are managed by secure monitor running in machine mode, they are isolated from each other by PMP/IOPMP and they may need different debug policies. The entity that owns secure monitor wants to disable external debug when shipping the secure monitor, however, the entity that owns the supervisor domain needs to enable external debug to develop the supervisor domain. Since the external debugger will be the granted highest privilege in the system, a malicious supervisor domain will be able to compromise machine mode secure monitor with the external debugger.

Chapter 3. Sdsec (ISA extension)

This chapter introduces the Sdsec ISA extension, which extends the Sdext of *The RISC-V Debug Specification* [1]. The RISC-V hart must implement all features in this chapter to ensure external debug security. The Sdsec extension imposes RISC-V privilege level based protection on debug operations and trigger behaviors [1]. Additionally, it constrains trace functionality [2] according to RISC-V privilege levels.

The Sdsec extension exclusively defines the machine mode external debug security control. The Smsdedbg and Smsdetrc extensions [4] comprise the security control for the supervisor domain, expanded by the Sdsec extension with additional details.

3.1. External Debug

The debug operations listed below are affected by Sdsec extension. Within the context of this chapter, **debug operations** refer specifically to those listed, while other operations are excluded.

Debug operations affected by Sdsec extension

- Halting the hart to entering debug mode
- Executing Program buffer
- Serving abstract commands (Access Register, Quick Access, Access Memory)

When the external debug are disallowed in the RISC-V privilege level, the RISC-V hart running in the privilege level behaves as the following:

Behaviors of hart when debug disallowed

- Halt request (haltreq), single step into disallowed privilege or halt group that cause hart to enter debug mode will be pending
- Trigger (with action=1) will not match or fire
- Abstract commands without halting (register access and quick access) will be dropped and set `cmderr` to 6

The subsequent subsections explains how external debug are granted by [machine mode debug control](#) and/or [supervisor domain debug control](#) with respect to hart privilege level.



A pending request to enter debug mode might be dynamically changed from disallowed state to allowed state due to the update of debug controls. For example, the software finished the confidential code and grants external debugger to debug. Afterwards, it spins in a while(1) loop, waiting for debugger to take control and jump out of the loop.

3.1.1. Machine Mode Debug Control

An input port, named `mdbggen[i]`, is introduced to control the debuggability of machine mode for each hart `i`. This signal is propagated to the hart `i` and Debug Module. When `mdbggen[i]` is set to 1, the [debug operations](#) are permitted when hart `i` executes in all modes. Moreover the following rules

apply:

- The **debug access privilege** for the hart can be configured to any privilege level
- If register access without halting the hart is supported, this access carries the privilege of machine mode.

when `mdbgen[i]` is set to 0, the **debug operations** are disallowed and the **behaviors** applies when the hart runs in machine mode.



For a homogeneous computing system, the implementation can consolidate all `mdbgen[i]` into a single port to enforce unified debug policy across all harts.

3.1.2. Supervisor Domain Debug Control

The `Smsdedbg` extension introduces `sdedbgalw` field in CSR `msdcfg` within hart `i` to control debuggability of supervisor domains [4]. The **debug operations** are allowed when hart `i` executes in the supervisor domain only if the logical-OR of values in `sdedbgalw` and `mdbgen[i]` is 1.

The legal value of **debug access privilege** for hart `i` is solely determined by `sdedbgalw` when `mdbgen[i]` is 0. In the event of `sdedbgalw` being 1 while `mdbgen[i]` is 0, the debug access privilege can be configured to privilege levels other than machine mode. Any attempt to set debug access privilege to machine mode will either result in an legal sub-machine mode privilege level or trigger a security fault error (cmderr 6).

If register access without halting is supported, this access bears the privilege of supervisor mode to access the hart when `mdbgen[i]` is 0 and `sdedbgalw` is 1.

The **debug operations** are always disallowed for hart `i` when the logical-OR of `sdedbgalw` and `mdbgen[i]` is 0. In this case, the hart follows the **behaviors** in all modes.

Table 1. External debug allowed privilege levels per debug controls

<code>mdbgen[i]</code>	<code>sdedbgalw</code>	Debug allowed privilege levels
1	x	All
0	1	All except M
0	0	None

3.1.3. Debug Access Privilege

The **debug access privilege** is defined as the privilege with which abstract commands or instructions in program buffers access hardware resources such as registers and memory. This privilege operates independently of hart privilege levels and exclusively affects operations within Debug Mode. Memory and register access within Debug Mode are subject to the **debug access privilege**, with all hardware protections, including MMU, PMP, and PMA, checked against it. This privilege is represented by the `prv` and `v` fields in `dcsr`. The permissible privilege levels programmable to `dcsr` in Debug Mode are elaborated in subsequent sections.

In addition, the `mprv` and `mpp` fields take effect exclusively when the **debug access privilege** is machine mode.

Table 2. Determining maximum debug access privilege with `mdbgen[i]` and `sdedbgalw`

<code>mdbgen[i]</code>	<code>sdedbgalw</code>	Maximum debug privilege allowed
1	x	M
0	1	S(HS)
0	0	None

Configuring `dcsr` for External Debugger Access Privileges

The `prv` and `v` fields in the `dcsr` (at `0x7b0`) have been modified to authorize privilege for external debug accesses. Upon transitioning into Debug Mode, the `prv` and `v` fields are updated to the privilege level the hart was previously operating in. The `dcsr` is always accessible in Debug Mode, and the fields `prv` and `v` are configurable. The maximum debug privilege level that can be configured in `prv` and `v` is determined in Table 2. It will generate a security fault error (`cmderr` 6) if the external debugger attempts to configure `prv` and `v` with a privilege higher than the maximum debug privilege level.



As the `prv` and `v` fields in `dcsr` are Write Any Read Legal (WARL) fields, the debugger has two options to confirm the success of a prior write: either by reading back the attempted written value or by checking the `cmderr`, depending on the hardware implementation choice. The external debugger is able to read back the written value to determine the maximum debug privilege level.

Memory and CSR accesses initiated by abstract commands or from the program buffer will be treated as if they are at the privilege level held in `prv` and `v`. These accesses will undergo protections of PMA, PMP, MMU, and other mechanisms, and triggers traps if they violate corresponding rules.

3.1.4. Privilege Level Changing Instructions

The RISC-V Debug Specification defines that the instructions that change the privilege mode have UNSPECIFIED behavior when executed within the Program Buffer, with exception of the `ebreak` instruction. In Sdsec, those instructions including `mret`, `sret`, `uret`, `ecall`, must either act as NOP or trigger an exception (stopping execution and setting `cmderr` to 3) in Program Buffer. Notably, these instructions retain their normal functionality during single stepping.

3.2. Trace

When Sdsec is supported, the optional sideband signal to trace encoder, `sec_check[i]` [2], must be implemented for each hart `i`, and this signal must be reset to 1. The `sec_check[i]` signal is only cleared when trace is allowed by [machine mode trace control](#) and/or [supervisor domain trace control](#).

Machine Mode Trace Control

For each hart i , an input port, `mtrcen[i]`, controls machine mode trace availability. Setting `mtrcen[i]` to 1 enables machine mode and supervisor domain trace by clearing the `sec_check[i]` signal to 0 across all privilege levels. Conversely, if `mtrcen[i]` is set to 0, the `sec_check[i]` signal cannot be cleared when the hart runs in machine mode.



For a homogeneous computing system, similarly to machine mode debug control, the implementation can consolidate all `mtrcen[i]` into a single port to constrain trace capability across all harts.

Supervisor Domain Trace Control

The `Smsdetrc` extension introduces `sdetr calw` field in CSR `msdcfg` within hart i . The `sec_check[i]` signal for hart i in supervisor domain is determined by the `sdetr calw` field and `mtrcen[i]`. When the logical-OR of `sdetr calw` and `mtrcen[i]` is 1, the `sec_check[i]` signal is cleared while the hart runs in supervisor domain.

When both `sdetr calw` and `mtrcen[i]` are set to 0, the `sec_check[i]` signal cannot be cleared at all.

Table 3. Status of the `sec_check[i]` sideband signal across privilege levels

<code>mtrcen</code>	<code>sdetr calw</code>	Machine mode	Supervisor domain
1	x	<code>sec_check[i] = 0</code>	<code>sec_check[i] = 0</code>
0	1	<code>sec_check[i] = 1</code>	<code>sec_check[i] = 0</code>
0	0	<code>sec_check[i] = 1</code>	<code>sec_check[i] = 1</code>



The `sec_check` signal serves as an additional signal for the trace module, indicating that trace output is prohibited due to security controls. Functionally, `sec_check` behaves identically to the `halted` signal. Both `sec_check` and `halted` signals cannot be active simultaneously. Reserved for future applications, the combined state of `[sec_check, halted]` as 0b11 remains unutilized. In cases where a trace module lacks support for the `sec_check` signal, the hart may alternatively toggle the `halted` signal to restrict trace output.

3.3. Trigger (Sdtrig)

The trigger configured to enter Debug Mode is checked by `Sdsec` extension. The trigger can fire or match in privilege modes when external debug is allowed, as outlined in Table 1.

The extension requires that all pending triggers intending to enter Debug Mode must match or fire before any hart mode switch to prevent privilege escalation.

3.3.1. Machine mode accessibility to `dmode` accessibility

The RISC-V Debug Specification defines that the `dmode` field is accessible only in Debug Mode. When this field is set, the trigger is allocated exclusively to Debug Mode, and any write access from the

hart are disregarded. The Sdsec extension relaxes the constraint to the **dmode**, allowing it to be R/W in machine mode when `mdbgen[i]` is set to 0. When `mdbgen[i]` is set to 1, it remains exclusively accessible within Debug Mode.



The Debug Mode exclusive trigger could potentially serve as an attack surface for unauthorized supervisor domains where debugging is forbidden. With Sdsec extension, machine mode software assumes responsibility for switching the trigger context according to the debug policy enforced for the supervisor domain. As a result, it maintains a clean trigger context for the supervisor domain.

3.3.2. External triggers

The external trigger outputs follow the same limitations as other triggers, ensuring they do not fire or match when the privilege level of the hart exceeds the ones specified in [Table 1](#).

The sources of external trigger input (such as machine mode performance counter overflow, interrupts, etc.) require protection to prevent information leakage. The external trigger inputs supported are platform-specific. Therefore, the platform is responsible for enforcing limitations on input sources. As a result, `tmexttrigger.intctl` and `tmexttrigger.select` should be restricted to legal values based on `mdbgen[i]` and `sdedbgalw`. Their definitions are provided in the [Table 6](#) below.

3.3.3. Trigger chain

The privilege level of the trigger chain is determined by the highest privilege level within the chain. The entire trigger chain cannot be modified if the chain privilege level exceeds the [debug access privilege](#).



This represents a balance between usability and hardware complexity. The integrity of the trigger chain set by the hart must be maintained when an external debugger intends to utilize triggers. There may be instances where the triggers are linked across different privilege levels (e.g., from supervisor mode to machine mode), while the external debugger may only have access to supervisor mode privilege. The external debugger should not alter the chain, because it could suppress or incorrectly raise breakpoint exceptions in machine mode.

3.3.4. Sdtrig CSR

The extension enforces access control in Debug Mode, which complicates trigger usage within Debug Mode. To mitigate these complications, certain trigger CSRs, `tselect`, `tdata1`, `tdata2`, `tdata3`, and `tinfo` are always permitted in Debug Mode, irrespective of the privileges granted to external debuggers. However, the remaining CSRs, `tcontrol`, `scontext`, `hcontext`, `mcontext`, and `mscontext` continue to adhere to the granted debug access privilege.

Table 4. Trigger CSR accessibility in Debug Mode

Register	without Sdsec	with Sdsec
<code>tselect(0x7a0)</code>	Always	<code>mdbgen[i] == 1 sdedbgalw == 1</code>
<code>tdata1(0x7a1)</code>	Always	<code>mdbgen[i] == 1 sdedbgalw == 1</code>

Register	without Sdsec	with Sdsec
tdata2(0x7a2)	Always	mdbgen[i] == 1 sdedbgalw == 1
tdata3(0x7a3)	Always	mdbgen[i] == 1 sdedbgalw == 1
tinfo(0x7a4)	Always	mdbgen[i] == 1 sdedbgalw == 1
tcontrol(0x7a5)	Always	mdbgen[i] == 1
scontext(0x5a8)	Always	mdbgen[i] == 1 sdedbgalw == 1
hcontext(0x6a8)	Always	mdbgen[i] == 1 sdedbgalw == 1
mcontext(0x7a8)	Always	mdbgen[i] == 1
mscontext(0x7aa)	Always	mdbgen[i] == 1

Beyond CSR level accessibility adjustments, the fields within mcontrol, mcontrol6, icount, itrigger, etrigger, and tmexttrigger (variants of tdata1 located at 0x7a1) are redefined to limit the effective scope of triggers as follows.

Table 5. Tdata1 fields accessibility against privilege granted to external debugger

Field	Accessibility
m	mdbgen[i] == 1
s	mdbgen[i] == 1 sdedbgalw == 1
u	mdbgen[i] == 1 sdedbgalw == 1
vs	mdbgen[i] == 1 sdedbgalw == 1
vu	mdbgen[i] == 1 sdedbgalw == 1

The **intctl** and **sselect** field within tmexttrigger are redefined as follows.

Table 6. Redefinition of field **intctl** and **sselect** within tmexttrigger

Field	Description	Access	Reset
intctl	This optional bit, when set, causes this trigger to fire whenever an attached interrupt controller signals a trigger. the field is only configurable when mdbgen[i] is set to 1.	WLRL	0
sselect	Selects any combination of up to 16 Trigger Module external trigger inputs that cause this trigger to fire The legal value must be constrained by mdbgen[i] and sdedbgalw according to trigger input type.	WLRL	0

3.4. Other CSR updates

3.4.1. Debug Control and Status (dcsr)

The access rule for field **prv** and **v** are addressed in subsection [Section 3.1.3.1](#). Beside **prv** and **v**, the fields in dcsr are further constrained based on their sphere of action. When a field is effective in machine mode, it is accessible only to debugger which is granted with machine mode privilege. The

detailed accessibility is listed in the following table.

Table 7. Dcsr fields accessibility against privilege granted to external debugger

Field	Accessibility
ebreakvs	mdbgen[i] == 1 sdedbgalw == 1
ebreakvu	mdbgen[i] == 1 sdedbgalw == 1
ebreakm	mdbgen[i] == 1
ebreaks	mdbgen[i] == 1 sdedbgalw == 1
ebreaku	mdbgen[i] == 1 sdedbgalw == 1
stepie	mdbgen[i] == 1
stoptime	mdbgen[i] == 1
mprven	mdbgen[i] == 1
nmip	mdbgen[i] == 1

3.4.2. Debug PC (dpc) and Debug Scratch Register (dscratch0 and dscratch1)

Debug PC (at 0x7b1) and Debug Scratch Register (at 0x7b2 and 0x7b3) are not restricted by [debug access privilege](#) and are always accesible in debug mode.

3.4.3. Sdsec CSR

The Sdsec extension does not introduce any new CSR. The CSR control knobs in [msdcfg](#) for supervisor domain debug and trace are specified in Smsdedbg and Smsdetr extension respectively in *RISC-V Supervisor Domains Access Protection* [4]. The Smsdedbg and/or Smsdetr extension must be implemented to support security control for debugging and/or tracing in supervisor domain.

Chapter 4. Debug Module Security Extension (non-ISA extension)

This chapter outlines the security enhancements defined for the Debug Module as non-ISA extension. The debug operations listed below are modified by the non-ISA extension. All features in this chapter must be implemented in Debug Module to achieve external debug security.

- Halt
- Reset
- Keepalive request
- Issuing abstract commands (Access Register, Quick Access, Access Memory)
- System bus access

4.1. Debug Module Security Extension Discovery

The Debug Module Security Extension imposes security constraints and introduces non-backward-compatible changes. The presence of the Debug Module Security Extension can be determined by polling the `allsecured/anysecured` bits in `dmstatus` [Table 8](#).

4.2. Halt

The halt behavior for a hart is detailed in [Section 3.1](#). According to *The RISC-V Debug Specification*, a halt request must be responded within one second. However, this constraint must be eliminated as the request might be pending due to the situations where debugging is disallowed. Additionally, when machine mode is not permitted (`mdbgen[i]` set to 0) to engage in debugging, the halt-on-reset (`resethaltreq`) operation must fail and raise security fault error. The debugger could check the error by polling `allsecfault/anysecfault` fields in `dmstatus` for selected harts, as specified in [Table 8](#).

4.3. Reset

The `hartreset` operation resets selected harts. This operation must be prohibited when machine mode is not allowed to be debugged. The security fault error will be raised if the operation is issued when `mdbgen[i]` is 0. The debugger could monitor the error by polling `allsecfault/anysecfault` in `dmstatus`.

The `ndmreset` operation is a system-level reset not tied to hart privilege levels and reset the entire system (excluding the Debug Module). It can only be secured by the system. Thus, it must be de-featured. The debugger can determine support for the `ndmreset` operation by setting the field to 1 and subsequently verifying the returned value upon reading.

4.4. Keepalive

The keepalive operation serves as an optional request for the hart to remain available for debugger. It is only allowed when machine mode is permitted to debug. Otherwise, it causes a security fault

error when `mdbggen[i]` is 0, indicated by `allsecfault/anysecfault` bits in `dmstatus`.

4.5. Abstract Commands

The hart response to abstract commands is detailed in [Section 3.1](#). The following subsection delineates the constraints when the Debug Module issues the abstract commands.

4.5.1. Relaxed Permission Check `relaxedpriv`

The field `relaxedpriv` in `abstractcs` (at 0x16 in Debug Module) allows for relaxed permission checks, such as bypassing PMA, PMP, MMU, etc. However, this relaxation violates security requirements, and the extension mandates that `relaxedpriv` be hardwired to 0.

4.5.2. Address Translation `aamvirtual`

The field `aamvirtual` in `command` (at 0x17 in Debug Module) determines whether physical or virtual address translation is employed. When `mdbggen[i]` is 0, the extension mandates that `aamvirtual` is hardware to 1 and memory access addresses are processed as if initiated by the hart in [debug access privilege](#).

4.6. System Bus Access

System Bus Access enables direct reading/writing of memory space without involving the hart. It must always be checked by bus initiator protection mechanisms such as IOPMP [5], WorldGuard [6], etc. If these protections are not implemented or not deployed for Debug Module, System Bus Access must not be supported. Failed system bus access attempts result in a bus security fault error (`sberror` 6).



In scenarios where a Debug Module lacks System Bus Access, memory access by the debugger can be achieved through the use of abstract commands. These commands provide secure means to access memory.



Trusted entities like RoT should configure IOPMP or equivalent protection before granting debug access to machine mode. Similarly, machine mode should apply the protection before enabling supervisor domain debug.

4.7. Security Fault Error Reporting

A dedicated error code, security fault error (`cmderr` 6), is included in `cmderr` of `abstractcs` (at 0x16 in Debug Module). Misconfigurations of the `dcsr` and issuance of abstract commands under disallowed circumstance will signify such an error. Additionally, the bus security fault error (`sberror` 6) is introduced in `sberror` of `sbscs` (at 0x38 in Debug Module) to denote errors related to system bus access.

The error raised by `resethaltreq`, `reset` and `keepalive` can be identified through the fields `allsecfault/anysecfault` in `dmstatus`. The security fault errors must be detectable prior to any subsequent read of the register responsible for reporting the error. Error statuses are internally

maintained for each hart, with the `allsecfault/anysecfault` fields indicating the error status of the currently selected harts. Any error indicated by `allsecfault/anysecfault` remains until updated through a successful `resethaltreq`, `reset` or `keepalive` operation.



While the `resethaltreq`, `reset`, and `keepalive` operations can potentially take a significant amount of time to complete depending on the implementation, the error status can be immediately reported via following read of `allsecfault/anysecfault` if the operation is prohibited. Therefore, if a read of `allsecfault/anysecfault` indicates no error, it suggests that the operation is allowed and either currently in progress or has been successfully executed.

4.8. Update of Debug Module Status (dmstatus)

31				27				26		25		24		22	
0								allsecfault		anysecfault		defined in Debug Module			
21		20		19		11									
allsecured		anysecured		defined in Debug Module											
10		0													
defined in Debug Module															

Register 1: Newly introduced fields in dmstatus

Table 8. Details of newly introduced fields in dmstatus

Field	Description	Access	Reset
allsecured	The field is 1 when all currently selected harts implement Sdsec extension	R	-
anysecured	The field is 1 when any currently selected hart implements Sdsec extension	R	-
allsecfault	The field is 1 when all currently selected harts have raised security fault due to reset or keepalive operation.	R	-
anysecfault	The field is 1 when any currently selected hart has raised security fault due to reset or keepalive operation.	R	-

Appendix A: Theory of Operation

This chapter explains the theory of operation for the External Debug Security Extension. The subsequent diagram illustrates the reference implementation of security control for the Debug Module and trace encoder, respectively.

A.1. Debug Module security control

As outlined in the specification, the security control on the Debug Module can vary for each hart. The dedicated security policy for hart *i* is enforced by the input port `mdbggen[i]` and the `sdedbgalw` field inside CSR `msdcfg`. The security control logic examines all debug operations and triggers (with `action=1`) firing/matching based on `mdbggen[i]`, `sdedbgalw`, and the privilege level of the hart. The failed action will either be dropped or pending. Additionally, the platform-specific external trigger inputs must obey to platform constraints, which must be carefully handled by platform owner. The `mdbggen[i]` can be bundled in an MMIO (Memory-Mapped I/O) outside the hart, such as in the Debug Module, or implemented as fuses.

The privilege level of the hart is determined by code execution, while the debug requests are validated against the privilege level generated by the hart. This process involves two actors, which may lead to a potential Time-of-Check Time-of-Use (TOCTOU) issue. To mitigate this, the implementation must ensure that the inspection and execution of debug requests occur within the same privilege level of the hart. Failure to do so could result in debug requests bypassing access controls intended for higher privilege levels. If the accesses fail the security check, it must prompt an immediate termination of access to prevent any information leakage.

When the external debugger is stepping through an instruction that triggers a transition to a higher privilege level, the security control logic must verify against debug capability according to [Table 1](#) before entering Debug Mode. If debugging is permitted, the hart re-enters Debug Mode after executing the instruction. Otherwise, the hart continues executing with the pending single step request until it becomes debuggable and can re-enter Debug Mode. In scenarios where multiple supervisor domains are debuggable, the secure monitor in machine mode may switch the context during single stepping. In such cases, the debugger might stop in a different application than the original one. Users of the debugger should be mindful of this possibility.

Application-level debugging is primarily accomplished through self-hosted debugging, allowing the management of debug policies at the supervisor/hypervisor level. As a result, user-level debugging management is not addressed within this extension.



Figure 1. The security control on Debug Module

A.2. Trace Encoder security control

Similar to the Debug Module, the trace encoder is controlled by the `mtrcen[i]` and `sdetrca1w` in CSR `msdcfg` for each hart `i`. The halted sideband signal to the trace encoder is determined by [Table 3](#).

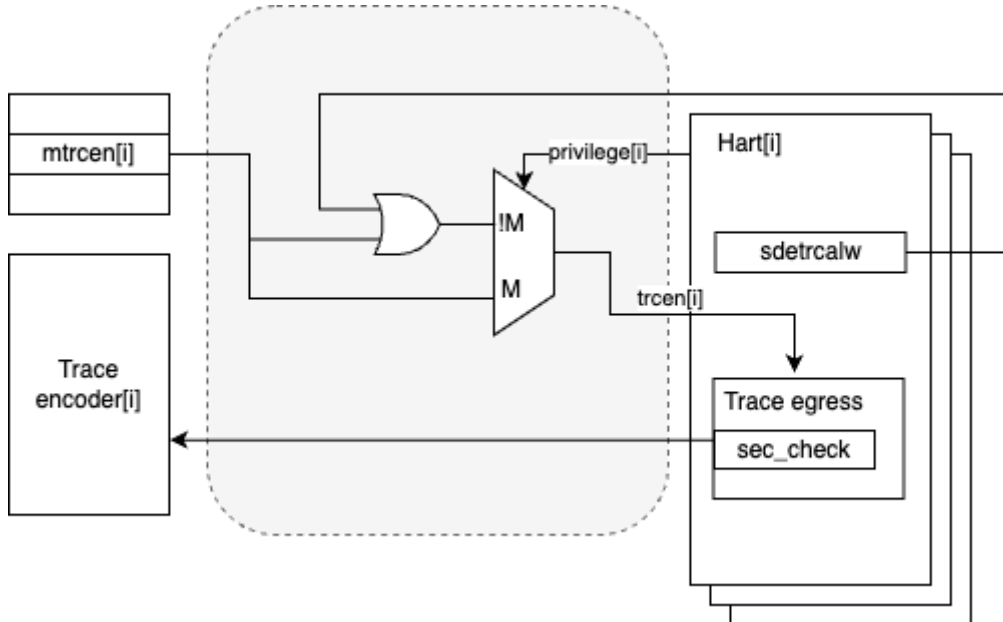


Figure 2. The security control on trace module

Bibliography

- [1] “RISC-V Debug Specification.” [Online]. Available: github.com/riscv/riscv-debug-spec.
- [2] “RISC-V Efficient Trace for RISC-V.” [Online]. Available: github.com/riscv-non-isa/riscv-trace-spec.
- [3] “RISC-V N-Trace (Nexus-based Trace) Specification.” [Online]. Available: github.com/riscv-non-isa/tg-nexus-trace.
- [4] “RISC-V Supervisor Domains Access Protection.” [Online]. Available: github.com/riscv/riscv-smmmtt.
- [5] “RISC-V IOPMP Architecture Specification.” [Online]. Available: github.com/riscv-non-isa/iopmp-spec/releases.
- [6] “WorldGuard Specification.” [Online]. Available: github.com/riscv-admin/security/blob/main/papers/worldguard%20proposal.pdf.